DEVELOPMENT OF AN ACOUSTIC SUSPENDED SEDIMENT MONITORING SYSTEM

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Abstract: Suspended sediments represent a serious worldwide pollutant which need to be monitored and ultimately controlled. Significant entrainment and transport of these sediments occur during adverse weather conditions and during relatively short time spans which make manual sampling and monitoring cumbersome, inefficient and dangerous. Toward that end, the development of a remote autonomous acoustic system to monitor suspended sediments in fluvial systems is considered. The system will transmit an arbitrary waveform via a Digital Analog Converter (DAC) and power amplifier using user defined inputs. This waveform can be any frequency up to 5 MHz. The receiver section is composed of two parts; 1) the modular pre-amplifier section which will incorporate the transmit/receive function, transducer impedance matching section and appropriate signal preconditioning in the form of voltage gain and 2) the Analog to Digital converter, which is a 12-bit 65 MSPS CMOS pipelined multi-stepped converter. The resulting A-D conversion is stored in the 16 MB of onboard RAM. The stored results are processed by an Analog Devices Blackfin ADSP-533 Digital Signal Processing chip. Other features of the unit include a serial port interface, a JTAG interface used in real-time emulation, a serial programming port which would allow real-time programming, a peripheral programming interface allowing easy changes to any of the control routines for the various peripherals and onboard power control and reset functions. The operation of the unit starts with a trigger from a stage height decision, either internally or externally, indicating that an event has occurred that warrants observation. The backscatter data is then collected for an amount of time depending on the determined depth. Multiple data sets are collected, processed using Fast Fourier Transforms and stored in memory at a rate of up to 3 times a second. Depending on the length of data capture, they are archived on board or sent to a host computer via serial port or wireless transfer. The unit is DC powered and may be put to sleep when there is no data to take to extend field deployments. This work has been supported by the USDA.

INTRODUCTION

Existing lab based systems to monitor suspended sediment are often based on personal computers (PC's) and 3rd party software and hardware for data acquisition. These types of systems have an advantage in that they are turn-key systems that usually require little if any modification. However they suffer two main disadvantages. The first is that even in a PC notebook configuration, they are not suited to long term exposure to the environment in which a suspended sediment monitoring system is deployed. The second disadvantage is one of cost. Unit costs may easily exceed several thousands of dollars when all factors are considered. The system under development seeks to alleviate both of these issues by being a rugged system that may be deployed in a variety of environments including the possibility of being submerged under water. With a per unit cost under $200USD, and the possibilty of becoming less expensive as

the individual integrated circuit technology matures, the unit under development will be far more affordable than current alternatives.

DESIGN CONSIDERATIONS

The primary design consideration that drove all other decisions was to make the system inexpensive due to the large number of potential data sites. This consideration eliminated any type of PC solution and suggested that some type of embedded system should be used. After an extensive review of available systems and integrated circuits it was decided to use an Analog Devices ADSP-BF533 Digital Signal Processing (DSP) integrated circuit (IC). This particular IC was designed to be used in video systems and high-end audio applications, such as cellular telephones. One of the challenges was the frequency range needed for the range of suspended sediments of interest. This application calls for a frequency range of approximately 500 kHz to around 5MHz (Kinsler et al.2000, Crocker 1998). The Nyquist Theorem calls for a sampling frequency of at least twice the highest frequency of interest (Smith, 2003), with a maximum frequency of 5 MHz yielding a 10 MSPS minimum acquisition rate. The chip chosen easily handles this data rate.

Other considerations included power consumption and portability. Since the IC chosen is used in cell phones and hand-held video devices it has a wide variety of power management modes, allowing long battery life and needing a minimum of external chips.

HARDWARE OPERATION

The system's primary function is to perform a Fast Fourier Transform (FFT) on the backscattered acoustic data. The FFT is a 1024 point complex radix-2 FFT. The routine takes 1024 points of data, performs the FFT on it and picks out the magnitudes for the three frequencies of interest. This process is done 392 times (representing a 1.28 mm range bin resolution for the anticipated creek depth of 5m) to complete one data set. Next the average of 20 data sets is found for each of the three frequencies. These averaged values are then transmitted back to the host Personal Computer (PC).

Setup of the system prior to field deployment will consist primarily of loading the flash memory unit with the desired programs. The flash memory unit has 1 MB available for program storage and must be programmed prior to deployment. Other issues are appropriate connections to peripheral systems such as specific transmit and communication connections. If desired, the unit may be placed in sleep mode such that the host computer may be used to wake the system via the serial port interface to start operations. Alternatively, an external power switch may be used. In some applications it may be desirous to minimize the number of openings in the system housing due to environmental concerns. Power and transmitting connections are relatively easy to harden against the environment but other connections such as switches could lead to increased cost and complexity.

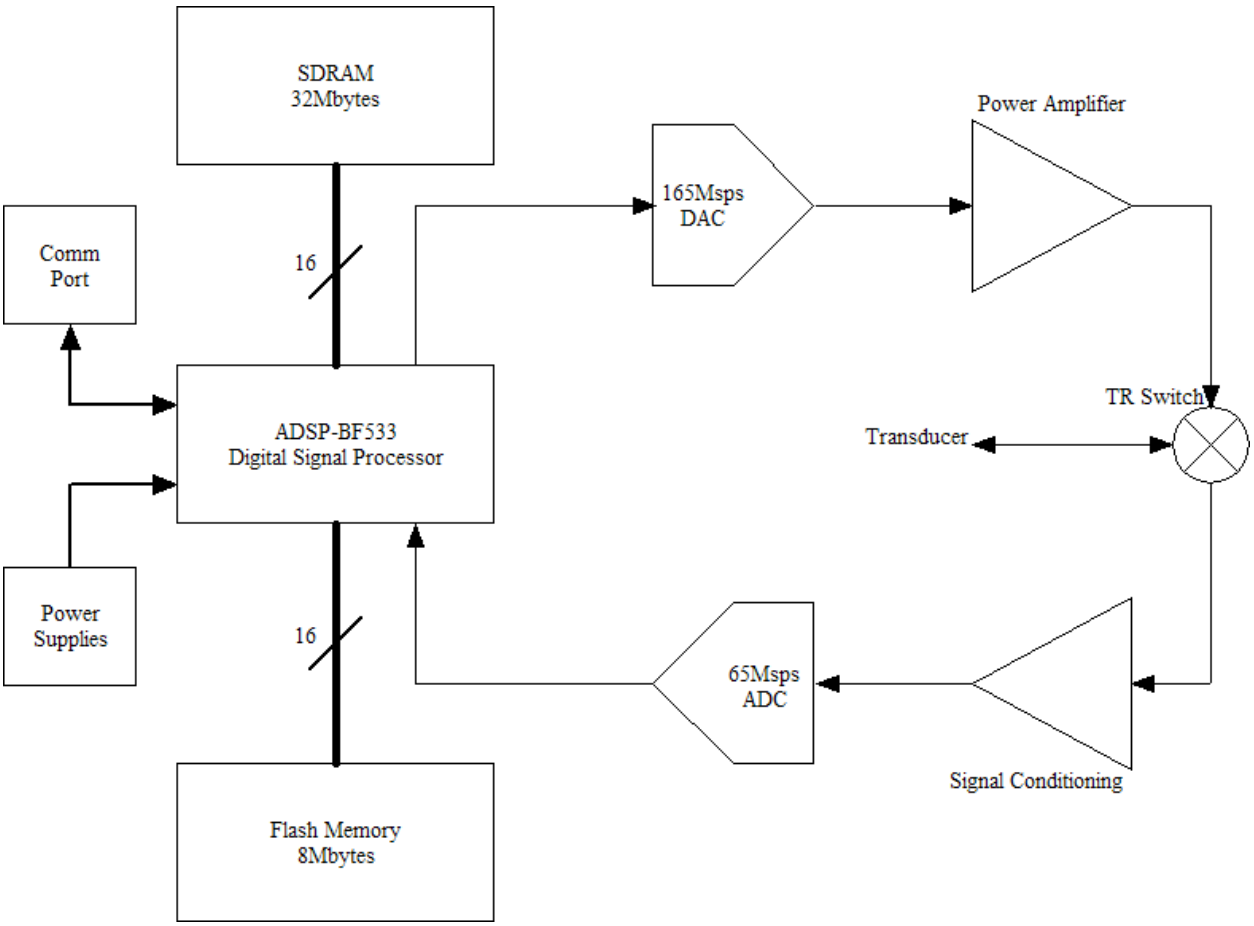

Figure 1 Block Diagram

Operation of the system begins with power being applied. At this time the DSP chip goes into a program loading mode called "boot loading" where the program stored in the onboard flash memory is loaded into the internal memory of the DSP and the system prepares to start taking data. After the boot operation is complete the first task performed is to check for connection to the land-based host computer. If communications are established the host computer will determine when data acquisition should begin. Generally this will be decided by a stage height monitoring system also connected to the host computer. Functions that may be performed while connected to the host computer include setting the data acquisition rate, transmitting of processed data, re-transmitting of processed data, initiating power saving modes and unit shutdown. In the event that communications are not established data acquisition will start automatically. The unit may also be instructed to wait for an activation signal directly from the stage height monitoring system. This is achieved through a hard wired connection to the stage height sensor. This data acquisition will continue until the memory buffer is full.

The data acquisition routine starts with a transmit pulse or chirp. The system has two transmit modes. The first mode is a single frequency mode which can generate any single frequency up to 20 MHz depending on transmitter power and transducer choices. The second mode is an arbitrary waveform mode which transmits a user defined waveform. The DSP chip has the capability to convert any mathematical expression into the necessary analog signals by

communicating with a 165 MSPS Digital to Analog Converter (DAC) chip. The output from the DAC is fed to the power transmitter circuitry which is chosen for a specific transducer type. The current transmitter circuitry is suited to transducers ranging in frequency from around 500 kHz to 5 MHz with impedances in the 50 ohm to 200 ohm range (Horowitz, 1989). Other transducers would require the appropriate transmitter circuitry.

After the transmitter pulse is generated and transmitted the system goes into a 134.04 μs wait state. This period allows time for the mechanical ring down of the transducer and to account for transducer near field effects. Depending on transducer type, impedance, and transmit levels this time may be adjusted. After the wait state is over, the system goes into receive mode. The time that the unit is receiving backscatter echoes is determined by the depth of the stream. This depth is determined in one of two ways. The first method is from the host computer which will relay depth information from the stage height sensor in the form of a status word. If the stage height information is not available the system can ping the bottom and acquire the depth itself by analyzing the return echoes. The second method is not as reliable since the algorithm for determining the bottom is affected by various factors, with the sediment flow being the primary one that could return a false bottom. There is also a default depth which is currently set at 5 meters.

The backscatter echoes from the entrained sediment are first sent to a signal conditioning circuit which matches impedance with the transducer, amplifies (if necessary) and anti-aliases the signal before it is applied to the Analog to Digital Converter (ADC). In the design phase an attempt was made to use standard parts for the amplifier section of the signal conditioner in order to accommodate various types of transducers, filter requirements, and gain. Also included in this stage is a diode clamp which acts as a transmit-receive switch to keep the high voltage of the transmitter stage out of the receiver stage. This section also converts the incoming transducer signal into a differential signal to drive the following ADC. In designing the signal conditioning stage, care was taken to insure that the IC's used were industry standard parts with standard pin outs. This decision was made to insure compatibility with as many types of transducers as possible. The bandwidth of the existing signal conditioning stage is approximately 10 MHz.

The ADC section is a 12-bit 65 MSPS integrated circuit with a Signal-to-Noise ratio of 72 dB. The ADC is configurable with a variety of input voltage levels and reference voltages to allow flexibility depending on the application. Some of the changes are software configurable by sending control words to the DSP and others are hardwired changes made during the board construction phase. The ADC digital output is fed directly to the synchronous dynamic ram under control of the SDRAM controller on the DSP. Both the control input and the analog signal inputs to the ADC are differential to reduce noise and jitter (Kester, 2003).

The DSP section is an Analog Devices ADSP-BF533 Digital Signal Processing integrated circuit. This chip is capable of running at a core clock speed of 756 MHz with a corresponding 1512 Million Multiply and Accumulate (MMAC) cycles. The prime function of the DSP is to take the raw backscatter data out of the SDRAM and perform a 1024-point complex radix-2 Fast Fourier Transform on that data and store the result back into the SDRAM. In addition to the core processing functions of the BF533, there are a number of other functions that it handles in controlling the system. One of these functions includes power management. By varying the

voltage and frequency significant power consumption reductions may be obtained. An example of where this might prove useful is during those times when a stream has too little water to maintain sediment flow. By utilizing the real time clock, you may dramatically reduce the power consumption of the chip by lowering the core voltage and since there is no processing to be done at the time, the clock speed as well. When the stage height monitoring system detects an event that needs observation the real time clock (RTC) can bring the processor back up to full speed. There are 5 modes of dynamic power management, each with a different power profile that can be used depending on needs and what types of external signals may be available to the system. With a real time clock subsection available, the processor can be put on an alarm system to awake once an hour or once a day to establish communications and make a determination if data collection is needed and if not, go back to sleep.

SOFTWARE AND MEMORY

The FFT routine is performed by dividing the raw data set into 1024 point bins, performing an FFT on each bin and picking out the magnitude of the frequency of interest. The number of bins will be determined by the depth of the measurement, e.g. a depth of 5 meters (the maximum depth available with the current system) would yield 392 bins. This number is arrived at by taking the number of raw data points and dividing by 1024. The number of raw data points is arrived at by taking the travel time of the acoustic signal times the ADC sampling rate. For 5 meters and a temperature of 20 degrees Celsius the equation would yielding a total number of raw data points of 402,220 (6.705 ms x 60 MSPS = 402,220). The 402,220 data points are then divided by the 1024 point FFT size to yield 392 individual bins. The number of data points may not be a multiple of 1024. In that case any left over data points are discarded. For three frequencies, the FFT routine needs 11,874 clock cycles. If the core speed of the DSP is set for 750 MHz the total FFT time would be 15.82 ms. This process is completed 20 times and the resulting FFT magnitudes are averaged together to create the final processed data set that is sent to the host computer. Including acoustic transmit and receive time, processing time and communications time, one processed event will take approximately 450 ms to complete. The amount of raw data collected for one processed event is approximately 320 MB while the processed event itself represents just a little over 2 KB of data. Depending on depth and sample rate there is enough onboard memory to store several minutes of processed data to insure that communication issues are not allowed to interfere with data collection and processing.

The routine that performs the FFT is 847 KB, while the communication routine is 77 KB. The routines are stored in the flash memory unit, separate from the SDRAM, and there is a total of 1 MB of storage in the flash memory. The communication routine and most of the FFT routine is common to any operation that the system may be asked to perform. The additional flash memory space may be used to store other possible profiles that the user may wish to run. These alternative profiles may be started by the host computer or by setting threshold conditions based on the processed data being accumulated. By allowing the user to pre-load various profiles and operating conditions a tremendous amount of flexibility is built into the system.

COMMUNICATION AND POWER

Communication between the host PC and the DSP system is provided by way of a serial port. The RS-232 standard was chosen due to the availability of standard and relatively inexpensive radios. At present the radio is an external component allowing each user to determine their best communication method. In current deployments both hard wired connections and radio links are used. Power is handled by onboard regulators that will accept an input voltage in the range of 5 VDC to 24 VDC. Power consumption is determined by the amount of time the unit is acquiring data and at what data rate the ADC is being operated. The higher the frequency of both the ADC and the DSP the more power consumed.

CONCLUSIONS

The system as described is both flexible and powerful. The DSP excels at performing FFT operations making the process of collecting and transmitting data a relatively simple one. The ability to communicate with the unit on the fly gives the user an opportunity to evaluate the data and make corrections or adjustments in the data collection routine without necessarily pulling the unit out of the experiment. Concerns and future improvements center on several areas. The first is power. Even with the different power modes available, this system will need approximately 1.5 Amp hours to run full-time. In meeting our current needs the system will not be processing data around the clock but only in instances where it is needed, such as storm events, renewable power sources will be needed. The primary consumers of power are the ADC and the DSP and both are optimized for power consumption. The second issue that will be addressed is communications. Currently the only communication method available is RS-232 to external radio or hard wired to a host computer. Investigations are underway concerning onboard radios and modems and also other serial standards, including differential standards for when communication must be hard wired and the cable runs are long. Another area that will be addressed is memory. Depending on communication issues, the system may be outfitted with sufficient memory to store days or weeks of data. This would facilitate remote locations where communication with a host computer may be impractical. It is anticipated that future systems will be even less expensive as the technology employed matures.

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