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Self-calibrating seismic amplifier and telemetry system

by

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This report is preliminary and has not been edited or reviewed for conformity with Geological Survey standards and nomenclature.

Self-calibrating seismic amplifier and telemetry system

Introduction

A frequency modulated, constant bandwidth, telemetry system has been designed to transmit simultaneously up to 8 channels of seismograph data from remote locations to a central recording site via radio or voice-grade telephone circuit. By utilizing state-of-the-art integrated circuits, the size of the remote unit has been considerably reduced over previous equipment and the power consumption has been decreased by a factor of over 100 to less than 2 milliwatts. This reduction in size and power makes it possible to package the electronic equipment, together with a year's supply of batteries, in a container the size of a tennis-ball can. The field equipment for a short-period station is now sealed in a 3-inch plastic tube 22 inches long. The tube, together with the connecting cable to the telephone terminal, is buried; greatly reducing losses due to water flooding, pilferage, etc. An important addition to the field unit is a daily calibration of the seismometer and amplifier.

Specifications and instructions for the three units that compose the system are presented separately, as follows:

1. J302 Preamplifier and voltage controlled oscillator
2. C-4 Calibrator
3. J101 Discriminator

J302 Preamplifier and Voltage-Controlled Oscillator Unit

A. General

The J302 Preamplifier and Voltage Controlled Oscillator (VCO) Unit (Figure 1) is designed primarily as a seismic signal amplifier and conditioner. This unit amplifies and filters seismic signals in the microvolt to millivolt range and bandwidth of from 0.1 to 30 Hz (Figure 2), then frequency modulates an audio carrier with the amplified seismic signal. This method allows low frequency seismic signals to be telemetered by telephone line or by radio link to a recording site. The modulated carriers can be multiplexed so that as many as 8 seismic signals can be transmitted over one voice grade phone line or radio link.

B. Specifications

1. Noise referred to input: 1.0 microvolt peak to peak with a source impedance of 10,000 ohms and a bandwidth of 0.1 Hz to 30 Hz.
2. Bandwidth, 3 db points: 0.1 Hz to 30 Hz with 12 db/octave roll-off.
3. Gain: Voltage gain 90 db max., with 48 db atten in 6 db steps.
4. Input: Differential, 10,000 ohms input impedance.
5. Supply voltage: ±4.05 vdc at 200 microamps with output lvel at -10 dbm.
6. VCO stability: 100 ppm/degree centigrade.
7. Output distortion: Harmonic frequencies less than 3% of fundamental frequencies.
8. Output level: -5 dbm maximum into a 600 ohms load, adjustable.
9. Output impedance: 600 ohms.
10. Carrier deviation: ±125 Hz, limited to 135 Hz maximum.
11. VCO sensitivity: Adjustable from $\frac{2\text{Hz}}{\text{microvolt}}$ to $\frac{0.001\text{ Hz}}{\text{microvolt}}$ referred to input.
12. Operating temperature range: -30 degrees C. to +50 degrees C.

C. Theory of Operation

The J302 (Figure 3) consists of a preamplifier (A1), an amplifier (A2), and a voltage-controlled oscillator (VCO), along with associated filtering and wave shaping circuitry. The seismic signal is direct-coupled to the preamplifier which has an input impedance of 10,000 ohms. This amplifier stage has resistance and capacitance feedback to provide a fixed gain of 48 db and low-pass filtering with 6 db per octave roll-off above 30 Hz. The D.C. offset of this amplifier can be nulled with R7.

The preamplifier and amplifier stages are resistance-capacitance coupled through C3 and R8, resulting in high-pass filtering with 6 db per octave roll-off below 0.1 Hz. Series resistors R25 through R33 provide 48 db of attenuation in 6 db steps.

The amplifier stage also has resistance and capacitance feedback with a fixed gain of 42 db and low pass filtering with 6 db per octave roll-off above 30 Hz. The D.C. offset of this stage can be nulled with R13. Both A1 and A2 are micropowered integrated circuit operational amplifiers that require about 15 μa each to operate at ±4 VDC.

The output of the amplifier stage is resistance-capacitance coupled through C5 and R14 and R15 to the VCO stage to produce 6 db per octave roll-off below 0.1 Hz. The result is an amplifier system with a maximum voltage gain of 90 db and a bandpass of 0.1 Hz to 30 Hz with 12 db per octave roll-off outside of these frequencies.

The VCO utilizes only the VCO section of a COS MOS phase-locked-loop integrated circuit. The amplified seismic signal is fed into the VCO through potentiometer R15, which functions as a deviation control. The center frequency of the VCO is determined by C6 and R22 with potentiometer R21 being a fine adjustment control for the center frequency. The center frequency of the

VCO is temperature compensated by the circuit consisting of R17, R18, R19, and thermistor R20. The output of the VCO is fed through potentiometer R23, the output level adjust control, into I1, C8, and C7, the wave shaping network, then into the output transformer T1. The center frequencies given in Table I have become standard in the transmission of seismic data by constant bandwidth methods. All frequencies are operated in a constant bandwidth system, each having a maximum deviation of ± 125 Hz.

D. Alignment Procedures

1) Amplifier Section

Insert integrated circuits A1, A2, and VCO into their respective sockets (Figures 4 and 5), shunt the preamplifier input with a 10 K ohm resistor, and apply ±4VDC power. Connect an oscilloscope to common and tie point 1 (TP1) and adjust R7 for OVDC ±5 MV. Next, connect the oscilloscope to tie point 2 (TP2) and adjust R13 for OVDC ±5 MV. Last, connect the oscilloscope to the amplifier monitor and remove the 10 K ohm shunt from the input to A1. Connect a microvolt AC signal source across the inputs to A1 and monitor the amplifier output for proper gain at each attenuator setting. Gains may vary a maximum of 10%.

2) VCO Section

To align the VCO to the proper center frequency, determine the resistor and capacitor values from Table I and install them. These values are only approximate and some trimming may be required. R21, the center frequency adjust pot provides about 2% adjustment of the center frequency.

Load the secondary of output transformer T1 with 600 ohms and connect a frequency counter and an oscilloscope across the load. Set the attenuator switch to 48 db so that no amplifier noise will modulate the carrier frequency. C7 should be trimmed to obtain a maximum output with distortion held to less than 3%. C8 may be trimmed if necessary to meet this objective.

To set the deviation of the VCO, apply 3VDC between common and the amplifier monitor, and adjust R15 for 125 Hz offset of the carrier frequency. Reverse the polarity of the 3VDC and check for 125 Hz in the opposite direction. A positive monitor voltage should give a positive deviation.

For a more precise setting of the carrier deviation to standardize the overall gain between units in hertz/microvolt, the following procedure can be used: With the attenuator set at 0 db, apply a 10 microvolt RMS 5 Hz signal to the preamplifier input. Measure the amplifier output at the amplifier monitor in volts peak to peak. Insert the measured value in the following equation. The result will be the proper sensitivity of the VCO in hertz/volt:

$$\frac{36.9}{\text{measured volts peak to peak}} = \text{deviation in hertz/volt}$$

Apply a known dc voltage of 3 volts or less to the amplifier monitor and set the deviation control (R15) for the proper number of hertz offset. The preamplifier/VCO sensitivity at this setting is 1.32 Hz/microvolt referred to the preamplifier input.

TABLE I

Frequency	C6 uf	C7 uf	C8 uf	R 34
680 hz	.0015	.033	.033	300 ohm
1020 hz	.0015	.022	.015	270 ohm
1360 hz	.001	.012	.0082	240 ohm
1700 hz	.001	.0068	.0068	200 ohm
2040 hz	.001	.0047	.0047	180 ohm
2380 hz	.001	.0039	.0033	150 ohm
2720 hz	.00068	.0033	.0027	130 ohm
3060 hz	.00068	.0027	.0022	100 ohm

R22 varies with individual VCO ICs. Minimum value for R22 should not be less than 300 K ohms. Maximum value may be 3 meg ohms.

Table II--Parts list, J302 Preamplifier-VCO

Component	Value
R1, R2	4.99k RN55D 1%
R3, R4	1.5 Meg 1/4w 5%
R5, R11	51 ohm 1/4w 5%
R6, R12	5.1 Meg 1/4w 5%
R7, R13, R23	100k trimpot
R8, R9	66.5k RN55D 1%
R10	8.2 Meg 1/4w 5%
R14	51k 1/4w 5%
R15	200k trimpot
R16	150k 1/4w 5%
R17, R24	100k 1/4w 5%
R18	91k 1/4w 5%
R19	30k 1/4w 5%
R20	10k thermistor Fenwall KP41J2
R21	50k trimpot
R22	300k - 3 Meg 1/4w 5% Frequency dependent
R25	16.2k RN55D 1%
R26	8.06k RN55D 1%
R27	4.02k RN55D 1%
R28	2.00k RN55D 1%
R29	1.00k RN55D 1%
R30	499 ohm RN55D 1%
R31	249 ohm RN55D 1%
R32, R33	124 ohm RN55D 1%
R34	Frequency Dependent See Table I

Trimpots; Spectrol 43W series or equivalent

Component	Value
C1, C2	.0022uf CK05BX222 K
C3	25uf 6VNP, GE 29F538
C4	.00039uf CK05BX391K
C5	7.5uf 6VNP Sprague 151D
C6	.00068-0015uf NPO type see Table I
C7, C8	.0027uf-.1uf C D WMF series Frequency dependent, see Table I.
I1	1.5hy choke Mot. 25B82751D01
T1	25k pri. 500 ohm sec. UTC SSO 14 or equivalent
S1, S2	16 pin DIP sockets Amphenol 821 25011 164
SW1	12 pos. rotary switch Grayhill switch 71AY23179
A1, A2	National op amp LM4250CN
VCO	RCA COS/MOS ppl CD4046AE
P1-P15	teeminals, USECO 2003 B

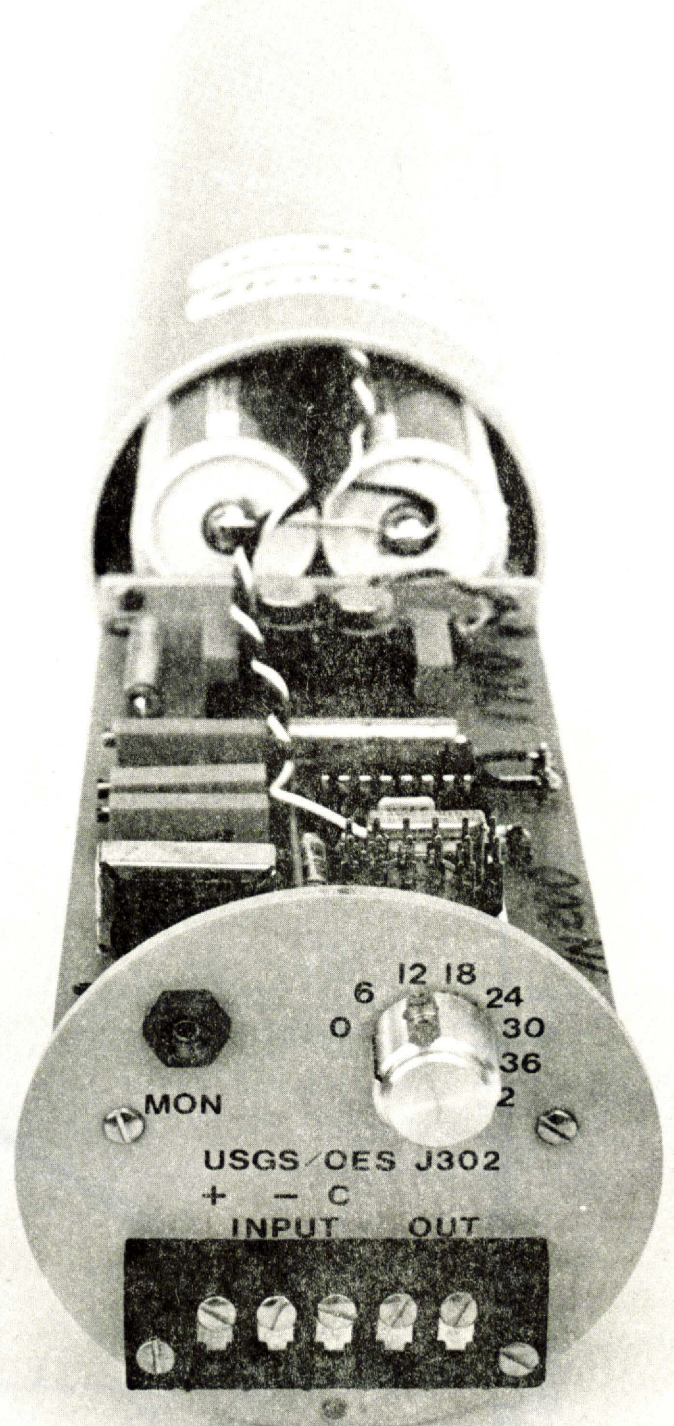


FIGURE 1

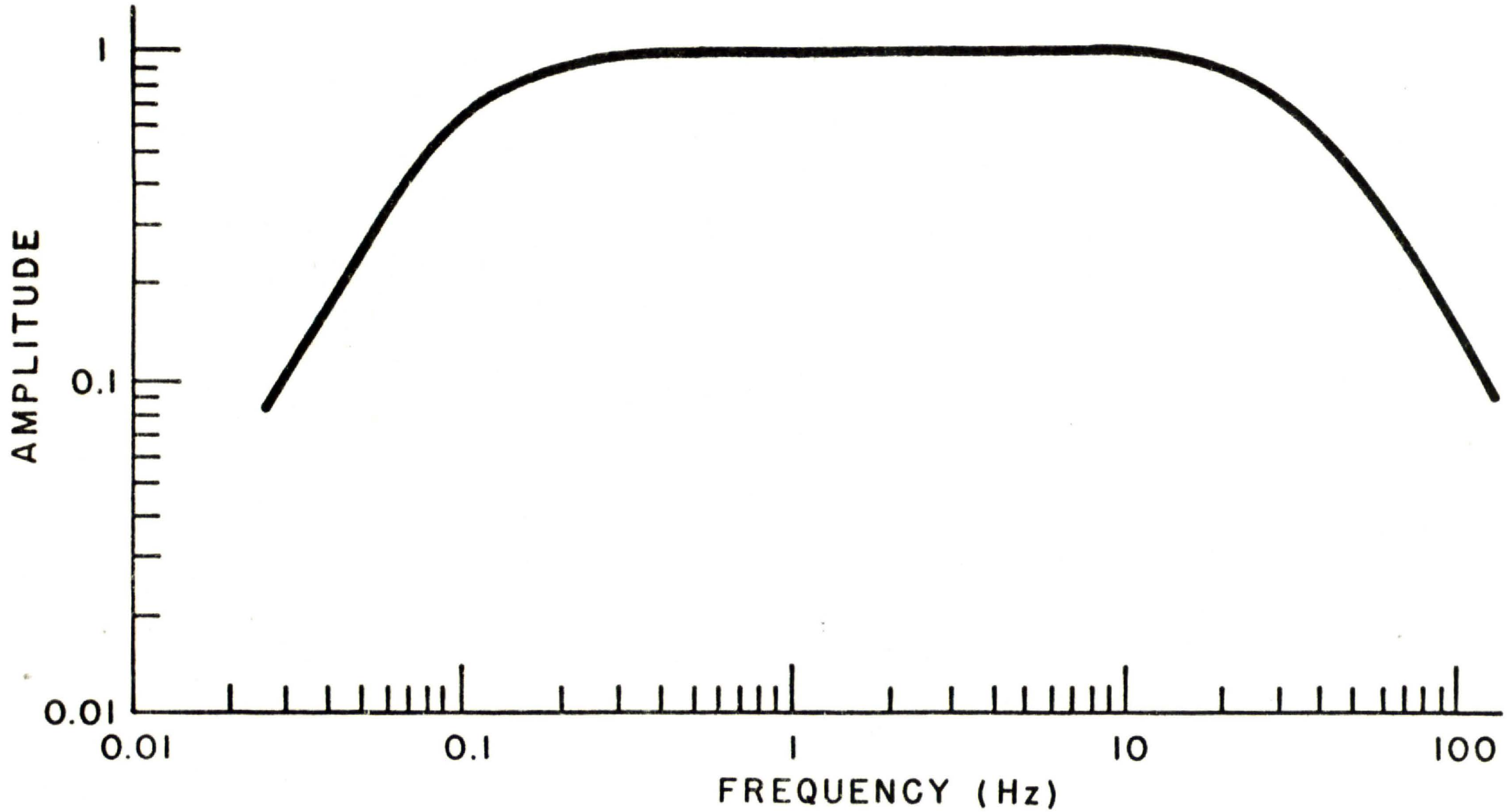
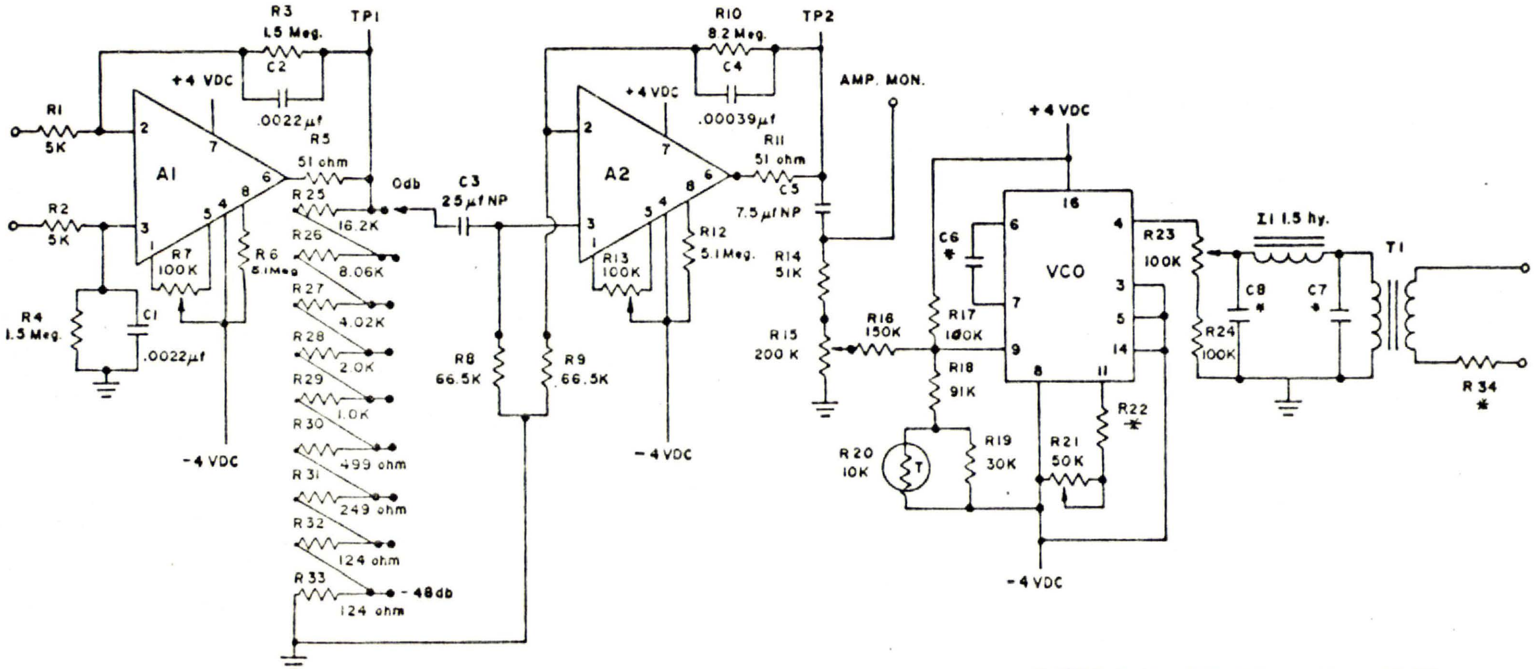


Figure 2. Frequency response of J302 Preamplifier/VCO at amplifier monitor.

Figure 3 J302 Preamplifier / Voltage Controlled Oscillator



* FREQUENCY DEPENDENT COMPONENTS
SEE TABLE I

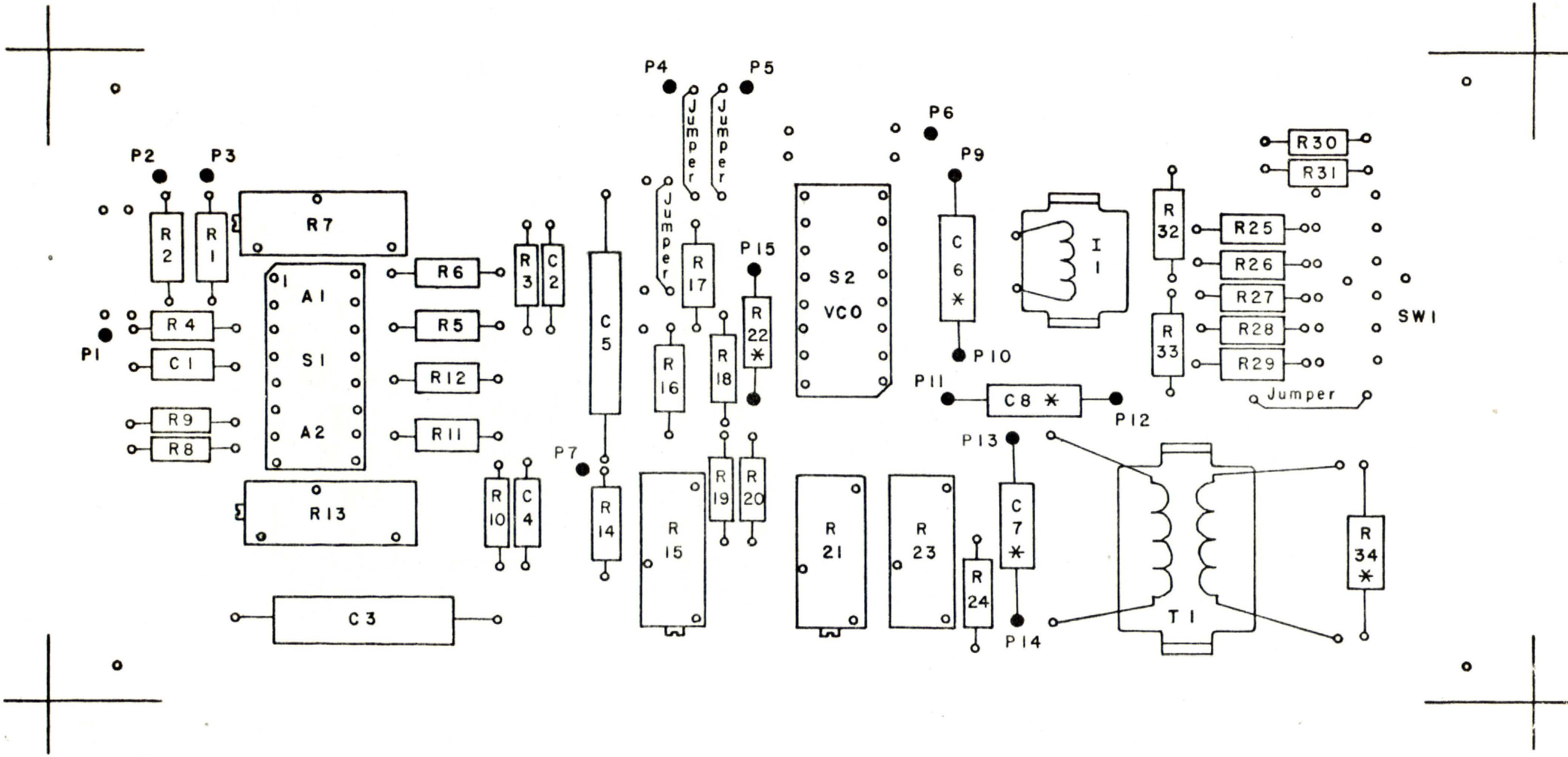


Figure 4. Component Layout, J3-2 Preamplifier/VCO

Terminal Points

* Starred components, frequency dependent

P1	Input shield	P5	Batt - 4.05V
P2	Input +	P6	Batt common
P3	Input -	P7	Amplifier monitor
P4	Batt + 4.05V		

Circuit Board J302 Preamplifier/Voltage Controlled Oscillator

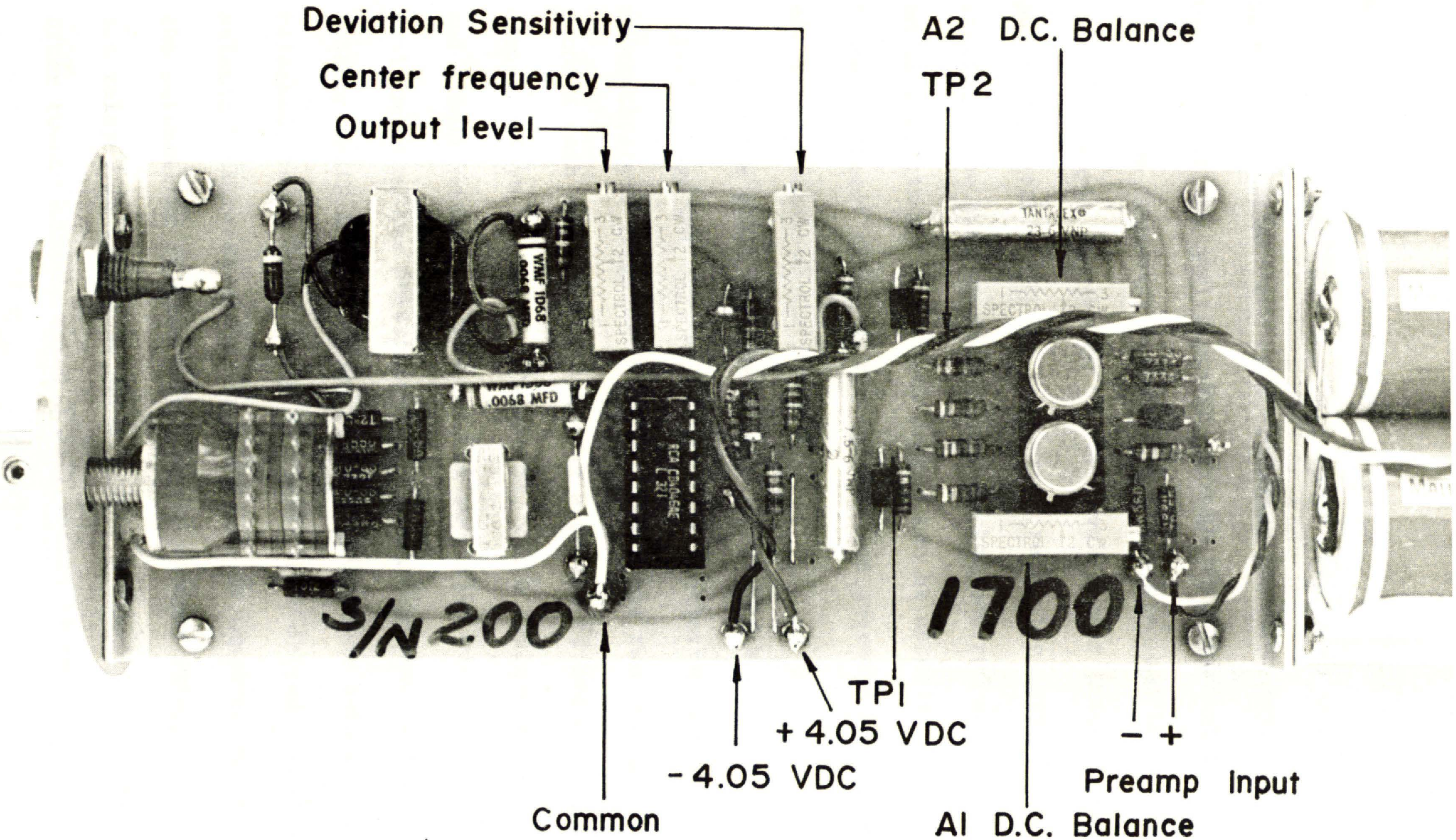


FIGURE 5

C-4 Calibrator

A. Operation

Once each day the calibrator (Figure 1) applys a known direct current step to the seismometer coil, releases it, then applys a DC voltage step to the input of the amplifier-VCO through the seismometer L-pad.

The frequency response of the system can be calculated from a digitized signal. Simple inspection of the Develocorder trace, however, will indicate polarity reversals in the telemetry, recording, and playback systems after stations have been installed and checked out and any gross changes in seismometer sensitivity or natural period can be detected by comparison with previous traces. "Dead" times in the calibration sequence will give a measure of the electronic noise of the system.

The clock portion (Figure 2) provides a square wave output with one negative edge per day, which triggers sequentially a chain of three one-shot multivibrators (Figures 3 and 4), the first two having periods of about eight seconds each and the third having a period of twenty seconds. Multivibrator 1 closes relays 1A and 1B (Figure 5), which applies a current to the seismometer and simultaneously terminates the amplifier with 5.6K ohms, the approximate resistance of the seismometer. The eight-second closure time allows the mass to stop oscillating. About three milliseconds before relays 1A and 1B are released, relay 2 is closed to insert a 20-db pad. This pad attenuates the seismic background noise, resulting in an improved signal-to-noise ratio for the seismometer release test. Eight seconds later relay 2 returns to normal and relay 3 is closed to apply a step voltage to the input of the amplifier-VCO. After twenty seconds relay 3 will return to normal operation for another 24 hours.

B. Power Supplies

Mercury batteries are used as a standard (1.35 volts) in the seismometer circuit and to power (5.4 volts) the clock and multivibrator circuits. These batteries are used mainly because of their high capacity and their stable voltage. Quiescent current drain is about 150 microamperes. Even in extremely cold temperatures, the mercury batteries provide enough power to operate the clock and multivibrator circuits for one year. A 9-volt alkaline transistor battery, used to close the relays, has both adequate shelf life and capacity to provide power for a year. Only fresh battery replacements should be used.

C. Testing

Two separate common connections are necessary: the seismometer signal common, and the case common which is connected to the relay control and relay ground. All tests are made using GND or case common (Figure 4).

1. Trigger test. Connect the seismometer to the proper terminals and make sure the S and T resistors are in place. Monitor the amplifier output MON with an oscilloscope or a recorder. Momentarily connect the Trigger terminal to GND and observe sequence illustrated in Figure 5.

2. Clock pulse. Referring to Figures 1 and 2, observe the 10.54-second period clock square wave.

3. Reset. Momentarily connect the Reset terminal to the +5V terminal. This will reset the CD4020AE integrated circuit only. To insure this component has been reset, perform the operation when the clock pulse is "high" (+5 volts). Reset operation will cause it to return to zero. Be sure to make a note of reset times for each calibrator, otherwise the 36-second calibration will be very difficult to locate over a 24-hour period.

D. Attenuation

Amplitudes of the seismometer release test and the step voltage amplifier input test are approximately the same at the amplifier output. The ATTEN resistor (Table I) can be varied to increase or decrease the desired amplitudes. In general, the ATTEN resistance versus VCO-preamplifier attenuation shown in the table can be used to provide usable data.

E. Seismometer L Pad

The calibrator will not operate without a seismometer L pad. Each seismometer will be supplied with its S and T resistors (Figure 5). If the VCO-preamplifier is changed at any station, be sure to transfer these resistors to the new equipment.

F. Clock

The oscillator frequency can be adjusted with C_1 (Figure 2) and monitoring pin 16 of the CD4045AE chip, using a 5-pf capacitor (or less) to minimize loading effects of the frequency counter. The crystal is not temperature compensated; stability is about 1.5 ppm/°C.

Table 1 -- Attenuator resistance values

Preamplifier Attenuation	Attenuator Resistance
0 Db	10 megohms
6	5.6 (")
12	3.0 (")
18	1.3 (")
24	560K
30	180K
36	0 ohms

PARTS LIST for C-4 CALIBRATOR

R1	15 meg ohm 1/4w 5%
R2	1k ohm 1/4w 5%
R3	2.2k ohm 1/4w 5%
R4	20k ohm 1/4w 5%
R5, R7, R14	200k ohm 1/4w 5%
R6, R8,	2 meg ohm 1/4w 5%
R9, R10, R16	27k ohm 1/4w 5%
R11, R13, R17	110 ohm 1/4w 5%
R12	300 ohm 1/4w 5%
R15	5.6 meg ohm 1/4w 5%
R18	91k ohm 1/4w 5%
R19, R20	5.6k ohm 1/4w 5%
R21	180 ohm 1/4w 5%
R22	9.1k ohm 1/4w 5%
R23	1.1k ohm 1/4w 5%
C1	15-60pf cap Erie 538-011F 15-60
C2	25pf cap Sprague 10TCC Q25 NPO
C3, C4, C8	4.7uf Components Inc. CCM 020 475-10
C5, C6, C7	.47uf Erie 8131 050 651 474M
C9	.22uf Erie 8131 050 651 224M

Q1 through Q6	2N3569
D1, D2, D3, D4	1N645
IC1	CD4045AE, RCA
IC2	CD4020AE, RCA
IC3	CD4049AE, RCA
RL1A, RL2, RL3	W118DIP 1, Magnecraft
RL1B	W107DIP 1, Magnecraft
CRYSTAL	Monitor Prod. 2243976824 MC-6C
SOCKETS	Amphenol 821250-11-164
TERMINALS	USECO 2003B
CONNECTORS	Winchester JF2S, JF2P

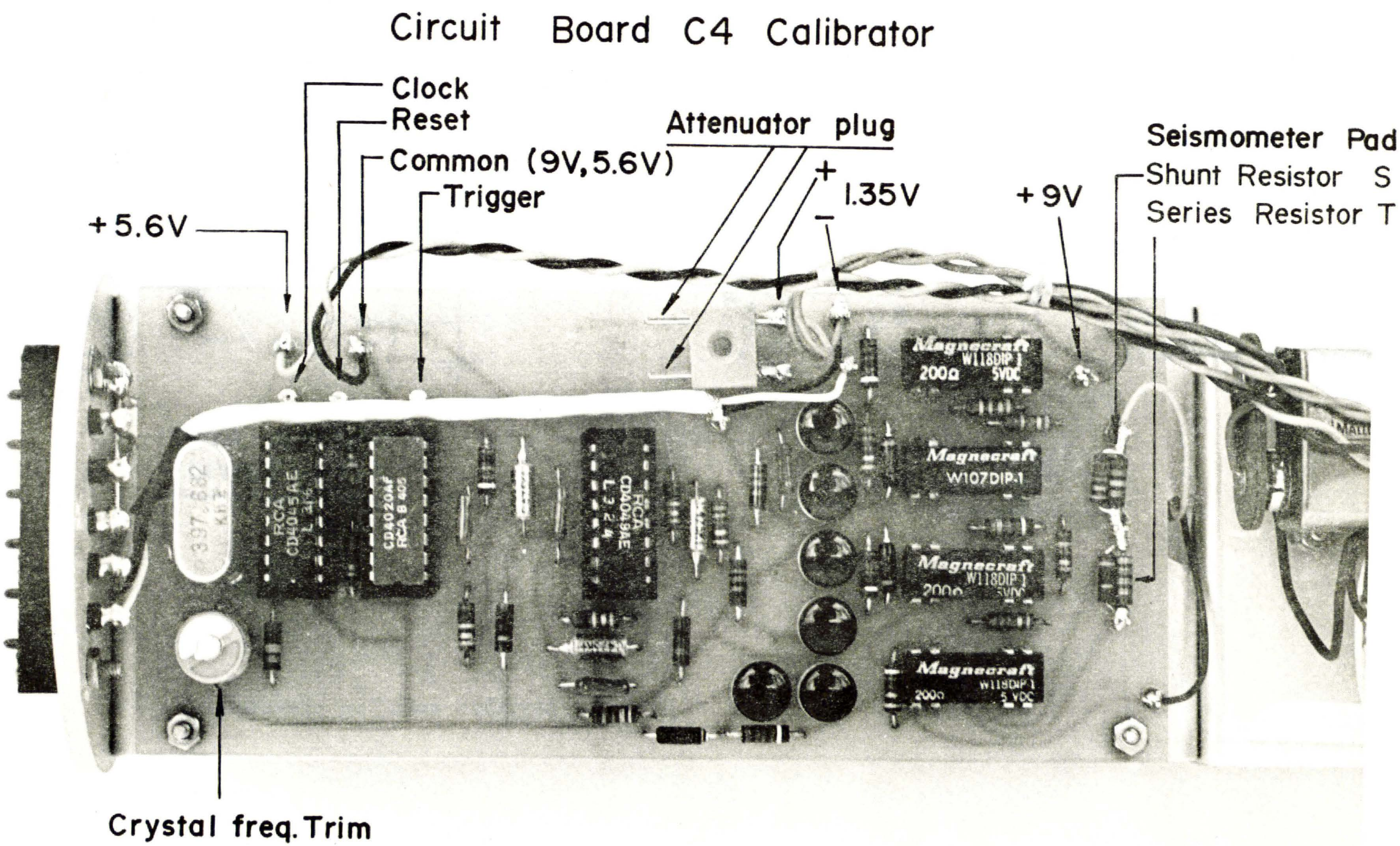

Circuit Board C4 Calibrator
Clock
Reset
Common (9V, 5.6V)
Trigger
+5.6V
Attenuator plug
+
1.35V
−
+9V
Seismometer Pad
Shunt Resistor S
Series Resistor T
Crystal freq. Trim
Magnecraft
W107DIP-1

FIGURE 1

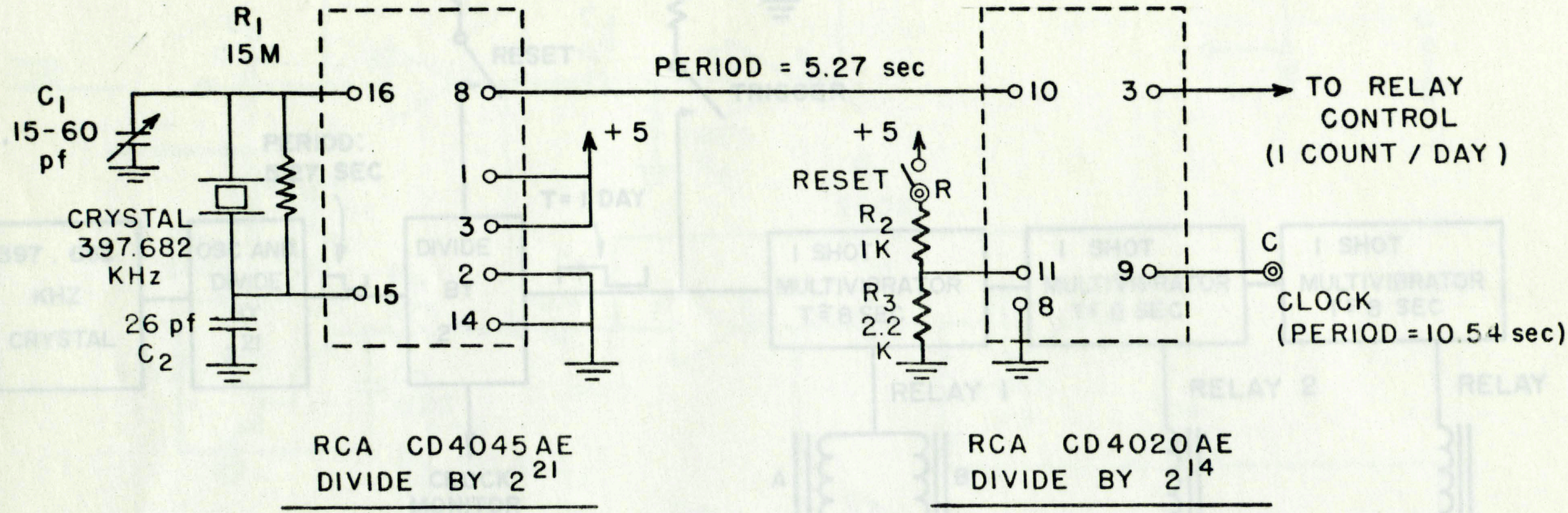


Figure 2. -- Clock circuit.

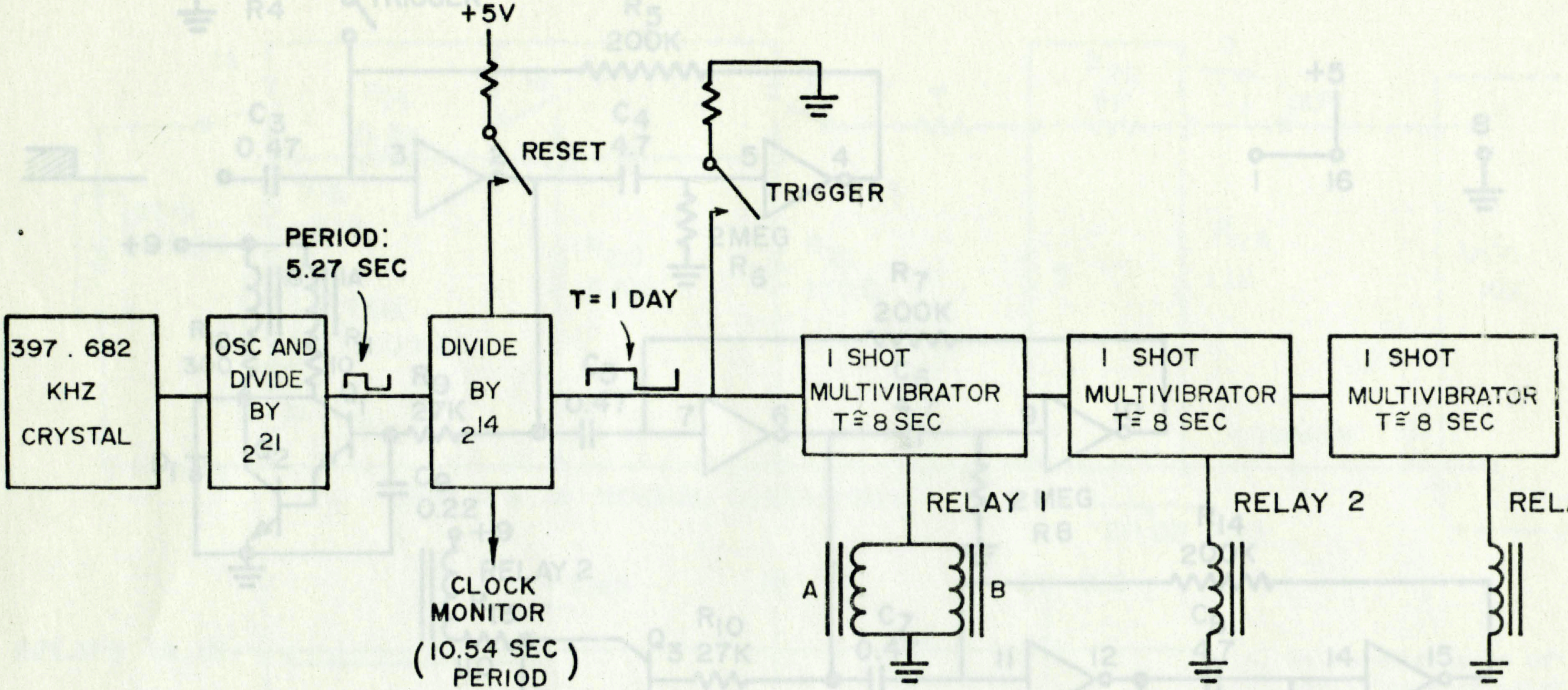


Figure 3. -- Block diagram of calibrator control circuit.

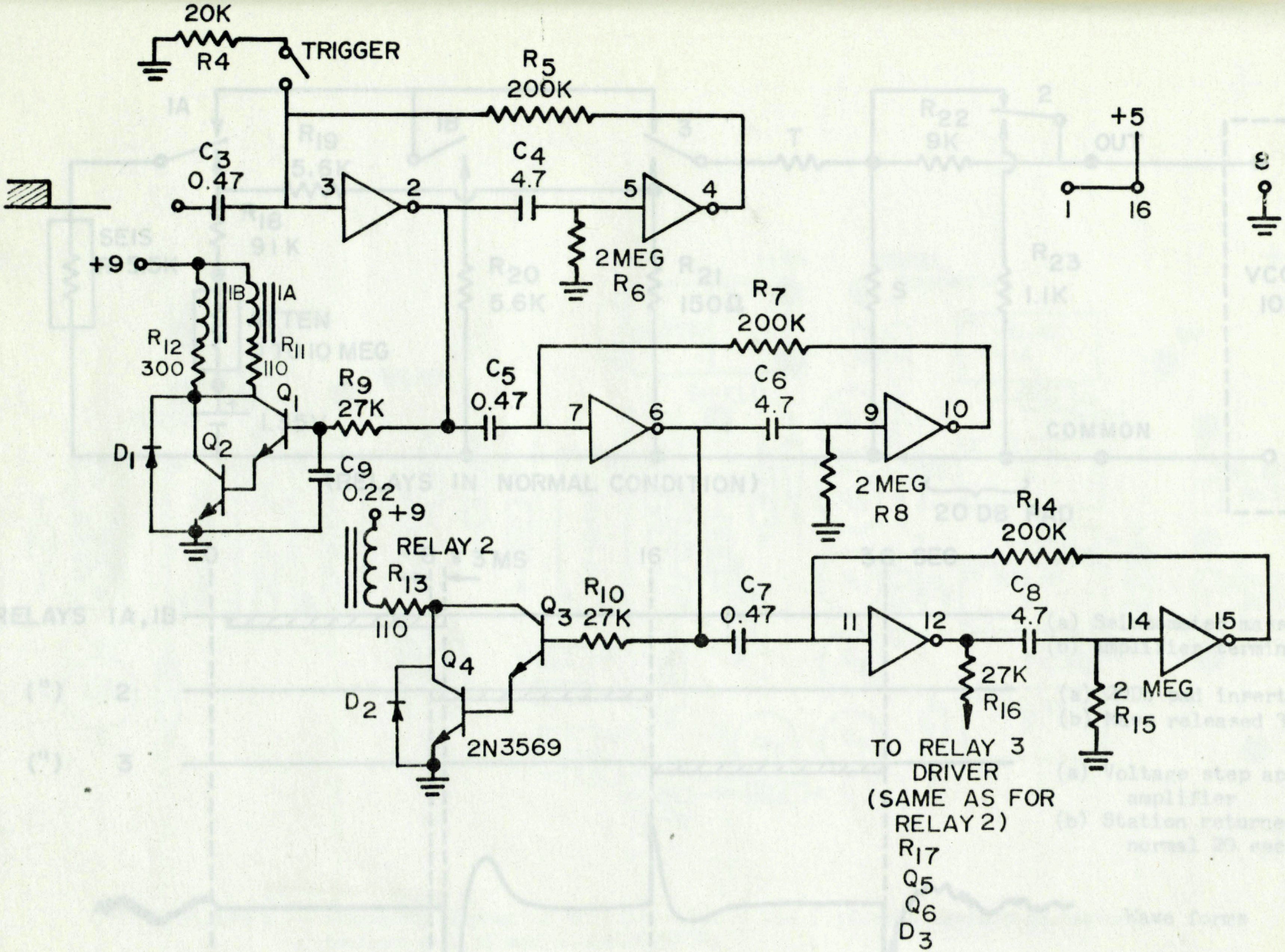


Figure 4. -- Schematic diagram of relay control circuits.

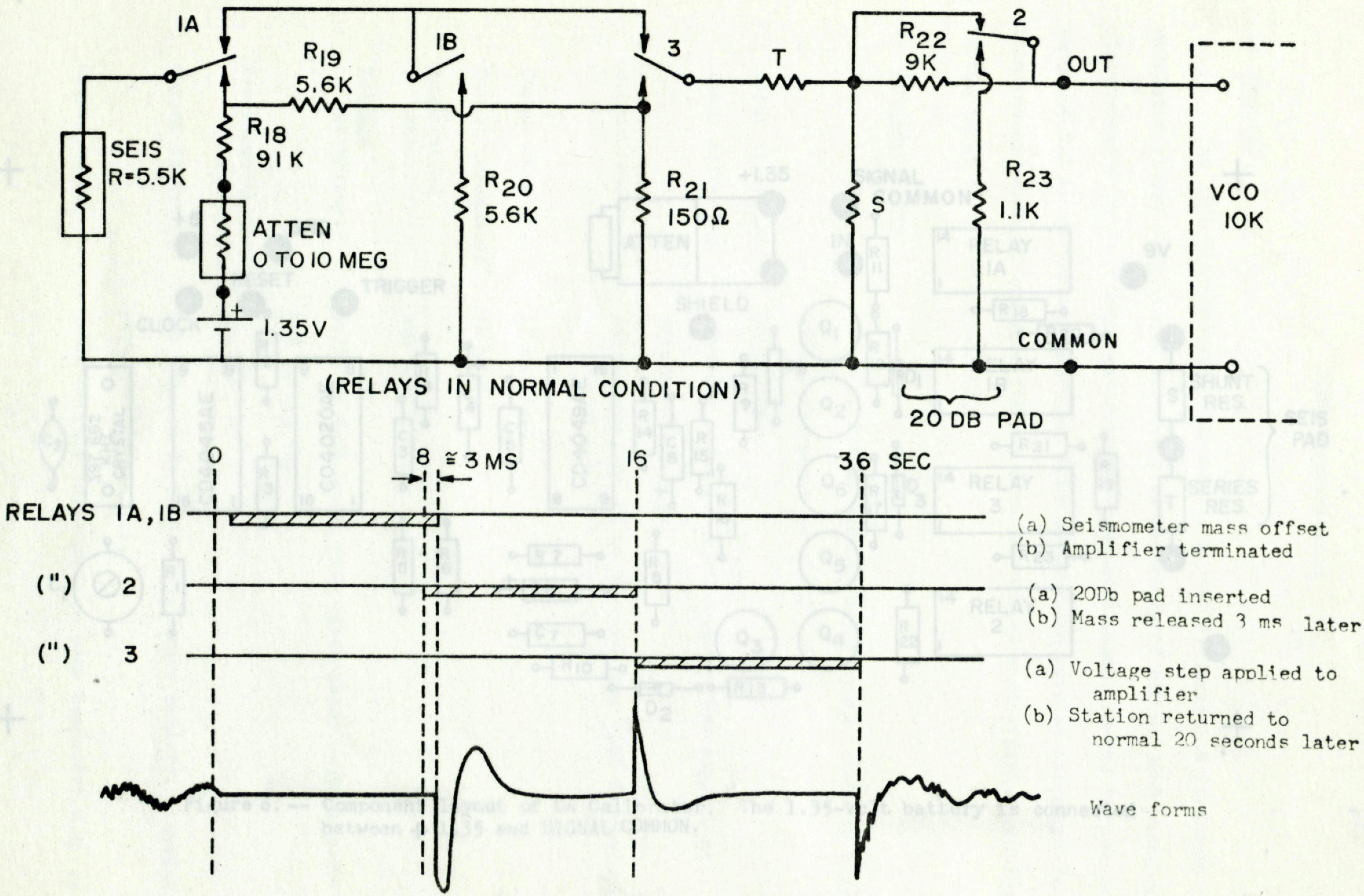


Figure 5. -- Seismometer and amplifier calibrating circuit

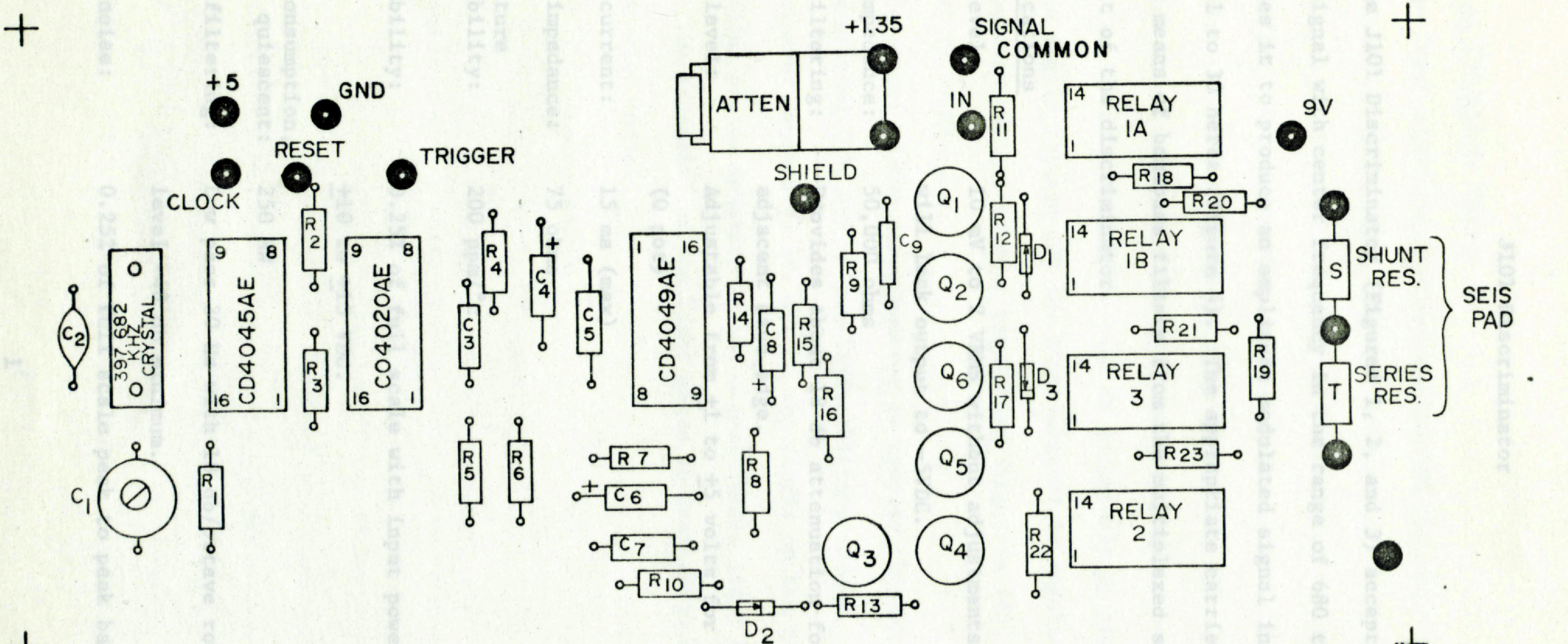


Figure 6. -- Component layout of C4 Calibrator. The 1.35-volt battery is connected between + 1.35 and SIGNAL COMMON.

J101 Discriminator

A. General

The J101 Discriminator (Figures 1, 2, and 3) accepts a frequency modulated signal with center frequency in the range of 680 to 3060 hertz and discriminates it to produce an amplitude modulated signal in the frequency range of 0.1 to 30 hertz (Figure 4). The appropriate carrier frequency is selected by means of bandpass filters from the multiplexed signal appearing at the input of the discriminator.

B. Specifications

Input level:	10 mV to 2 VRMS without adjustments. Loss of signal will lock output to -5VDC.
Input impedance:	50,000 ohms
Input filtering:	Provides about 18 db attenuation for signals at adjacent band edge.
Output level:	Adjustable from ±1 to ±5 volts for ±125 Hz deviation. (0 pot)
Output current:	15 ma (max)
Output impedance:	75 ohms
Temperature stability:	200 ppm/°c
Voltage stability:	0.25% of full scale with input power voltage between ±10 to ±15 VDC.
Power consumption, quiescent:	250 MW
Output filtering:	Low pass 30 Hz with 18 db/octave rolloff. Carrier level -48 db minimum.
Output noise:	0.25% of full scale peak to peak bandwidth D.C. to 30 Hz.

C. Theory of Operation (Figure 5)

The input signal is transformer-coupled through a two-stage active bandpass filter (amplifier IC1, IC2) and into a phase-locked-loop discriminator IC3. The output of the discriminator is filtered and amplified by an operational amplifier (IC4) and direct coupled to the output. The filtered carrier signal is also fed into a threshold detector circuit (Q2, Q3) that will lock the amplifier to -5 volts when the input carrier level drops below a predetermined level. This threshold level is adjustable by potentiometer, R1.

The supply voltage for the discriminator is regulated to within ±5% by two integrated circuit circuit regulators (negative IC6, positive IC5) on the board at ±7 volts.

The output of the discriminator is coupled through two diodes (D3, D4) and two transistors (Q5, Q6) to two light-emitting diodes. When the output of the discriminator exceeds ±0.5V, one of the diodes on the front panel will light depending on the polarity of the signal (upper light is plus, lower light is minus). The intensity of the light gives an indication of the DC offset of the discriminator output.

D. Alignment of Discriminator

1) Adjustment of free-running multivibrator

Monitor the frequency of the square wave between pins 4 and 5 (shorted) of integrated circuit IC3 and ground. Substituting a resistance decade box for resistor Rcf (Figure 6), adjust resistance until the desired center frequency is reached. The precise resistance of the decade box should be measured with a digital ohmmeter and a quarter-watt, carbon resistor of this value used for Rcf.

2) Alignment of bandpass filter

The bandpass filter consists of two 741 operational amplifiers used as active filters. The first stage (Figure 5) determines the amplitude and cut-off frequency of the upper band edge, and the second stage determines the amplitude and cut-off frequency of the lower band edge. Three resistors in each stage determine the frequency and amplitude characteristics of the filter.

The following procedure is used in determining the values of these resistors:

1. Using the values of R1, R2, and R3 in Table I, connect a resistance decade box in parallel with RA2 and a second decade box in parallel with RB2.
2. Connect a signal generator to the discriminator input (Pins A and B, Figure 1) and a db meter between the "F" pin on the front panel and ground.
3. Set the generator to the desired center frequency and adjust its level for a 0 db output at the "F" pin jack.

4. Set the signal generator frequency to the upper band edge (center frequency + 125 Hz) and adjust the decade resistance in the first 741 stage so the signal level monitored at "F" is -3 to -5 db. Repeat Step 3).

5. Set the generator frequency to the lower band edge (center frequency -125 Hz) and adjust the decade resistance in the second 741 stage so the signal level monitored at "F" is -3 to -5 db. Repeat Step 3).

6. Repeat Steps 4 and 5 to get desired results (Table I). Install quarter-watt, carbon resistors of the proper value in place of the decade boxes.

These discriminators have also been used with center frequencies of 300, 400, and 500 Hz and deviations of $\pm$25 Hz.

C. Adjustment of Zero, Upper, and Lower Output Levels

The discriminator output should be zero when the input signal frequency equals the discriminator center frequency. This adjustment is made using R34 (Figure 5) which is mounted on the front panel and marked "Z" (Zero). Maximum and minimum output voltage levels obtained at upper and lower band edges respectively, are adjusted with R33 which is mounted on the front panel and indicated "O" (Output). Adjustments are made as follows:

1) Connect a signal generator and a db meter to the discriminator input (Pins A and B, Figure 5), and a frequency counter to pin jack "F". Adjust the generator to the desired center frequency. Monitoring the pin jack "O" with a digital voltmeter, adjust "Z" for a voltage null. Reset the signal generator to the lower band edge and set potentiometer "O" for an output of -2 VDC. If the

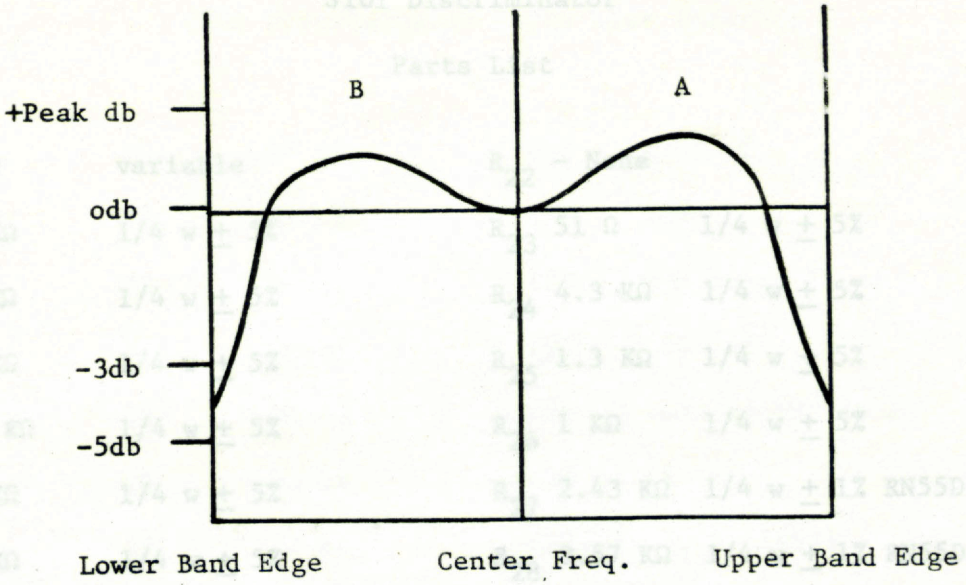
adjustments have been made correctly a sweep through the frequency range corresponding to the lower band edge, center frequency, and upper band edge will result in an output of -2 VDC, 0 VDC, and +2 VDC respectively.

D. Carrier Threshold Level Adjustment

The discriminator should operate with input signal levels as low as -30 db. For weaker signals, or loss of signal, the output will be locked to -5 VDC. The level adjustment potentiometer, R1, is mounted on the printed circuit board (Figure 6) and is adjusted as follows:

1) With the test setup used in C-1, set the signal generator frequency to the upper band edge and the signal level to the desired threshold level. The output monitor, pin jack "O", will indicate +2 VDC (Section C).

2) Reduce the signal generator level by 2 db. The output should drop to -5 VDC if properly adjusted; if not, readjust R1.



Channel			B			A			Freq. Determining Resistors (ohms)		
Number	Cf Hz	Band Width ± Hz	Peak +db	Freq. Hz	Band Edge -db	Peak +db	Freq. Hz	Band Edge -db	RA1 RB1 Ohms	RA2 RB2 Ohms	RA3 RB3 Ohms
AD	300	25	.5	286	4	.5	311	4	20K	1500	2.0 meg
BD	400	25	.3	388	4	.2	410	4	16K	1100	1.6 meg
CD	500	25	.2	491	4	.2	510	4	13K	910	1.3 meg
BA	400	75	-.5	365	4	1	427	4	4.7K	200K	470K
1	680	125	-.5	602	3.5	1	734	3.5	3K	9100	300K
2	1020	125	-.2	955	4	1	1070	4	3K	2000	300K
3	1360	125	-.5	1310	3.5	.5	1401	3.5	2.4K	1000	240K
4	1700	125	1	1640	4.5	1	1760	4	3.6K	300	360K
5	2040	125	.5	1980	4	1	2090	4	3.0K	240	300K
6	2380	125	.5	2317	4	1	2430	3	2.7K	200	270K
7	2720	125	-0.5	2645	3.5	.5	2779	3.5	2.4K	150	240K
8	3060	125	-1.5	2973	3.5	.5	3105	3.5	2.2K	130	220K

C23, .047uf channels BA-5, .022 uf channels 6-8

Rcf, selected for each IC-3, approximately 13K for Ch 1, 2K for Ch 8

Table I Bandpass Filter characteristics and values

J101 Discriminator

Parts List

R_1	5 KΩ	variable
R_2	91 KΩ	1/4 w ± 5%
R_3	1 KΩ	1/4 w ± 5%
R_4	10 KΩ	1/4 w ± 5%
R_5	5.6 KΩ	1/4 w ± 5%
R_6	56 KΩ	1/4 w ± 5%
R_7	15 KΩ	1/4 w ± 5%
R_8	820 Ω	1/4 w ± 5%
R_9	9.1 KΩ	1/4 w ± 5%
R_{10}	390 KΩ	1/4 w ± 5%
R_{11}	9.1 KΩ	1/4 w ± 5%
R_{12}	27 KΩ	1/4 w ± 5%
R_{13}	240 KΩ	1/4 w ± 5%
R_{14}	10 Ω	1/4 w ± 5%
R_{15}	2.43 KΩ	1/4 w ± 1% RN55D
R_{16}	7.5 KΩ	1/4 w ± 1% RN55D
R_{17}	5.6 KΩ	1/4 w ± 5%
R_{18}	5.6 KΩ	1/4 w ± 5%
R_{19}	680 Ω	1/4 w ± 5%
R_{20}	8.25 KΩ	1/4 w ± 1% RN55D
R_{21}	30 KΩ	1/4 w ± 5%
R_{22}	- None	
R_{23}	51 Ω	1/4 w ± 5%
R_{24}	4.3 KΩ	1/4 w ± 5%
R_{25}	1.3 KΩ	1/4 w ± 5%
R_{26}	1 KΩ	1/4 w ± 5%
R_{27}	2.43 KΩ	1/4 w ± 1% RN55D
R_{28}	3.57 KΩ	1/4 w ± 1% RN55D
R_{29}	10 Ω	1/4 w ± 5%
R_{30}	5.11 KΩ	1/4 w ± 1% RN55D
R_{31}	10 KΩ	1/4 w ± 5%
R_{32}	10 KΩ	1/4 w ± 5%

Rcf, RA_1, RA_2, RA_3, RB_1, RB_2, RB_3 — Frequency dependent components. See Table I

R_{33}	200 KΩ	Bourns Panel Mount Pot 272L
R_{34}	50 KΩ	Bourns Panel Mount Pot 272L

J101 Discriminator Parts List (cont'd)

C1	.22 uf	C21	.047 uf
C2	.01 uf	C22	none
C3	.01 uf	C23	See Table I
C4	.01 uf	C24	.22 uf
C5	.01 uf	C25	.033 uf WMF 1S33
C6	.22 uf	C26	15 uf
C7	.22 uf	CR1, 2, 3, 4	1N914
C8	4.7 uf	CR 5, 6	Sprague ED123 LED
C9	.47 uf		
C10	15 uf	Q1, Q4, Q6,	2N3711
C11	15 uf	Q2	2N3391
C12	15 uf	Q3	2N2484
C13	15 uf	Q5	2N3702
C14	15 uf	T1	UTC SSO-2
C15	15 uf	IC1, IC2, IC4,	LM741CH
C16	.22 uf	IC3	LM565CH
C17	100 uf	IC5	LM305H
C18	.0015 uf	IC6	LM304H
C19	.1 uf		
C20	.1 uf		

Front Panel J101 Discriminator

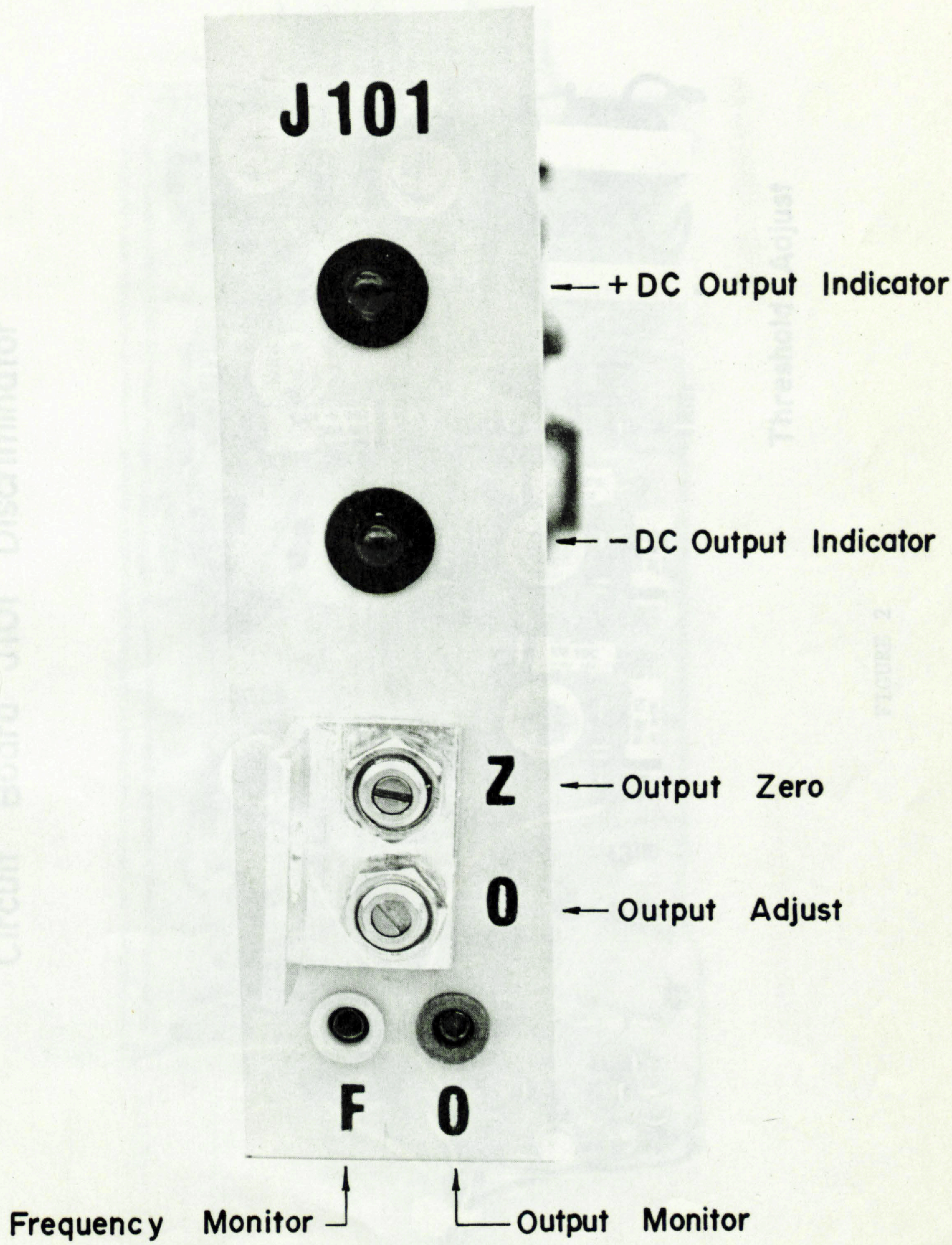


FIGURE 1

Circuit Board J101 Discriminator

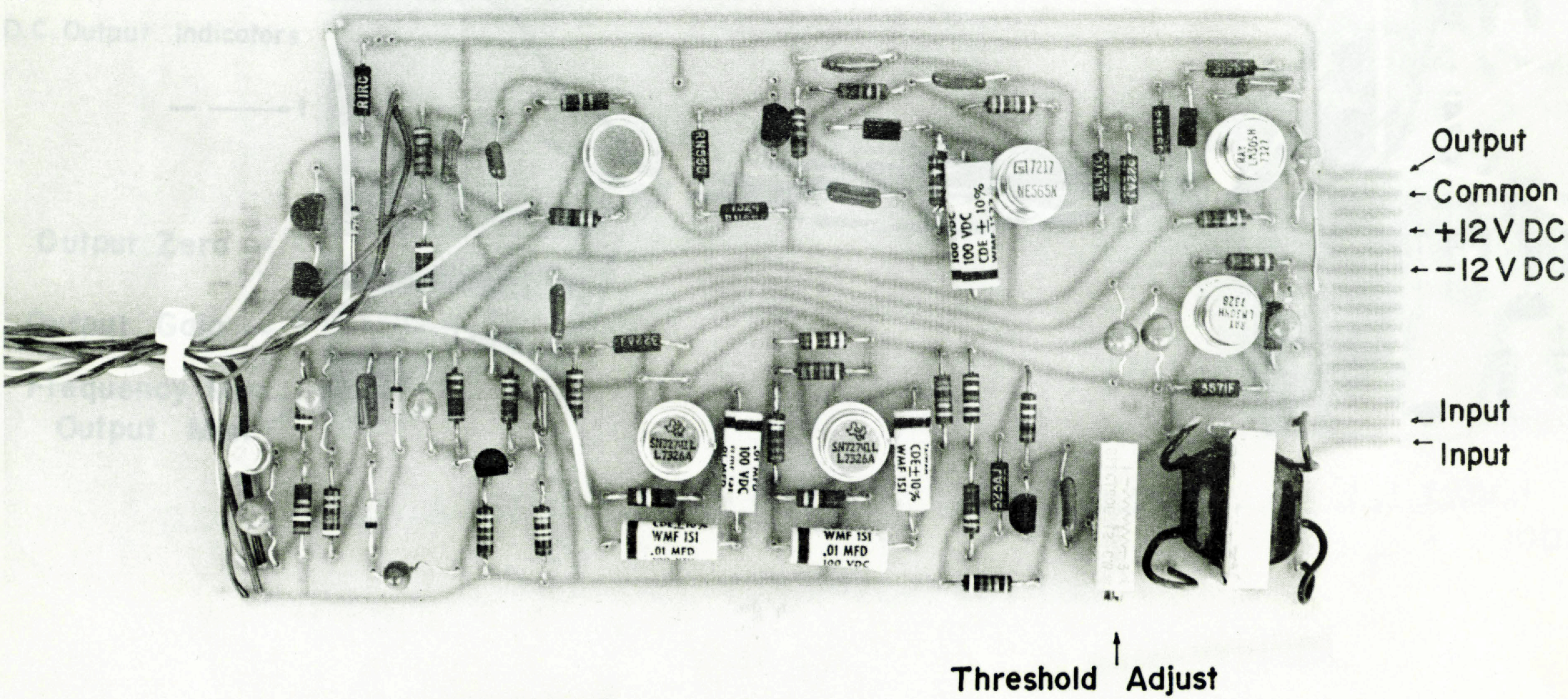


FIGURE 2

Circuit Board J1O1 Discriminator

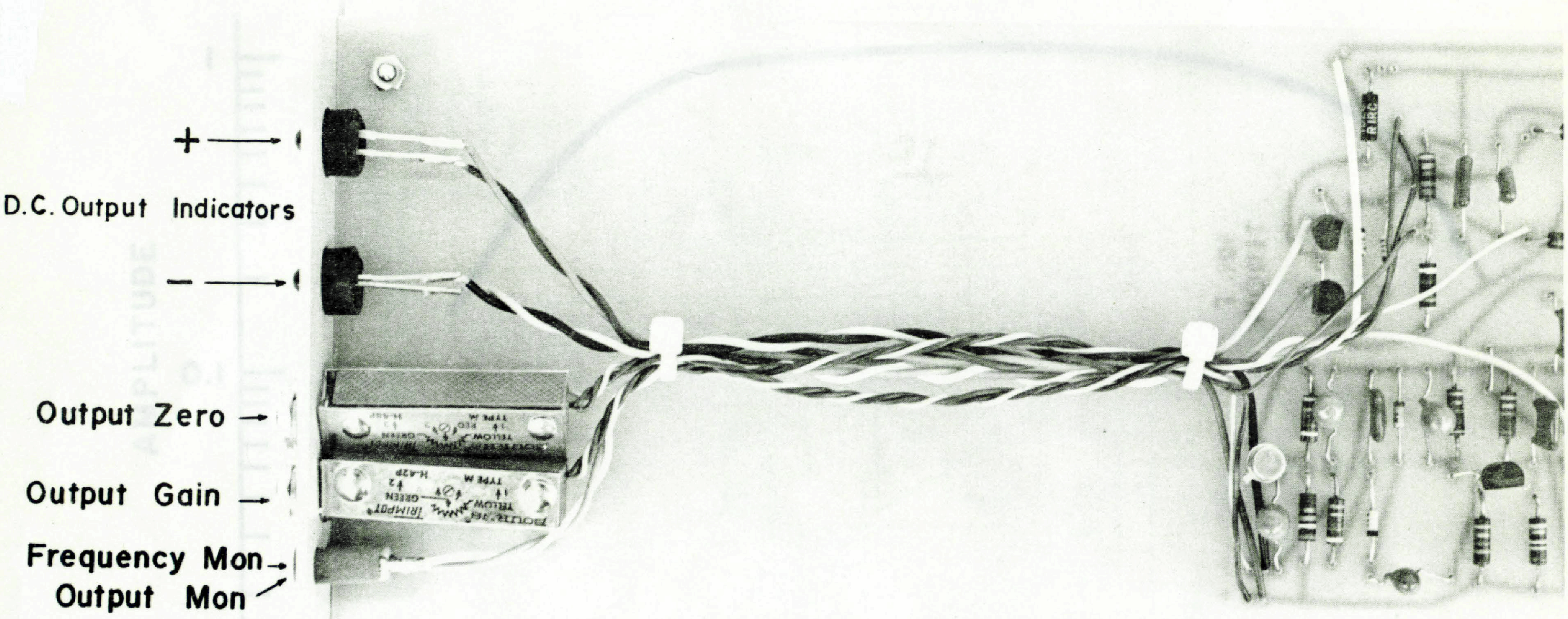


FIGURE 3

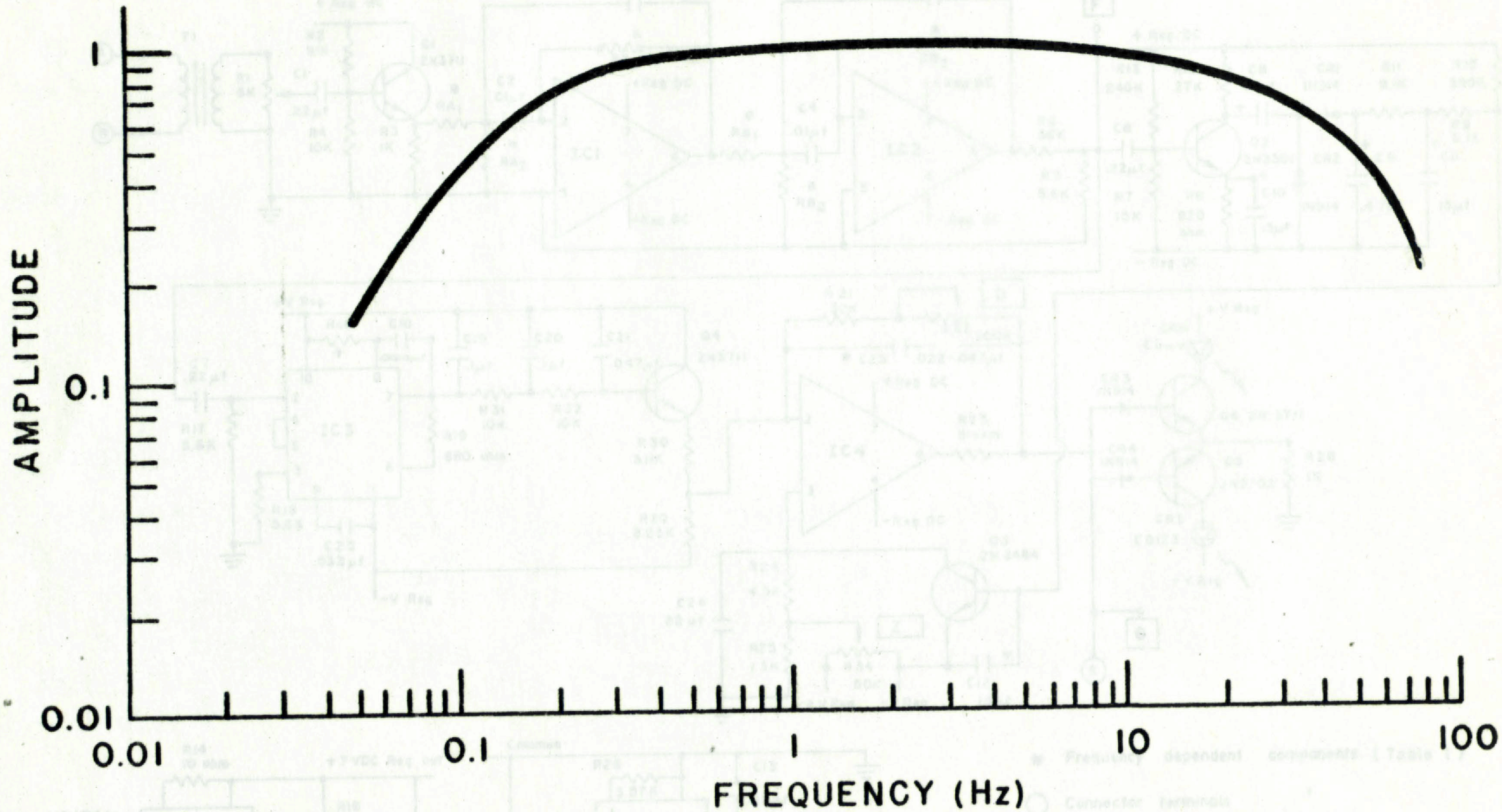
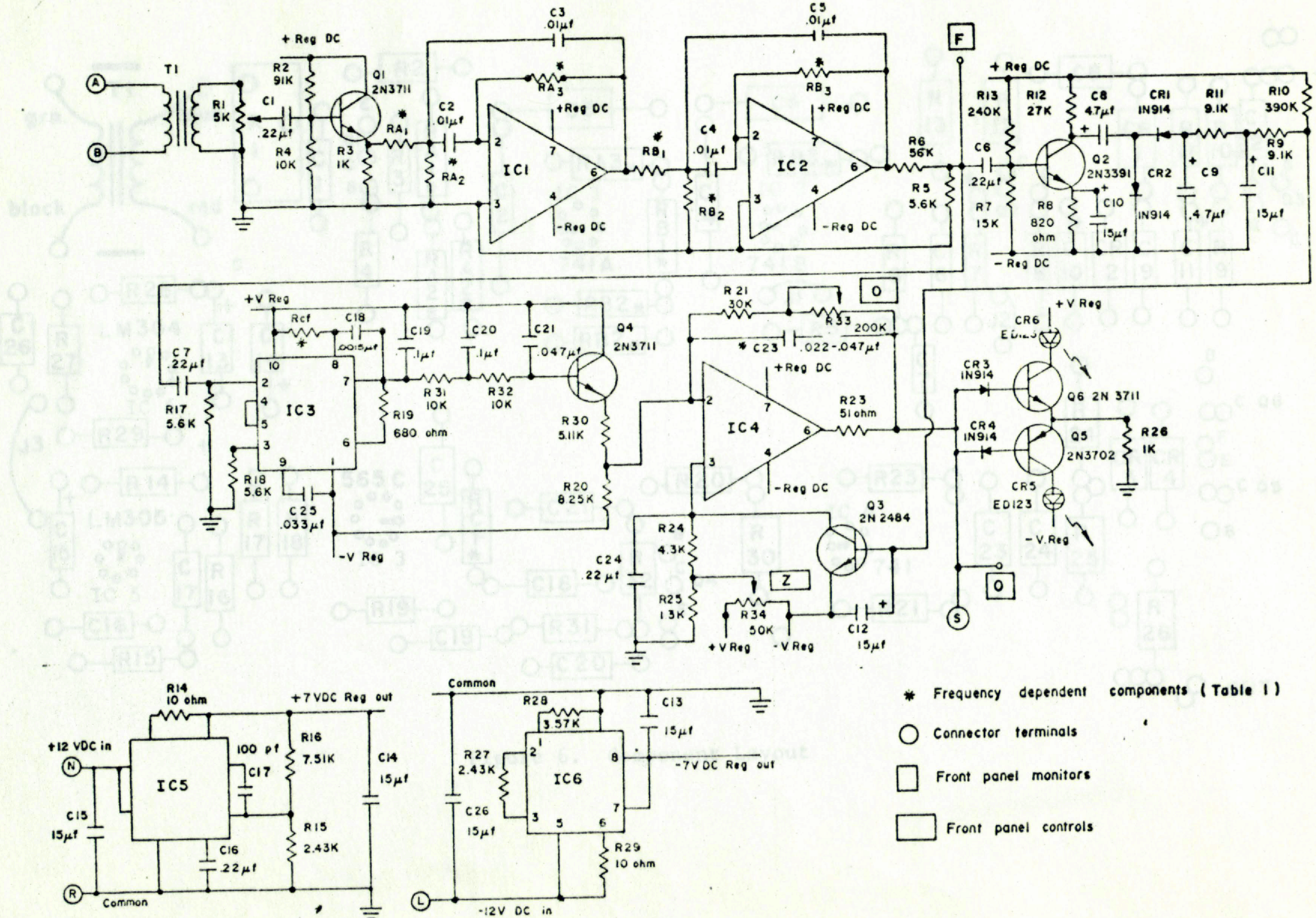


Figure 4. Combined frequency response of J302 Preamplifier/VCO and J101 Discriminator.

Figure 5. J101 Discriminator Schematic Diagram



J 101 Discriminator

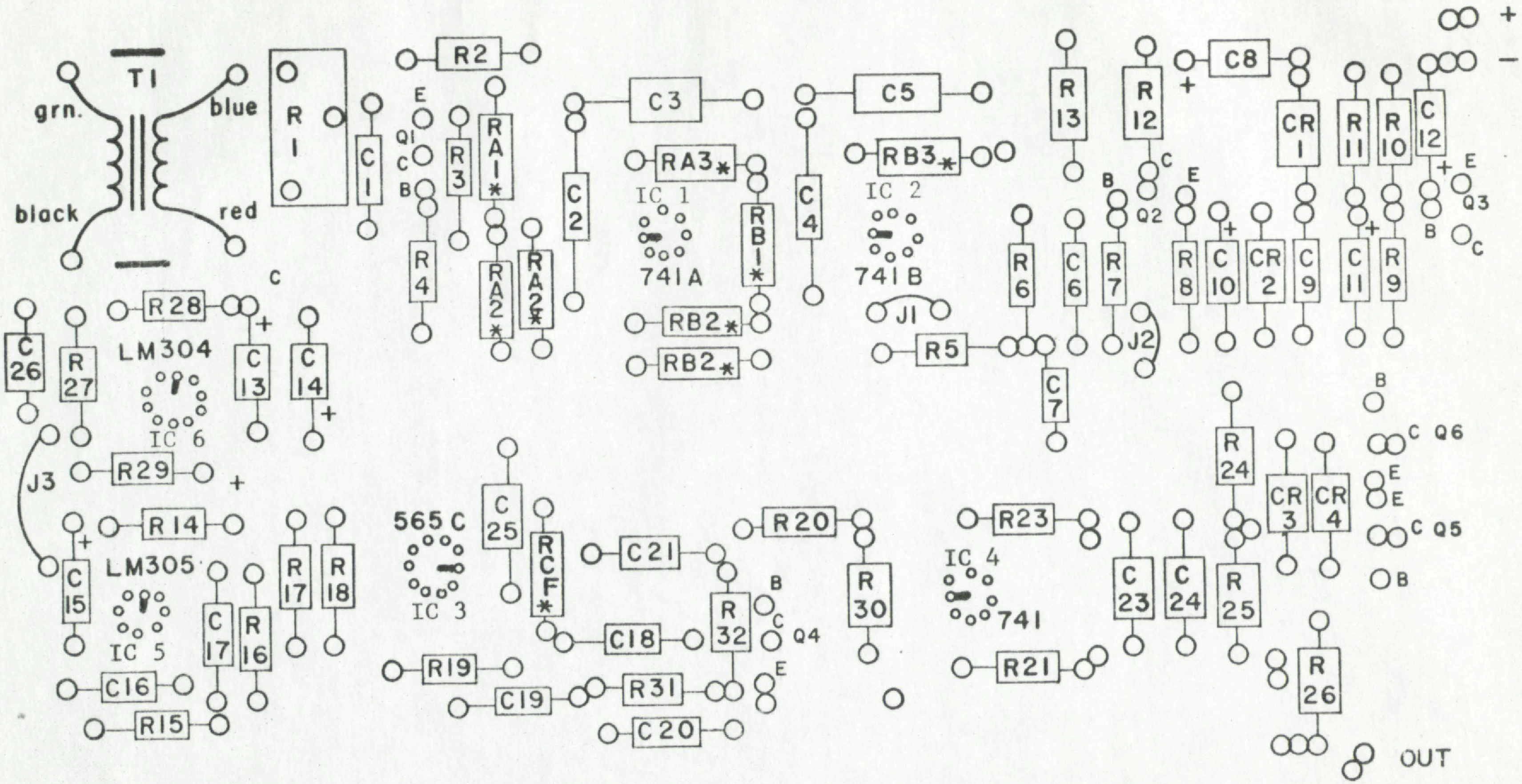


Figure 6. Component Layout