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TSUNAMI MICROPROCESSOR TIDE SYSTEM

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TM

Open-File Report 78-95

Table of Contents

List of Figures

ABBREVIATIONS USED

ACC	Accumulator
ALU	Arithmetic logic unit
ASCII	American Standard Code for Information Interchange
ASL	Albuquerque Seismological Laboratory
CR	Carriage return
CHAR	Character
CHIP	Integrated semiconductor package
CMOS	Complementary metal oxide semiconductor
CRLF	Carriage return line feed
CPU	Central processing unit
EOT	End of transmission
EPROM	Erasable programmable read only memory
GOES	Geostationary Orbiting Environmental Satellite
HEX	Hexidecimal
I/O	Input output
Ld	Load
LF	Line feed
MS	Millisecond
"N"	Number of skipped tide words
N	No decision for logic chart
NOAA	National Oceanic and Atmospheric Administration
PROM	Programmable read only memory
P_1	Parity bit 1
P_2	Parity bit 2
P_3	Parity bit 3
P_4	Parity bit 4

RAM	Random access memory
ROM	Read only memory
T DATA	Tide data
TTL	Transistor transistor logic
T WORD	Tide word pointer for address location
T* WORD	Tide word pointer for transmitted tide word
U.S.	United States
USASCII	United States American Standard Code for Information Interchange
USGS	United States Geological Survey
XCH	Exchange
X_1	Accumulator bit 1
X_2	Accumulator bit 2
X_3	Accumulator bit 4
X_4	Accumulator bit 8
Y	Yes decision for logic chart

ABSTRACT

A Tsunami Microprocessor Tide System was developed to replace the Advanced Tsunami Tide System. The use of microprocessor based systems will reduce manpower and hardware costs from $4,000 per advanced system to $400 per microprocessor system. In addition to the cost reduction; the capacity, capability, and flexibility of the microprocessor systems were increased over the conventional systems. The microprocessor system can store up to 80 tide words as compared to 40 for the original systems. The microprocessor system can easily change data output formats from 11-bit ASCII to 8-bit ASCII codes, change tide sensors from float sensors to either crystal or bubbler sensors, and change other desired commands such as end of transmission (EOT) commands by simple software modifications.

The new Tsunami Microprocessor Tide System is programmed to operate in an "Interrogate" mode over the GOES Satellite Network. The Tsunami Microprocessor Tide System was developed for use in the Tsunami Warning Network. This system could be used in any water level measuring system because with simple software changes it could operate over standard radio link telemetry systems or over dial-up telephone circuit.

INTRODUCTION

As part of a continuing joint effort by the National Oceanic and Atmospheric Administration (NOAA) and the U. S. Geological Survey (USGS) to evaluate and develop new electronic techniques and systems for possible future use in a Tsunami Warning Network, the Albuquerque Seismological Laboratory (ASL) designed, developed, and assembled a microprocessor based water measuring data system. This new microprocessor based system is called the Tsunami Microprocessor Tide System and is shown in Figures 1, 2, and 3. This new microprocessor system was designed to replace the Advanced Tsunami Tide System which utilizes conventional electronic integrated circuit systems. The Advanced Tsunami Tide System is described in the USGS Open-File Report 76-735, titled "Tsunami Tide System."

Microprocessors are the latest technological advancement in electronic systems. Microprocessor systems will reduce the required manpower and electronic parts costs by 60 to 90 percent as compared to conventional integrated circuit systems. Other than input, output, and power wiring, all other wiring is accomplished by the printed circuit boards and the software instructions. The conventional wiring is replaced by software instructions and commands. Because of the ease of program changes and the flexibility of microprocessors, major system changes or modifications are quickly and easily altered by simple software instructions. The program instructions can be stored in non-volatile erasable programmable read only memories (EPROM's). These EPROM's can be erased by exposure to strong ultra-violet light and can be reused again when reprogrammed.

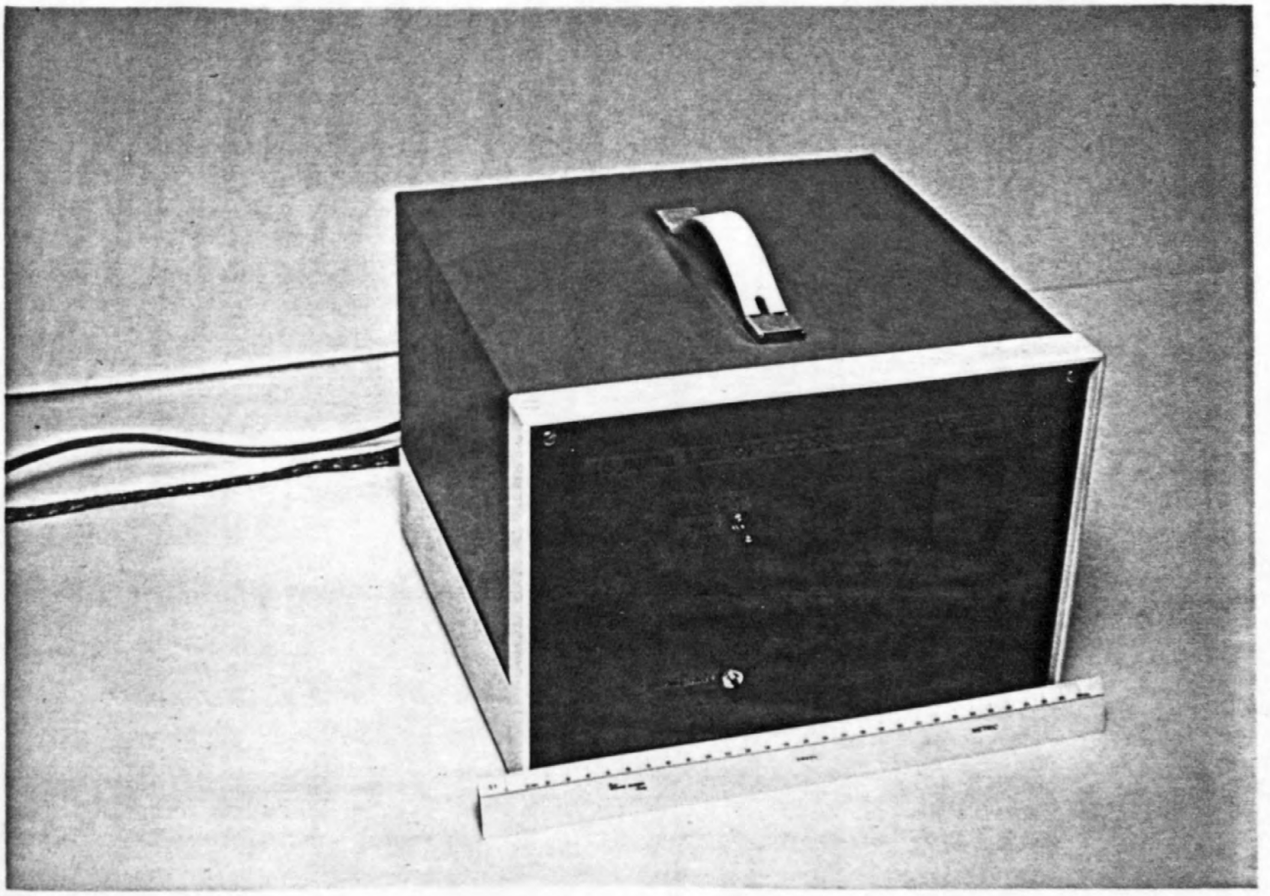

Figure 1. Front View of Tsunami Microprocessor Tide System

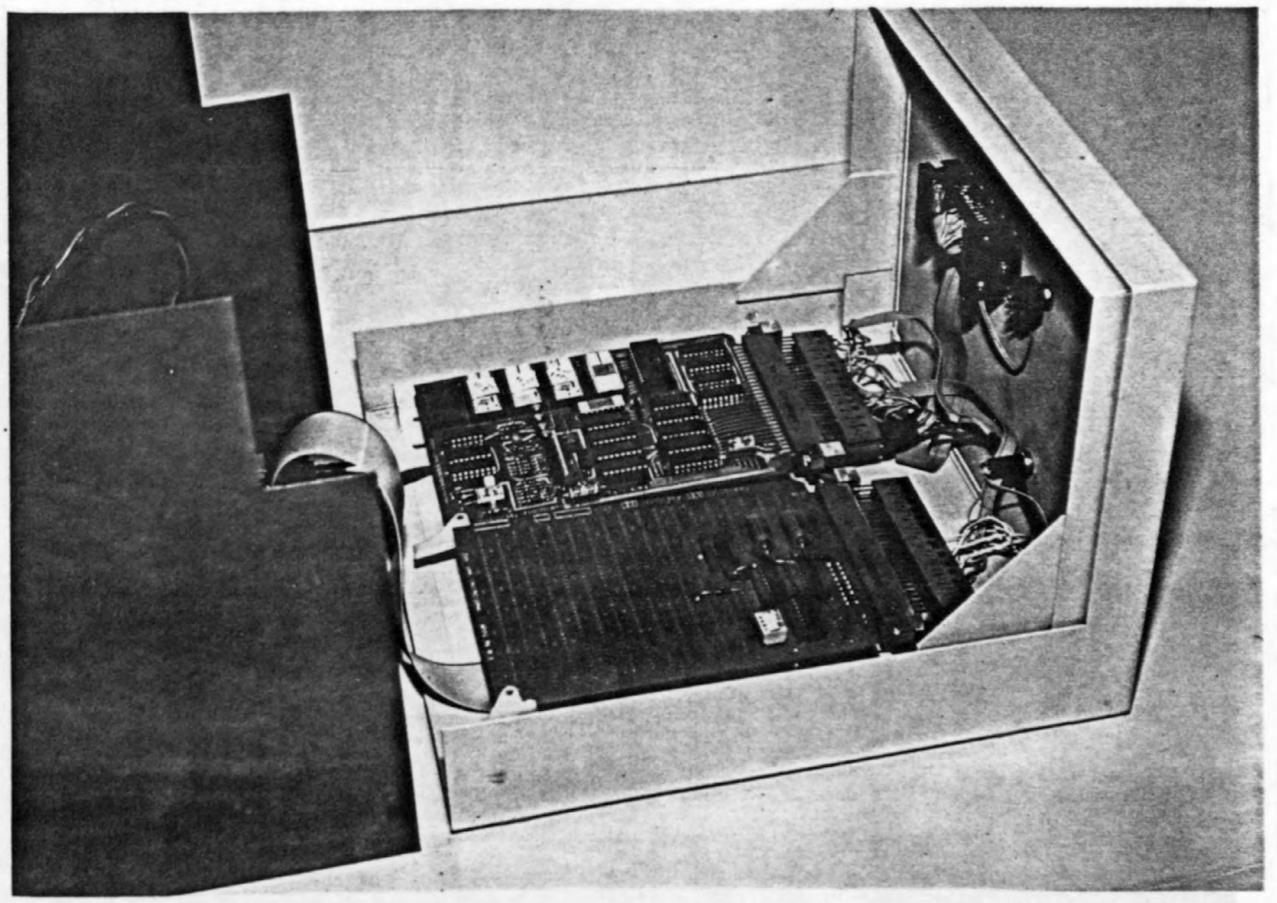

Figure 2. Inside View of Tsunami Microprocessor Tide System

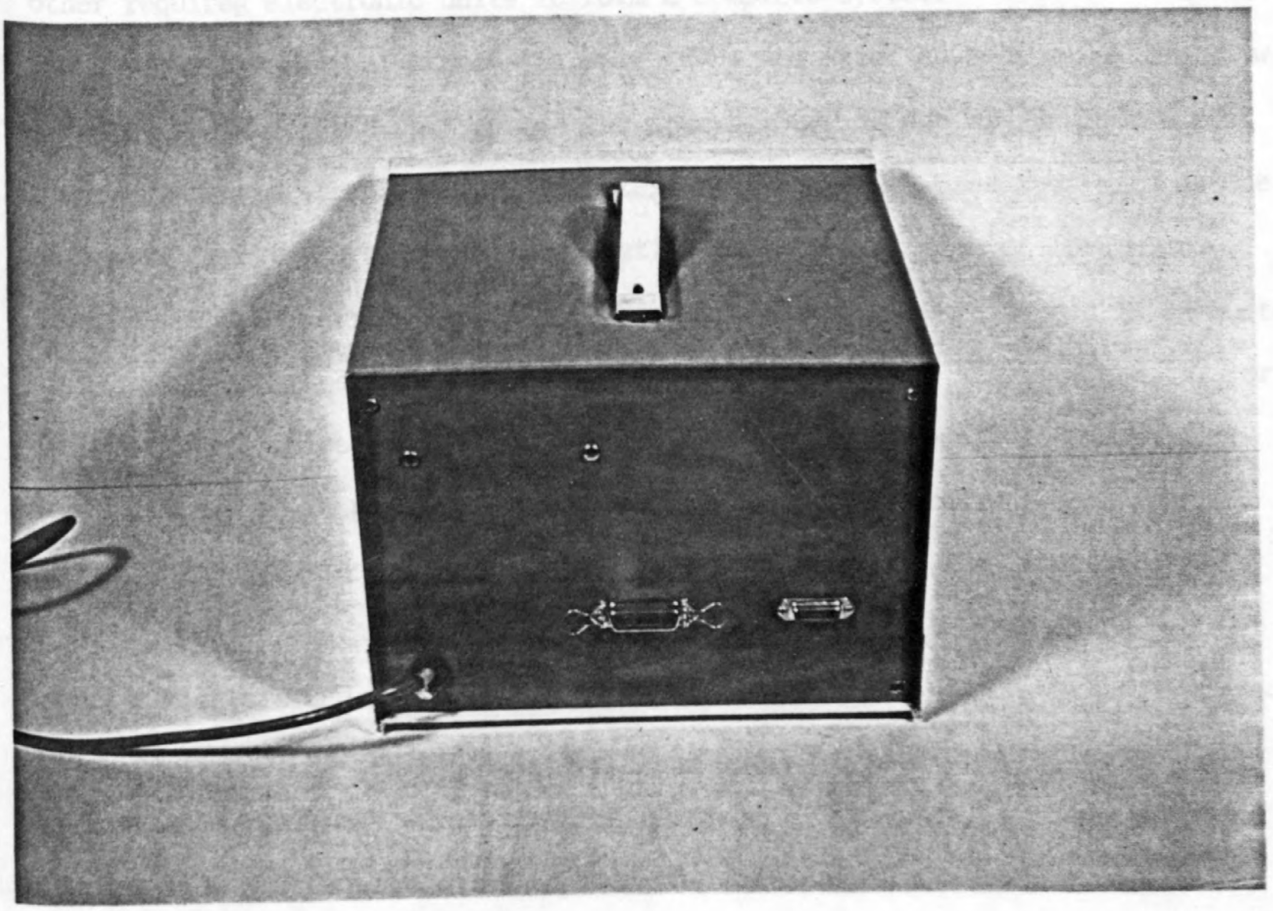

Figure 3. Rear View of Tsuami Microprocessor Tide System

It is possible to use programmable read only memories (PROM's) or read only memories (ROM's) in substitution for the EPROM's for lower cost and power consumption if desired. PROM's and ROM's are generally not reusable or erasable, but they operate the same as EPROM's in the storage of the system program.

A single board microprocessor system was selected for the tide system application. A single board microprocessor contains all the required electronic units and components to be a self-contained operational microprocessor. This single board system has the required clock, central processing unit (CPU), random access memories (RAM's), input/output ports, control units, EPROM's and other required electronic units to form a complete system.

A four bit Central Processing Unit (CPU) was selected because of the slow speed of the tide data and because the four bit CPU is one of the lowest cost microprocessor systems. The microprocessor architecture uses four bits as one data word or byte throughout its operation at a typical time of 10.8 micro-seconds per instruction execution. This word size and system speed is adequate for the tide systems. The operation of a four bit CPU is similar to 8, 12, or 16 bit CPU's. These other CPU's use more bits simultaneously as one word or instruction. It is possible to do 32 bit arithmetic operations on a four bit CPU by doing a series of four bit partial calculations. This would require more CPU operations and time, but if time is not critical there is no problem in using a four bit CPU.

The Tsunami Microprocessor Tide System performs the tide meter readings, data storage, and GOES Satellite transmission in the same way as the Advanced Tsunami Tide System with the exception that the data transmission is in an 8 bit ASCII format, with an end of transmission (EOT) character at the completion of transmission. The GOES interrogated data collection platform set is shown in Figure 4, and the GOES Radio Set Antenna is shown in Figure 5.

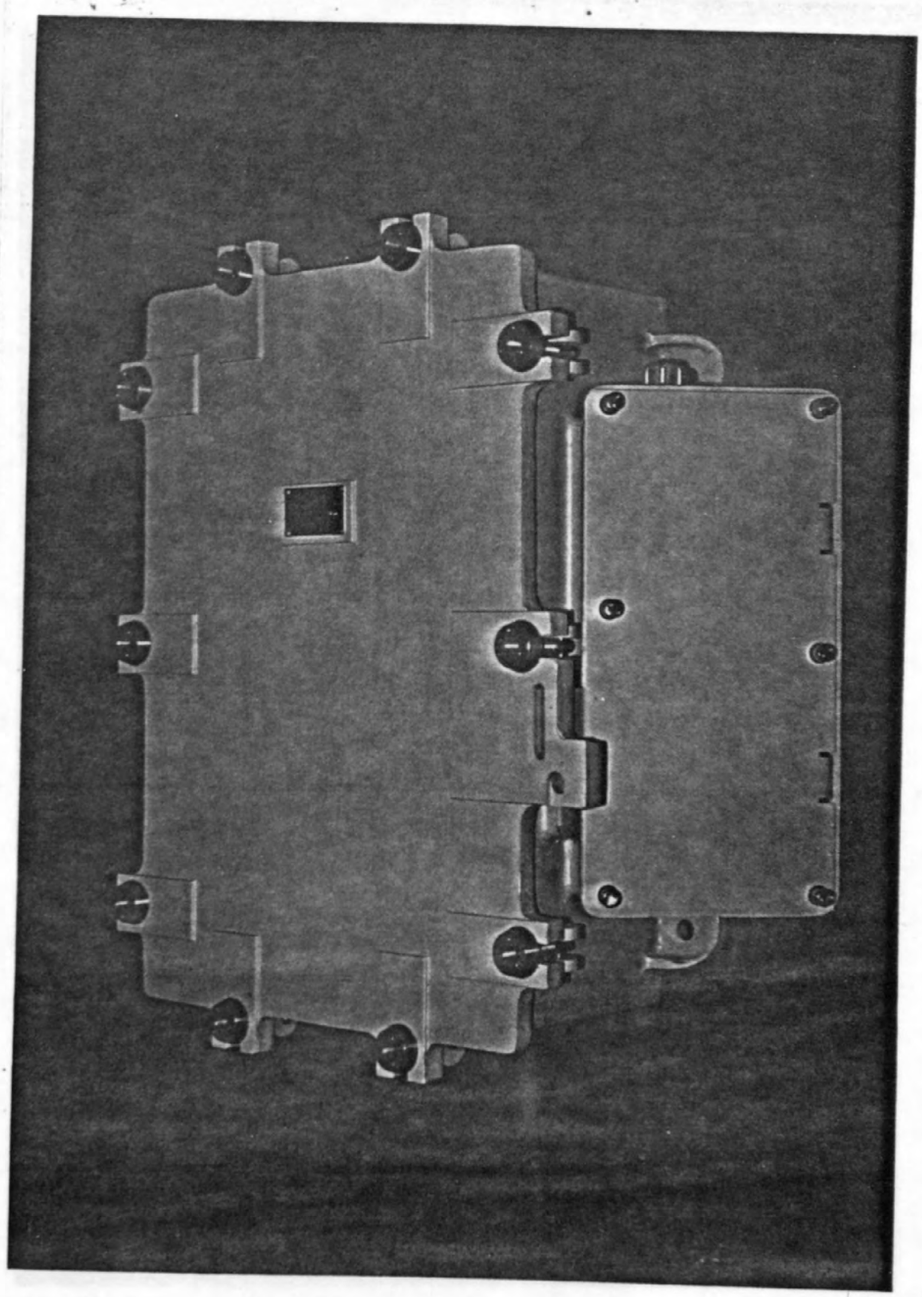

Figure 4. GOES Interrogated Data Collection Platform Radio Set

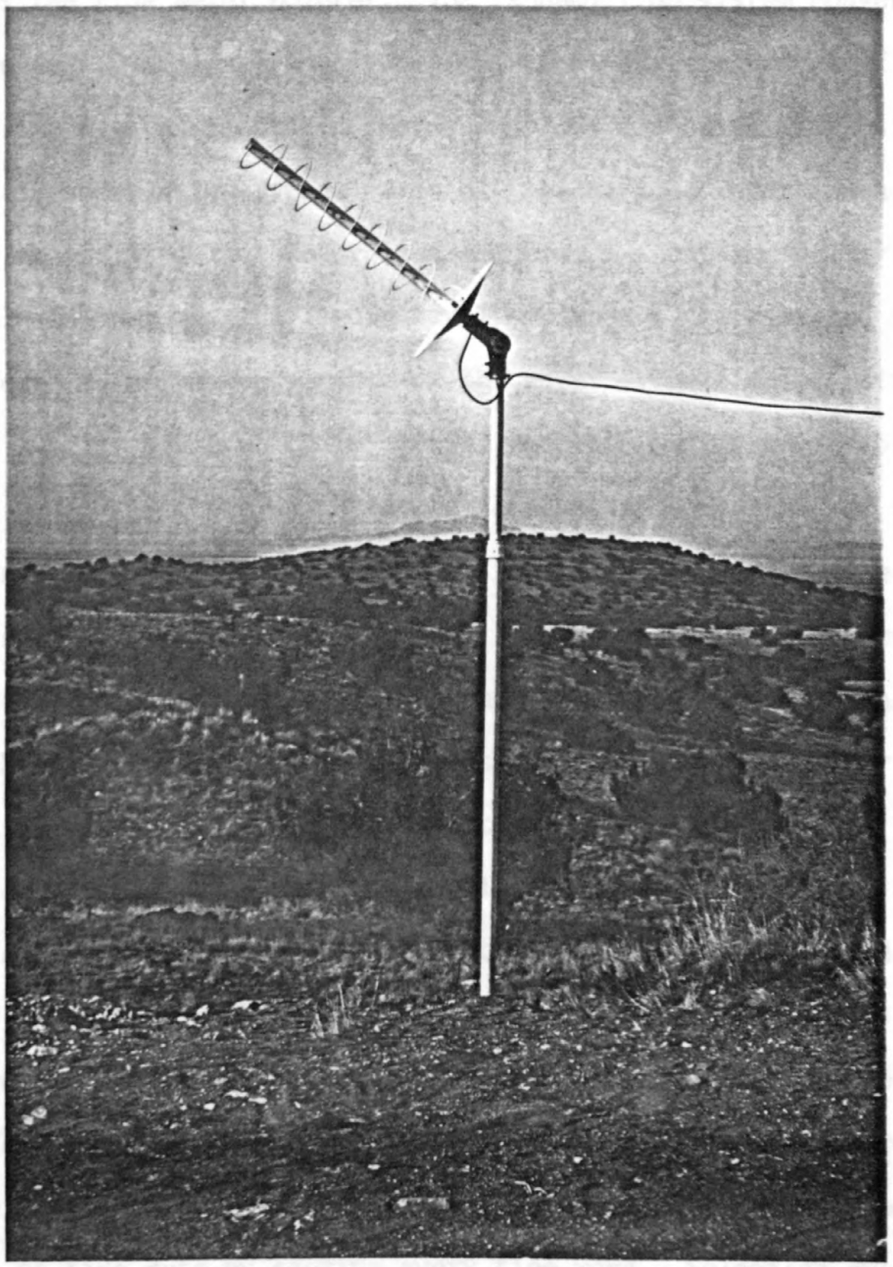

Figure 5. GOES Radio Set Antenna

The initial system program was set up to allow a float type tide meter to operate with the tide systems. These types of float tide meters have a signal whose pulse-width is proportional to the position of the float or tide level position of the tide meter pointer. The Tsunami tide system converts this variable-pulse-width signal into a digital count representative of the actual tide level. A typical float tide meter provides one pulse-width signal or tide word every 15 seconds. A typical Bristol[1/] Float Tide Meter is shown in Figure 6. The Bristol Tide Meter is a commercial float and pulley type tide instrument. It measures the liquid level by sensing the rise and fall of a buoyant float riding on the surface of the water. The float is attached to a perforated tape or cable which is carried over the pulley on the back of the tide meter case. A counterweight is fastened at the other end of the tape to keep the tape taut. When the tide meter is indicating zero on the meter, the unit is transmitting a pulse-width signal of three seconds duration. When the tide meter is indicating full scale on the meter, the unit is transmitting a pulse-width signal of 12 seconds duration. The Bristol Tide Meter will transmit a pulse-width duration signal, corresponding to the tide level, every 15 seconds and thus four tide level readings per minute.

The Tsunami Microprocessor Tide System reads every tide word from the tide meter and displays the tide level reading on digital displays. The storage program allows for every tide word, or second tide word, or every "N" th tide word to be stored into memory. The value of "N" is program selectable. With forty words of tide memory it is possible to store the last 10 minutes of tide data by storing every tide word. Selecting every fourth tide word for storage, it is possible to store the last forty minutes of tide data. This system converts the pulse-width analog output signal from the

[1/] Use of brand names in this report is for descriptive purposes only and in no way constitutes endorsement by the U.S. Geological Survey.

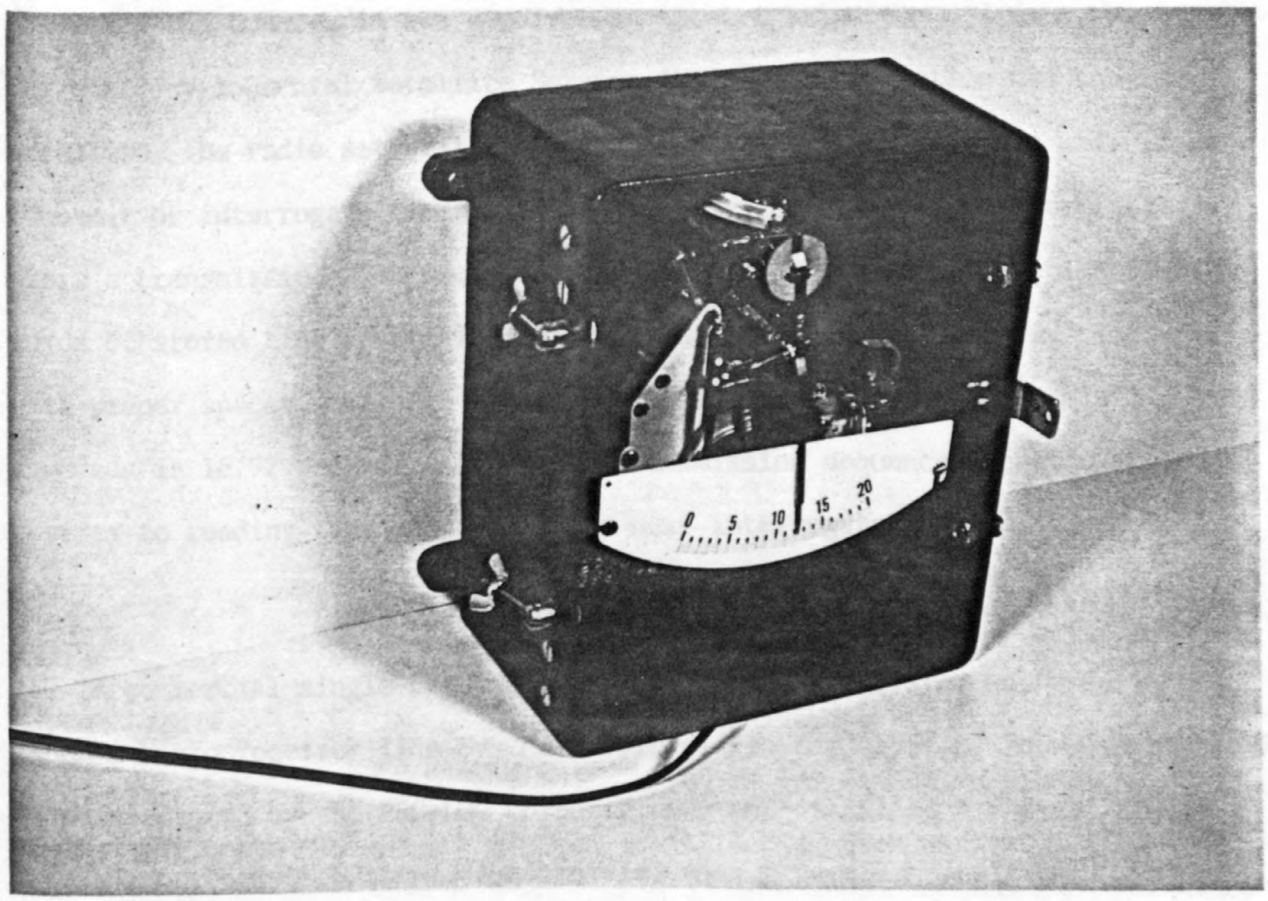

Figure 6. Typical Bristol Float Tide Meter

Bristol Tide Meter into a digital value corresponding to the duration of the tide meter pulse. This digital value will be represented by four decimal digits of tide data, expressed in units of tide. The value of tide data can vary corresponding to the tide level and may take on values from 0000 to 1999. These 13 digital bits correspond to one tide-data word.

It is possible to scale the digital values of 0000 to 1999 into any measurement units by simple software changes. Thus it is possible to represent the tide levels in inches, feet, centimeters, meters, or any other unit of length.

When the GOES radio set receives an interrogation command from the National Environmental Satellite Service (NESS) ground station via the GOES Satellite, the radio set will turn on its RF transmitter and then will issue a transmit or interrogate command to the tide system. The tide system will start a transmission mode sequence and will serially transmit the last forty words of stored tide data. The entire transmission time for forty tide words with proper spaces, carriage returns, line feeds, and end of transmission commands is 16.72 seconds. After the transmission sequence the tide system reverts to reading tide data until the next interrogate command is received.

4004 MICROPROCESSOR SYSTEM

A commercial single-card 4004 CPU microprocessor system was used in the Tsunami Microprocessor Tide System. This single-card system, shown in Figure 7, is manufactured by the PRO-LOG Corporation[2/] and is called a PLS-401 Single Card Microprocessor System. A commercial microprocessor single-card system was selected for several reasons. The first reason was to use commercial

2/ Use of brand names in this report is for descriptive purposes only and in no way constitutes endorsement by the U. S. Geological Survey.

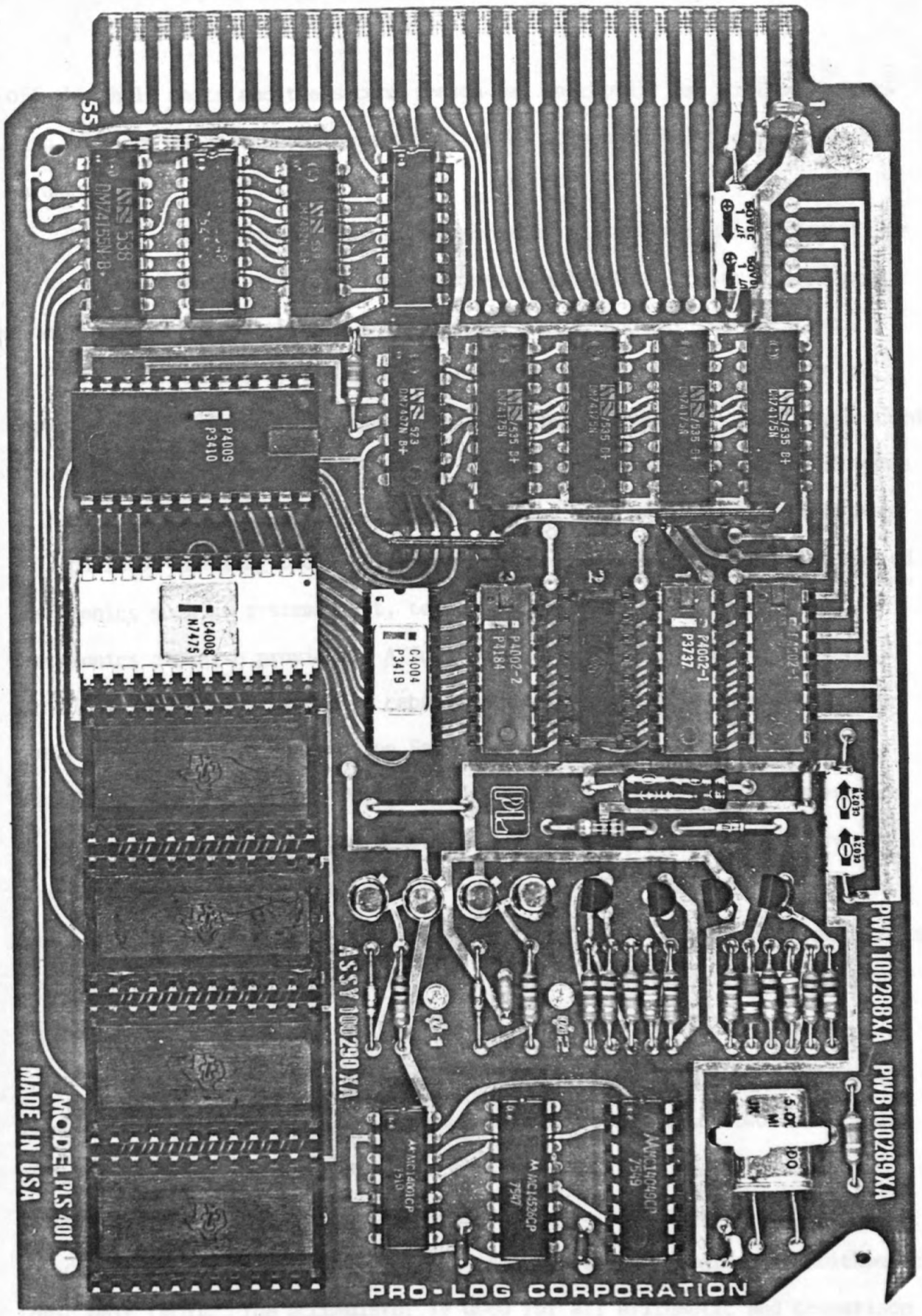

Figure 7. Single Card 4004 Microprocessor System

off-the-shelf units and the second reason was to rapidly use microprocessors with no long design time or development tasks to obtain the microprocessor hardware.

The PLS-401 microprocessor system contains all the essential elements or units to implement a complete working system with CPU, EPROM or ROM program memory, random access memory (RAM), crystal clock, and digital data input/output ports. Such a system organization provides adequate capability and capacity to perform complex system functions and operations. This single card system provides 1024 words of EPROM or ROM program memory capacity, 320 words of RAM storage capacity, five output ports, and four input ports. Each port is capable of handling one parallel 4-bit word. All the necessary associated electronics such as system reset, test, system clock, and CPU interface electronics are also provided. A functional schematic is shown in Figure 8.

This single card system is capable of executing all 46 program instructions of the 4004 CPU Instruction Set except the DCL and WPM instructions. The DCL instruction is for "Designate Command Line," and the WPM instruction is for "Write into RAM Program Memory." In a one card system there are no command lines nor RAM program memory, but the loss of these two instructions does not have any effect on the effectiveness or capability of the instruction set and microprocessor performance. The 4004 CPU instructions are shown in Figures 9, 10, and 11.

The 4004 CPU has eight internal register pairs for temporary internal data or instruction storage. Each register pair consists of two 4-bit index registers. These index registers or register pairs can be individually addressed or paired addressed for data storage or data retrieval. The CPU has one 4-bit accumulator with one bit of carry commonly called an Arithmetic Logic Unit (ALU). The accumulator is used for all arithmetic and comparison

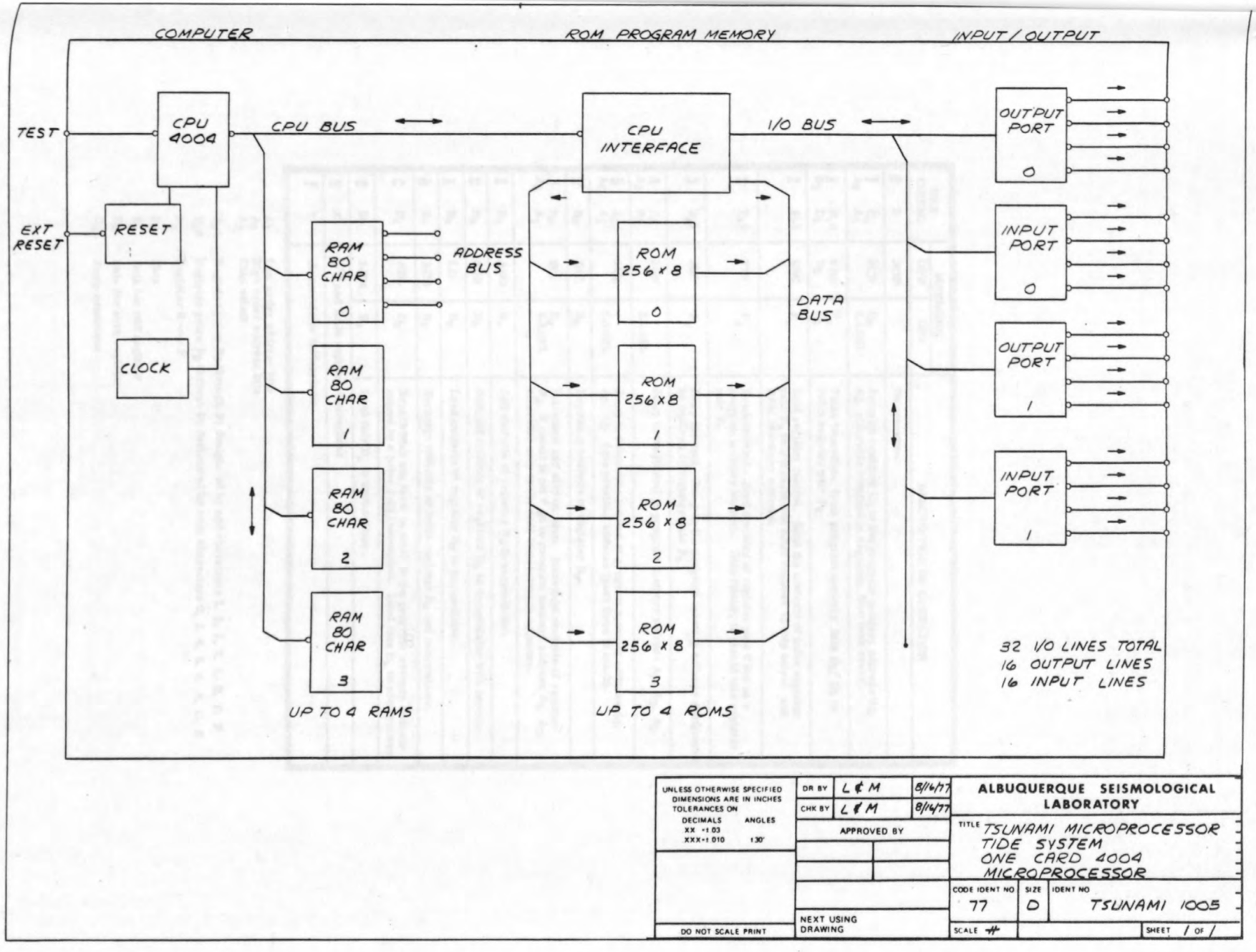

Figure 8. Single Card 4004 Microprocessor System Functional Schematic

HEX CODING	MNEMONIC OPR	MNEMONIC OPA	DESCRIPTION OF OPERATION
0 0	NOP		No operation.
1 C_X A_2 A_1	JCN	C_X LABEL	Jump on condition C_X to the program memory address A_1, A_2, otherwise continue in sequence. (see back cover).
2 P_X0 D_2 D_1	FIM D_2	P_X D_1	Fetch immediate from program memory data D_1, D_2 to index register pair P_X
2 P_X1	SRC	P_X	Send register control. Send the contents of index register pair P_X to I/O ports and RAM register as chip select and RAM character address.
3 P_X0	FIN	P_X	Fetch indirect. Send contents of register pair 0 out as a program memory address. Data fetched is placed into register pair P_X
3 P_X1	JIN	P_X	Jump indirect. Jump to the program memory address designated by contents of register pair P_X
4 A_3 A_2 A_1	JUN	LABEL	Jump unconditional to program memory address A_1, A_2, A_3.
5 A_3 A_2 A_1	JMS	LABEL	Jump to subroutine located at program memory address A_1, A_2, A_3. Save previous address (push down in stack).
6 R_X	INC	R_X	Increment contents of register R_X.
7 R_X A_2 A_1	ISZ	R_X LABEL	Increment and step on zero. Increment contents of register R_X, if result is not 0 go to program memory address A_1, A_2, otherwise step to the next instruction in sequence.
8 R_X	ADD	R_X	Add contents of register R_X to accumulator.
9 R_X	SUB	R_X	Subtract contents of register R_X to accumulator with borrow.
A R_X	LD	R_X	Load contents of register R_X to accumulator.
B R_X	XCH	R_X	Exchange contents of index register R_X and accumulator.
C D_X	BBL	D_X	Branch back one level in stack to the program memory address stored by a prior JMS instruction. Load data D_X to accumulator.
D D_X	LDM	D_X	Load data D_X to accumulator.
E X	I/O and RAM register instructions		
F X	Accumulator instructions		

A_1 Low order address bits
A_2 High order address bits
A_3 Chip select

P_X1- Register pairs P_0 through P_7 designated by odd characters 1, 3, 5, 7, 9, B, D, F

P_X0 Register pairs P_0 through P_7 designated by even characters 0, 2, 4, 6, 8, A, C, E

R_X Register 0 ⟶ F

D_X Data

D_1 Data for odd register

D_2 Data for even register

C_X Jump conditions

Figure 9. 4004 CPU Instructions

I/O AND RAM REGISTER INSTRUCTIONS

HEX CODING	MNEMONIC OPR	MNEMONIC OPA	DESCRIPTION OF OPERATION
E 0	WRM		Write the contents of the accumulator into the previously selected RAM register character.
E 1	WMP		Write the contents of the accumulator into the previously selected RAM output port. (Output lines.)
E 2	WRR		Write the contents of the accumulator into the previously selected output port. (I/O lines.)
E 3	WPM		Write the contents of the accumulator into the previously selected RAM program memory.
E 4	WR0		Write the contents of the accumulator into the previously selected RAM status character 0.
E 5	WR1		Write the contents of the accumulator into the previously selected RAM status character 1.
E 6	WR2		Write the contents of the accumulator into the previously selected RAM status character 2.
E 7	WR3		Write the contents of the accumulator into the previously selected RAM status character 3.
E 8	SBM		Subtract the previously selected RAM register character from accumulator with borrow.
E 9	RDM		Read the previously selected RAM register character into the accumulator.
E A	RDR		Read the contents of the previously selected input port into the accumulator. (I/O lines.)
E B	ADM		Add the previously selected RAM register character to accumulator with carry.
F C	RD0		Read the previously selected RAM status character 0 into accumulator.
E D	RD1		Read the previously selected RAM status character 1 into accumulator.
E E	RD2		Read the previously selected RAM status character 2 into accumulator.
E F	RD3		Read the previously selected RAM status character 3 into accumulator.

ACCUMULATOR INSTRUCTIONS

HEX CODING	MNEMONIC OPR	MNEMONIC OPA	DESCRIPTION OF OPERATION
F 0	CLB		Clear both. (Accumulator and carry.)
F 1	CLC		Clear carry.
F 2	IAC		Increment accumulator.
F 3	CMC		Complement carry.
F 4	CMA		Complement accumulator.
F 5	RAL		Rotate left. (Accumulator and carry.)
F 6	RAR		Rotate right. (Accumulator and carry.)
F 7	TCC		Transmit carry to accumulator and clear carry.
F 8	DAC		Decrement accumulator.
F 9	TCS		Transfer carry subtract and clear carry.
F A	STC		Set carry.
F B	DAA		Decimal adjust accumulator.
F C	KBP		Keyboard process. Converts the contents of the accumulator from a one out of four code to a binary code.
F D	DCL		Designate command line.
F E			
F F			

Figure 10. 4004 Accumulator, I/O, and RAM Instructions

C_x CONDITION TABLE FOR JCN INSTRUCTION

JCN HEX	C_x MNEMONIC	C_8	C_4	C_2	C_1	Invert Jump Condition Jump if Accumulator = 0 Jump if Carry Bit = 1 Jump if Test Input = 0 (High)
10		0	0	0	0	NO OPERATION
11	T0	0	0	0	1	Jump if test = 0 (High)
12	C1	0	0	1	0	Jump if CY = 1
13	T0+C1	0	0	1	1	Jump if test = 0 or CY = 1
14	A0	0	1	0	0	Jump if AC = 0
15	T0+A0	0	1	0	1	Jump if test = 0 or AC = 0
16	C1+A0	0	1	1	0	Jump if CY = 1 or AC = 0
17	T0+C1+A0	0	1	1	1	Jump if test = 0 or CY = 1 or AC = 0
18		1	0	0	0	Jump Unconditionally
19	T1	1	0	0	1	Jump if test = 1 (Low)
1A	C0	1	0	1	0	Jump if CY = 0
1B	T1C0	1	0	1	1	Jump if test = 1 and CY = 0
1C	A1	1	1	0	0	Jump if AC $\neq$ 0
1D	T1A1	1	1	0	1	Jump if test = 1 and AC $\neq$ 0
1E	C0A1	1	1	1	0	Jump if CY = 0 and AC $\neq$ 0
1F	T1C0A1	1	1	1	1	Jump if test = 1 and CY = 0 and AC $\neq$ 0

REGISTER PAIR PX LOOKUP TABLE

	PX 0 RRR 0		PX 1 RRR 1	
PX	FIM	FIN	SRC	JIN
P0	20	30	21	31
P1	22	32	23	33
P2	24	34	25	35
P3	26	36	27	37
P4	28	38	29	39
P5	2A	3A	2B	3B
P6	2C	3C	2D	3D
P7	2E	3E	2F	3F

Figure 11. 4004 Register Pair and Jump On Condition Instructions

instructions as well as the central transfer register. All incoming, outgoing, or transferred data must pass thru the accumulator. The CPU also has a 12-bit program address register, 3 level 12-bit subroutine address stack, and an 8-bit instruction register. These units comprise the 4004 CPU. The 4004 CPU is contained within one 16 pin dual-in-line chip. The 4004 CPU performs all control and data transfer functions with the program memory, RAM registers, and input/output ports thru an interconnecting 4-bit CPU bus, CPU interface, and data bus.

TSUNAMI MICROPROCESSOR TIDE SYSTEM DESIGN

The Tsunami Microprocessor Tide System flow diagram is shown in Figure 12. This flow diagram represents the tide program for use with the Bristol Tide Meter. During the non-interrogated periods, the tide system continually reads and stores the sequential tide readings, but it also checks every 4.5 milliseconds or less for the GOES Satellite interrogation command. If no interrogation command is received the system will continue in the "Data Processing and Storage" loop of the program. If an interrogation command is received, the tide system will jump to the "Transmit" loop of the program. In the "Transmit" loop the microprocessor tide system will synchronize itself with the GOES Radio Set clock, then automatically start the serial data transmission with the next clock transition and will transmit the stored tide readings in 8-bit ASCII code with spaces between each tide reading. After every ten tide readings, carriage return and line feed (CRLF) commands will be transmitted. After the completion of the tide reading transmission, an end of transmission (EOT) command will be transmitted to alert the GOES Satellite ground station that the transmission is complete. After the EOT is sent the tide system will send a pulse to the GOES Radio Set to turn off the radio set

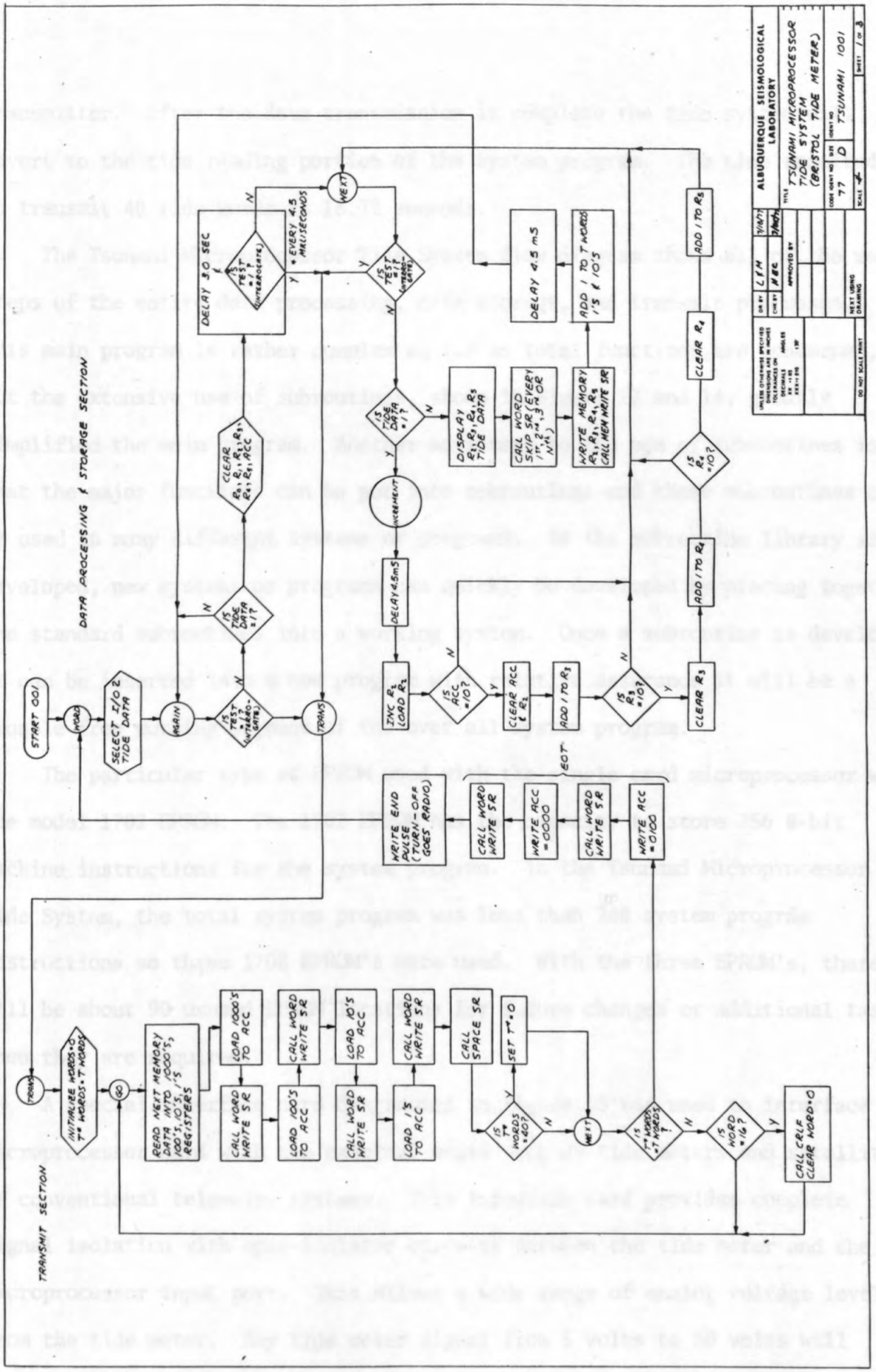

Figure 12. Tsunami Microprocessor Tide System Program Flow Diagram

transmitter. After the data transmission is complete the tide system will revert to the tide reading portion of the system program. The time required to transmit 40 tide words is 16.72 seconds.

The Tsunami Microprocessor Tide System flow diagram shows all of the main steps of the entire data processing, data storage, and transmit processes. This main program is rather complex as far as total functions are concerned, but the extensive use of subroutines, shown in Figure 13 and 14, greatly simplified the main program. Another advantage to the use of subroutines is that the major functions can be put into subroutines and these subroutines can be used in many different systems or programs. As the subroutine library is developed, new systems or programs can quickly be developed by piecing together the standard subroutines into a working system. Once a subroutine is developed it can be inserted into a new program with relative assurance it will be a trouble free working segment of the over all system program.

The particular type of EPROM used with the single card microprocessor was the model 1702 EPROM. The 1702 EPROM has the capacity to store 256 8-bit machine instructions for the system program. In the Tsunami Microprocessor Tide System, the total system program was less than 768 system program instructions so three 1702 EPROM's were used. With the three EPROM's, there will be about 90 unused EPROM locations for future changes or additional tasks when they are required.

A special interface card diagrammed in Figure 15 was used to interface the microprocessor card with the external units such as tide meters and satellite or conventional telemetry systems. This interface card provides complete signal isolation with opto-isolator circuits between the tide meter and the microprocessor input port. This allows a wide range of analog voltage levels from the tide meter. Any tide meter signal from 5 volts to 30 volts will

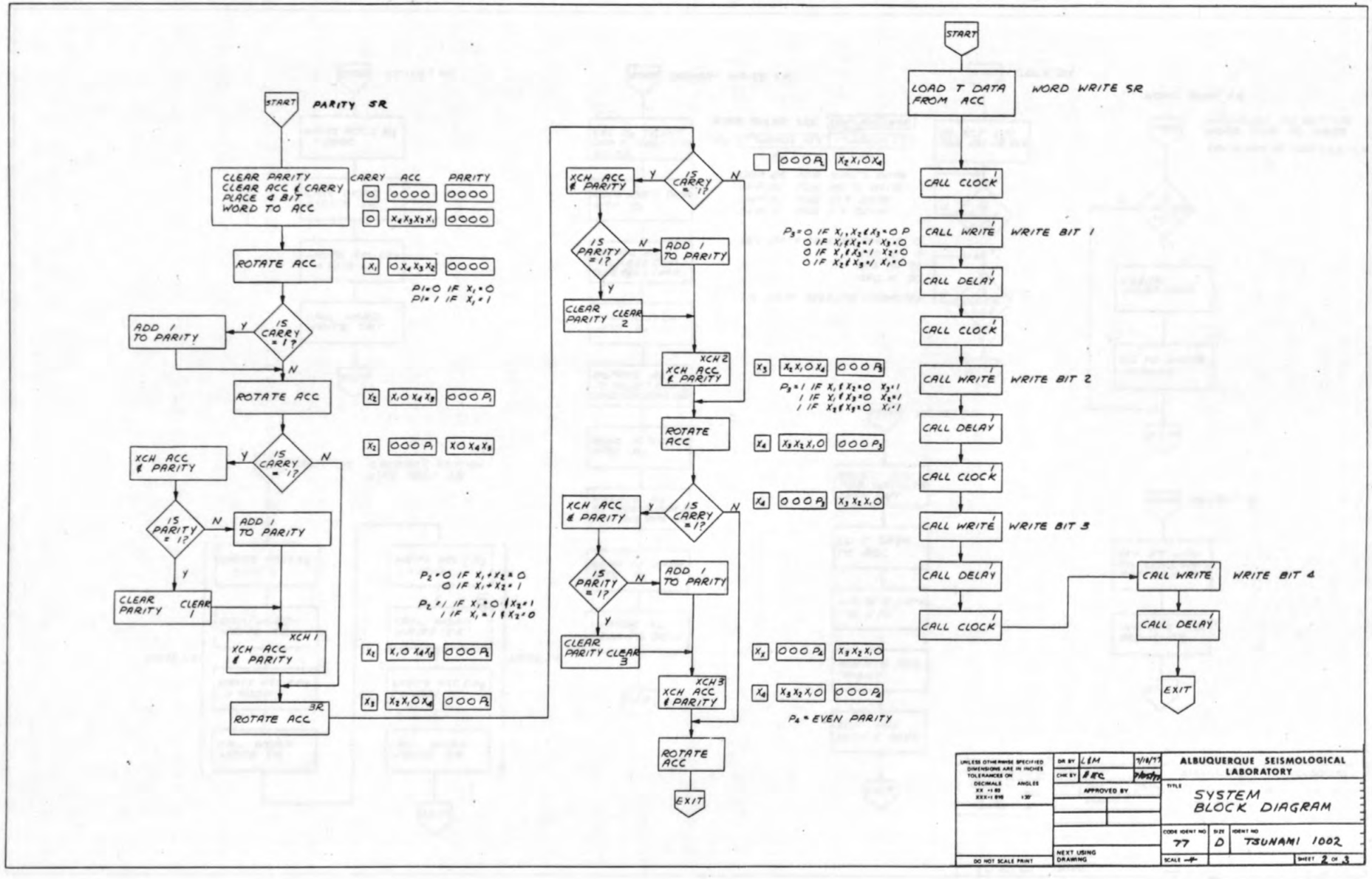

Figure 13. Tsunami Microprocessor Tide System Subroutine Flow Diagram 1

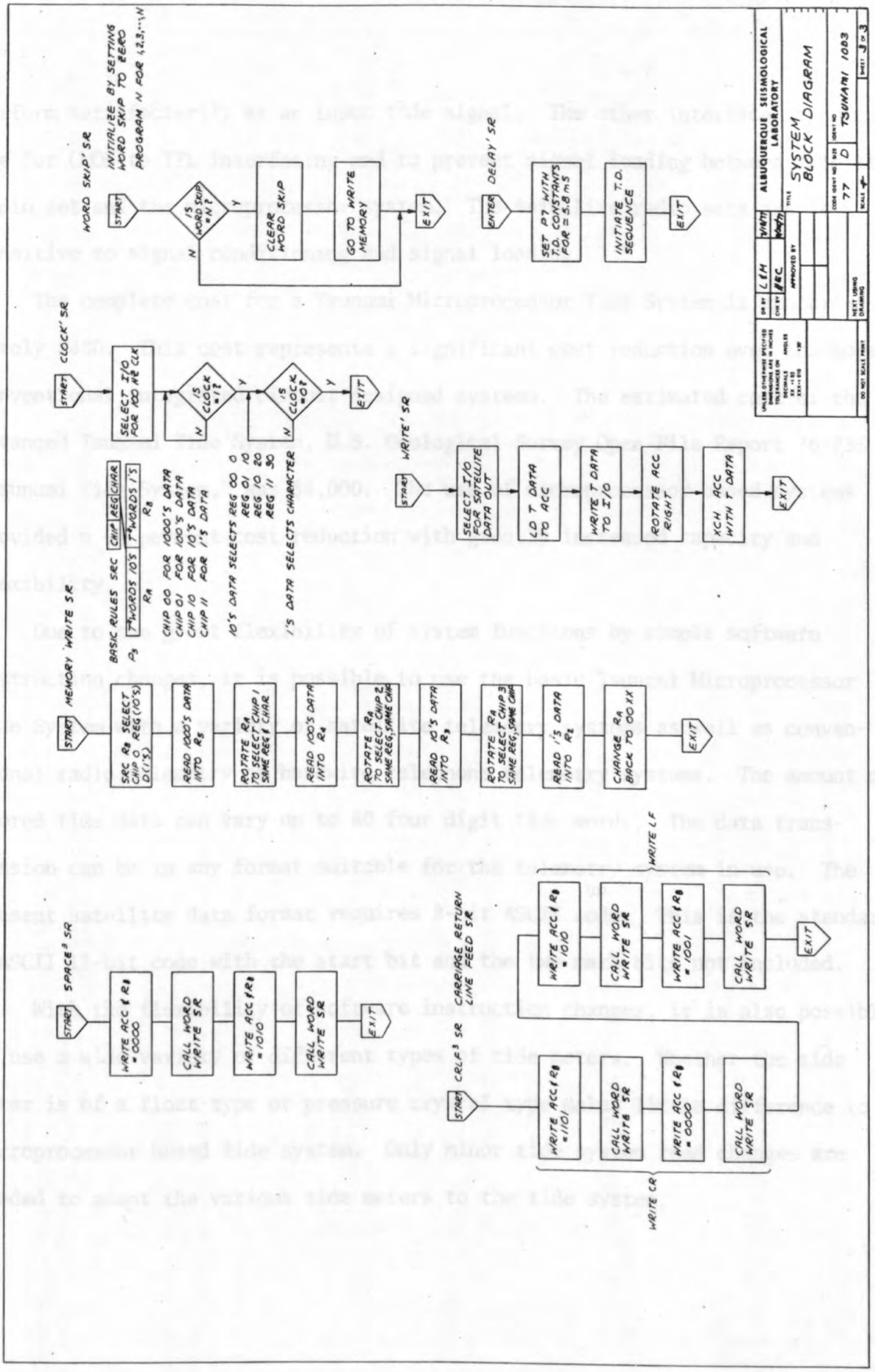

Figure 14. Tsunami Microprocessor Tide System Subroutine Flow Diagram 2

perform satisfactorily as an input tide signal. The other interface circuits are for CMOS to TTL interfacing and to prevent signal loading between satellite radio set and the microprocessor system. The satellite radio sets are very sensitive to signal conditioning and signal loading.

The complete cost for a Tsunami Microprocessor Tide System is approximately $400. This cost represents a significant cost reduction over the more conventional integrated circuit designed systems. The estimated cost of the Advanced Tsunami Tide System, U.S. Geological Survey Open-File Report 76-735 "Tsunami Tide System," was $4,000. The use of microprocessor based systems provided a 90 percent cost reduction with greatly increased capacity and flexibility.

Due to the great flexibility of system functions by simple software instruction changes, it is possible to use the basic Tsunami Microprocessor Tide System with a variety of satellite telemetry systems as well as conventional radio telemetry or hardwire telephone telemetry systems. The amount of stored tide data can vary up to 80 four digit tide words. The data transmission can be in any format suitable for the telemetry system in use. The present satellite data format requires 8-bit ASCII code. This is the standard USASCII 11-bit code with the start bit and the two mark bits not included.

With the flexibility of software instruction changes, it is also possible to use a wide variety of different types of tide meters. Whether the tide meter is of a float type or pressure crystal type makes little difference to a microprocessor based tide system. Only minor tide system read changes are needed to adapt the various tide meters to the tide system.

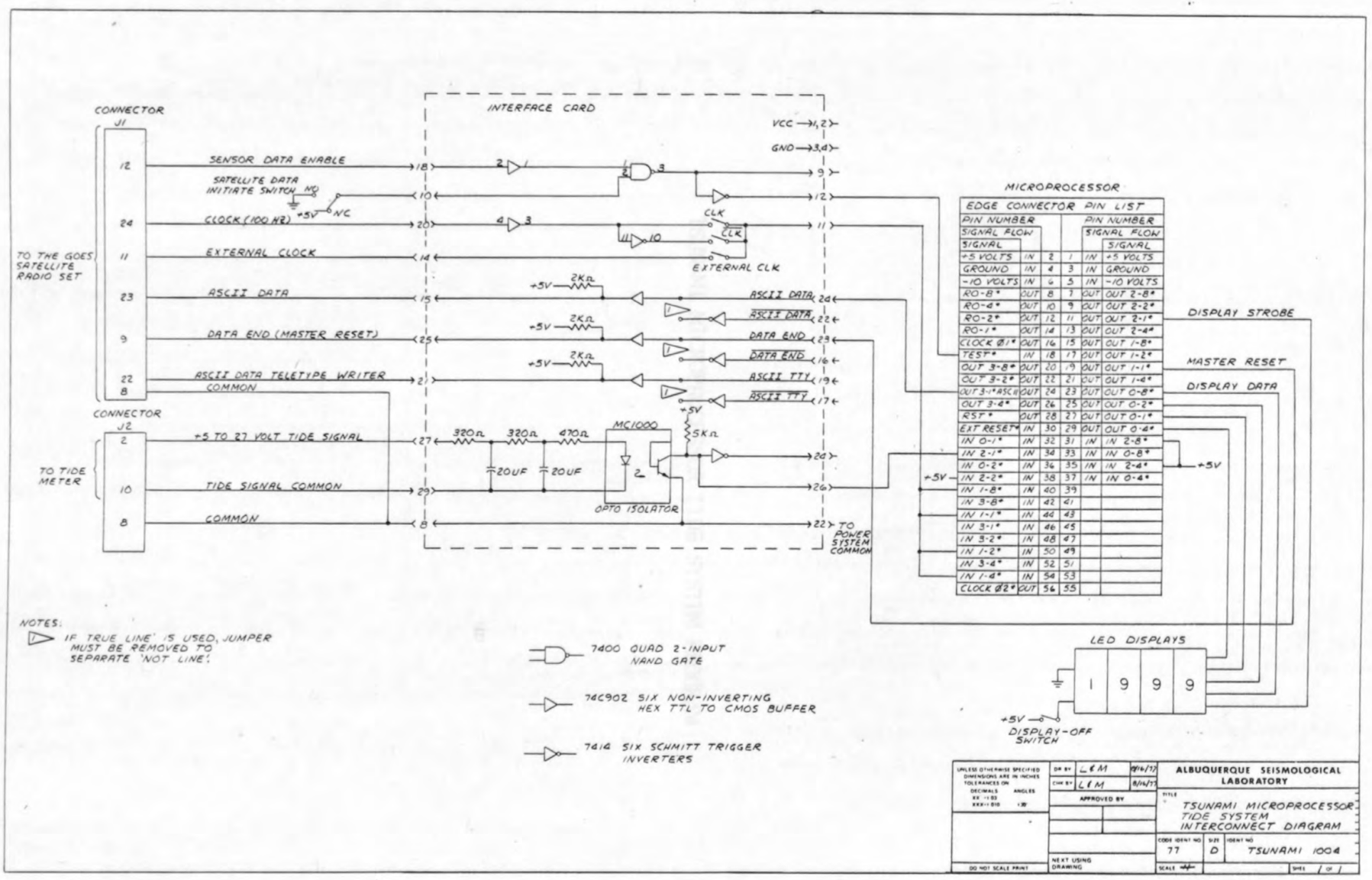

Figure 15. Tsunami Microprocessor Tide System Interconnect Diagram

TSUNAMI MICROPROCESSOR TIDE SYSTEM PROGRAM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	LABEL	MNEMONIC INSTRUCTION OPERATION	MNEMONIC INSTRUCTION OPERAND	TITLE Tsunami Tide II DATE Sept 76 COMMENTS
	00	00	NOP	NOP		
	1	2E	WORD	FIM	P7	Select I/O = Part 2 for Tide Data
	2	22			22	
	3	2F		SRC	P7	
	4	19	AGAIN	JCN	T1	Jump to TRANS if T=1 Interrogate on.
	5	F0			TRANS	
	6	F0		CLB		Read Tide data in. Is TD = 1?
	7	EA		RDR		
	8	1C		JCN	AC ≠ 0	
	9	04			AGAIN	
	A	F0		CLB		Clear R_2, R_3, R_4, R_5
	B	B2		XCH	R_2	
	C	F0		CLB		
	D	B3		XCH	R_3	
	E	F0		CLB		
	F	B4		XCH	R_4	
0	10	F0		CLB		
	1	B5		XCH	R_5	
	2	F0		CLB		
	3	00				
	4	00				
	5	2A		FIM	P5	3 sec. time delay with Test = 1
	6	47			47	
	7	2C		FIM	P6	Check.
	8	30			30	
	9	2E		FIM	P7	
	A	E0			E0	
	B	7A	3 sec. →	ISZ	RA	
	C	1B	←		3 sec.	
	D	7B		ISZ	RB	
	E	1B	←		Check	
	F	19	Check	JCN	T = 1	Check for Test = 1

TITLE Tsunami Tide II DATE Sept 76

PAGE ADR	LINE ADR	INSTR	LABEL	INSTRUCTION OPERATION	INSTRUCTION OPERAND	COMMENTS
0	20	FO			TRANS	
	1	00				
	2	00				
	3	7C		ISZ	RC	
	4	1B			3 sec.	
	5	7D		ISZ	RD	
	6	1B			3 sec.	
	7	7E		ISZ	RE	
	8	1B			3 sec.	
	9	00				
	A	00				
	B	FO		CLB		
	C	19	Next.	JCN	Test = 1	T is Test = 1
	D	FO			TRANS	
	E	00				
	F	2E		FIM	P7	
0	30	22			22	
	1	2F		SRC	P7	
	2	EA		RDR		
	3	14		JCN	ACC = 0	
	4	CO			Increment	
	5	2A		FIM	P5	load display pointer to 0000
	6	00			00	
	7	2C		FIM	P6	
	8	22			22	
	9	2D		SRC	P6	
	A	AA		LD	RA	Write 0000 into Port 2
	B	E2		WRR		
	C	2A		FIM	P5	Load display pointer to D4 (1000's tide data)
	D	11			11	Display enable (1110)
	E	2E		FIM	P7	
0	F	00			00	Select Port 0 output for display data.

PAGE ADR	LINE ADR	INSTR	LABEL	MNEMONIC INSTRUCTION OPERATION	OPERAND	TITLE Tsunami Tide II DATE Sept 76 COMMENTS
0	40	2F		SRC	F7	
	1	A5		LD	R5	Write 1000's tide data into Port 0
	2	F4		CMA		
	3	E2		WRR		
	4	2D		SRC	P6	Strobe 1000's Data into D4
	5	AA		LD	RA	load 0001 (1110) into Port 2 then
	6	E2		WRR		load 0000 (1111) into Port 2
	7	AE		LD	Re	Strobe Port 2
	8	E2		WRR		
	9	2A		FIM	P5	Load display pointer to P3 (100's tide
	A	22			22	data) display enable (1101)
	B	2F		SRC	P7	Select Port 0 and write 100's data.
	C	A4		LD	R4	
	D	F4		CMA		
	E	E2		WRR		Strobe 100's data into P3
0	4F	2D		SRC	P6	Load 0010 (11011 into Port 2 then
0	50	AA		LD	RA	load 0000 (1111) Port 2
	1	E2		WRR		Strobe 100's data
	2	AE		2D	Re	
	3	E2		WRR		
	4	2A		FIM	P5	load display pointer to D2 (10's
	5	44			44	tide data) display enable (1011)
	6	2F		SRC	P7	Select Port 0 and write 10's Data
	7	A3		LD	R3	
	8	F4		CMA		
	9	E2		WRR		
	A	2D		SRC	P6	Strobe 10's data into D2
	B	AA		LD	RA	load 0100 (1011) into Port 2
	C	E2		WRR		then load 0000 (1111) into Port 2
	D	AE		LD	Re	
	E	E2		WRR		
0	5F	2A		FIM	P5	load display pointer to D1 (1's tide

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTRUCTION OPERATION	MNEMONIC INSTRUCTION OPERAND	TITLE Tsunami Tide II DATE Sept 76 COMMENTS
0	60	88			88	data. Display enable (0111).
	1	2F		SRC	P7	
	2	A2		LD	R_2	
	3	F4		CMA		
	4	E2		WRR		
	5	2D		SRC	P6	Select Port 2 strobe 1000 into Port 2
	6	AA		LD	P5	
	7	E2		WRR		Write
	8	AE		LD	P7	load P7 (0000) strobe 0000 into Port 2
	9	E2		WRR		
	A	FO	Word skip	CLB		Word skip will skip every other
	B	A8		LD	R8	word and not write into
	C	F6		RAR		memory
	D	00				
	E	00				
	F	68		INC	R8	
	70	1A		JCN	Carry = 0	
	1	01			Word	
	2	FO		CLB		
	3	00				
	4	00				
	5	00				
	6	00				
	7	27		SRC	P3	Select chip 0, Reg (10's), char (1's)
	8	A5		LD	RS	Write 1000's Data into Ram
	9	EO		WRM		
	A	A6		LD	P3	Change R6 to 10's 1's word point: 01 | XX | XXXX (chip, reg, char)
	B	F5		RAL		
	C	F5		RAL		
	D	FA		STC		
	E	F6		RAR		
	7F	F1		CLC		

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	LABEL	MNEMONIC INSTRUCTION OPERATION	MNEMONIC INSTRUCTION OPERAND	TITLE Tsunami Tide II , DATE Sept 76 COMMENTS
0	80	F6		RAR		
	1	B6		XCH	R6	
	2	27		SRC	P3	Select chip 1, Reg (10's), char (1's)
	3	A4		LD	R4	Write 100's Data into RAM
	4	E0		WRM		
	5	A6		LD	R6	Change R6 to 10XX XXXX
	6	F5		RAL		
	7	F5		RAL		
	8	F1		CLC		Change R6 to 10XX XXXX
	9	F6		RAR		
	A	FA		STC		
	B	F6		RAR		
	C	B6		Xch	R6	
	D	27		SRC	P3	Select chip 2, Reg (10's), char (1's)
	E	A3		LD	R3	Write 10's data into RAM
	F	E0		WRM		
0	90	A6		LD	R6	change R6 to 11XX XXXX
	1	F5		RAL		
	2	F5		RAL		
	3	FA		STC		
	4	F6		RAR		
	5	F6		RAR		
	6	B6		SCH	R6	
	7	27		SRC	P3	select chip 3, Reg (10's), char (1's)
	8	A2		LD	R2	write 1's data into RAM
	9	E0		WRM		
	A	A6		LD	R6	change R6 to 00XX XXXX
	B	F5		RAL		
	C	F5		RAL		
	D	F1		CLC		
	E	F6		RAR		
	9F	F1		CLC		

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTRUCTION OPERATION	MNEMONIC INSTRUCTION OPERAND	TITLE Tsunami Tide II DATE Sept 76 COMMENTS
	A 0	F6		RAR		
	1	B6		Xch	R6	
	2	FO		CLB		Add 1 to 1's T words if 10
	3	A7		LD	R7	set 1's to 0 add 1 to 10's T words
	4	F2		IAC		
	5	FB		DAA		
	6	B7		Xch	R7	
	7	1A		JCN	C=0	
	8	B4	←		Delay 1	
	9	FO		CLB		
	A	B7		XCH	R7	
	B	66	↓	INC	R6	
	C	FO		CLB		If 10's T word = 40 set 10's T word
	D	A6		LD	R6	
	E	F5		RAL		to 0
	A F	F5		RAL		
0	B 0	1A		JCN	C=0	
	1	B4	←		Delay 1	
	2	FO	↓	CLB		
	3	B6		XcH	R6	
	4	2E	Delay 1 →	FLM	P7	
	5	03			03	
	6	7E	D1 →	ISZ	RE	
	7	B6	←		D1	
	8	7E		ISZ	RF	
	9	B6	→		D1	
	A	40		JVN	0	
	B	01			Word	
	C	00				
	D	00				
	E	00				
0	B F	00				

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTRUCTION OPERATION	MNEMONIC INSTRUCTION OPERAND	TITLE Tsunami Tide II , DATE Sept 76 COMMENTS
0	C0	F0	Increment	CLB		clear carry
	1	2E		FLM	P7	
	2	25			25	Delay 4.5ms for 1 count T Data
	3	2C		FLM	P6	
	4	F0			F0	
0	C5	7E	Delay 2	ISZ	RE	
0	C6	C5			Delay 2	
	7	7F		ISZ	RF	
0	C8	C5			Delay 2	
	9	7C		ISZ	RC	
	CA	C5			Delay 2	
	B	62		INC	R2	
	C	A2		LD	R2	
	D	00				
	E	FB		DAA		
	CF	1A		JCN	CY=D	
0	D0	2C			Next	If ACC is 10 (R_2=10), clear ACC, R_2
	1	F0		CLB		and increment R3
	2	B2		XCH	R2	
	3	F0		CLB		
	4	63		INC	R3	
	5	00				If ACC is 10 (R_3=10), clear ACC, R3
	6	A3		LD	R3	and increment R4
	7	FB		DAA		
	8	1A		JCN	CY=0	
0	D9	2C			NEXT	
	A	F0		CLB		
	B	B3		XCH	R3	
	C	64		INC	R4	
	D	00				If ACC is 10 (R_4=10), clear ACC, R4
	E	A4		LD	R4	and increment R5
0	DF	FB		DAA		

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTRUCTION OPERATION	MNEMONIC INSTRUCTION OPERAND	TITLE Tsunami Tide II , DATE Sept 76 COMMENTS
0	E 0	1A		JCN	CY=0	
	1	2C			Next	
	2	F0		CLB		
	3	B4		XcH	R4	
	4	65		INC	R5	
	5	40		JVN	0	
	6	2C			Next	
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
0	EF					
0	F 0	F0	TRANS	CLB		
	1	BC		Xch	Rc	Clear Words register
	2	A6		LD	R6	
	3	BA		Xch	RA	Load T words' 10's into T* words 10's
	4	A7		LD	R7	register and T words 1's into T* words 1's
	5	BB		Xch	RB	register
	6	52		JMS		CRLF
	7	6C				
	8	41		JVN	100	
	9	00				
	A					
	B					
	C					
	D					
	E					
0	FF					

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTRUCTION OPERATION	MNEMONIC INSTRUCTION OPERAND	TITLE Tsunami Tide II , DATE Sept 76 COMMENTS
1	00					
	01					
1	02	D6	GO	LD	R6	Set up CR, LF counter
	03	BC		Xch	RC	
	04	51		JMS		Jump to Memory. Write to Load
	05	EO			Memory write	Registers 2,3,4,5, with Tide word.
	06					
	07					
	08					
1	09	A5	Word write	LD	R5	load 1000's data to R8
	0A	B8		Xch	R8	
	0B	52		JMS		
	0C	20			Parity	
	0D	51		JMS		Write 1000's data into bits b_1, b_2, b_3, b_4
	0E	CO			4 bit SW	
	0F	A9		LD	R9	Write &
1	20	F6		RAR		load parity and number code for
	21	00				b_5, b_6, b_7, b_8
	22	00				
	23	D3		LD	Re	
	24	F6		RAR		
	25	B8		Xch	R8	
	26	51		JMS		
	27	CO			4 bit SW	
	28	A4		LD	R4	load 100's data to R8
	29	B8		Xch	R8	
	2A	52		JMS		
	2B	20			Parity	
	2C	51		JMS		write 100's data into bits b_1, b_2, b_3, b_4
	2D	CO			4 bit SW	
	2E	00				
1	2F	00				

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTRUCTION OPERATION	MNEMONIC INSTRUCTION OPERAND	TITLE Tsunami Tide II , DATE Sept 76 COMMENTS
	20	A9		LD	R9 .	load and write parity and number code
	1	F6		RAR		for b_5, b_6, b_7, b_8
	2	D6		LD	Re	
	3	F6		RAR		
	4	B8		Xch	R8	
	5	51		JMS		
	6	CO			4 bit SW	
	7	A3		LD	R3	load 10's data to R8
	8	B8		Xch	R8	
	9	52		JMS		
	A	20			Parity	
	B	51		JMS		Write 10's data into bits b_1 b_2 b_3 b_4
	C	CO			4 bit SW	ASC 11 code
	D	A9		LD	R9	
	E	F6		RAR		load and wirte parity and bumber code
	F	D6		LD	Re	for b_5, b_6, b_7, b_8
	30	F6		RAR		
	31	B8		Xch	R8	
	2	51		JMS		
	3	CO			4 bit SW	
	4	A2		LD	R2	load 1's dat to R8
	5	B8		Xch	R8	
	6	52		JMS		
	7	20			Parity	
	8	51		JMS		Write 1's data into bits b_1, b_2, b_3, b_4
	9	CO			4 bit SW	
	A	A9		LD	R9	
	B	F6		RAR		load and wirte parity and number code
	C	D6		LD	Re	for b_5, b_6, b_7, b_8
	D	F6		RAR		
	E	B8		Xch	R8	
	3F	00				

TITLE Tsunami Tide II DATE Sept 76

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTRUCTION OPERATION	MNEMONIC INSTRUCTION OPERAND	COMMENTS
1	40	51		JMS		
	1	CO			4 Bit SW	
	2					
	3					
	4					
	5	52		JMS		
	6	60			SPACE	
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					
	50	60		Inc		Increment CRLF counter
	1					
	2					
	3					
	4					
	5					
	6	FO		CLB		Add 1 to 1's T* words of
	7	AB		LD	RB	10 set 1's to 0 add 1 to
	8	F2		IAC		10's T words
	9	FB		DAA		
	A	BB		XCH	RB	
	B	1A		JCN	CY=0	
	C	68			NEXT	
	D	FO		CLB		
	E	BB		Xch	RB	
	F	6A		INC	RA	

HEXADECIMAL PAGE ADR	LINE ADR	INSTR	LABEL	MNEMONIC INSTRUCTION OPERATION	OPERAND	TITLE Tsunami Tide II DATE Sept 76 COMMENTS
1	60	FO		CLB		If 10's T* words = 40 set 10's
	1	AA		LD	RA	T* words to 0.
	2	F5		RAL		
	3	F5		RAL		
	4	1A		JCN	C=0	"Yes this is Mext, not Next."
	5	68			Mext	
	6	FO		CLB		
	7	BA		Xch	RA	
1	68	00	Mext	NOP		
	9					
	A	FO		CLB		load T word 1's data, subtract
	B	A7		LD	R7	T* words 1's data if equal (ACC=0)
	C	9B		Sub	RB	check for 10's data. If not equal
	D	1C		JCN	ACC≠0	skip to 16 words
	E	76			16 words	
	F	FO		CLB		
	70	A6		LD	R6	Same check for 10's data
	1	9A		Sub	RA	
	2	1C		JCN	ACC≠0	If T words = T* words jump
	3	76			16 words	to EOT Tranmission complete
	4	41		JUN		
	5	81			EOT	
	6	FO	16 words	CLB		
	7	AC		LD	RC	Test words for word = 16 If not
	8	00		IAC		16, jump to again. If 16, call
	9	1C		JCN	Carry = 0	CRLF
	A	04			GO	
	B	52		JMS		
	C	6C			CRLF	
	D	FO		CLB		Set words register to zero.
	E	BC		Xch	Rc	
1	7F	41		JUN		

HEXADECIMAL			MNEMONIC			TITLE Tsunami Tide II	DATE Sept 76
PAGE ADR	LINE ADR	INSTR	LABEL	INSTRUCTION OPERATION	INSTRUCTION OPERAND	COMMENTS	
1	80	02			GO		
	1	52		JMS			
	2	6C			CRLF		
	3	00	EOT				
	4	00					
	5	D4		LD	Re		
	6	B8		Xch	R8		
	7	51		JMS			
	8	CO			4 bit SW		
	9	DO		LD	Rf		
	A	B8		Xch	R8		
	B	51		FMS			
	C	CO			4 bit S.W.		
	D	00					
	E	00					
1	8F	00					
1	90	2E		FLM	P7		
	1	FO			FO		
	2	20		FLM	PO		
	3	10			10		
	4	21		SRC	PO		
	5	AE		LD	Re		
	6	E2		WRR			
	7	51		JMS			
	8	B4		XCH	R4		
	9	AF		LD	Rf		
	A	E2		WRR			
	B	40		JUN			
	C	01			Word		
	D	00					
	E	00					
1	9F	00					

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTRUCTION OPERATION	MNEMONIC INSTRUCTION OPERAND	TITLE Tsunami Tide II DATE Sept 76 COMMENTS
1	A0	20	MARK[1]	FLM	P0	load R8 with 1111 data
	1	FF			FF	
	2	A0		LD	R0	
	3	B8		Xch	R8	
	4	52		JMS		Synch with clock 100H$_z$ write
	5	4C			Clock [1]	1 data or mark data for 1 clock
	6	52		JMS		time
	7	10			Write[1]	
	8	52		JMS		
	9	59			Delay	
	A	52		JMS		Synch with clock 100H$_z$, write
	B	4C			Clock	1 data or mark data for 1 clock
	C	52		JMS		time
	D	10			Write	
	E	52		JMS		
1	AF	59			Delay	
1	B0	C0		BBL		
	1					
	2					
	3					
	B4	2E	Delay[1] 5.8ms	FIM	P7	The 0.0 code provides
	5	00			00	5.530 milli seconds "0" first
	6	7E	First	ISZ	Re	.346 " " "0" second
	7	B6			First	5.876
	8	7F		ISZ	Rf	.5m sec 100H$_z$ ½ cycle = 5
	9	B6			First	100H$_z$ ½ cycle = 4
	A	C0		BBL		for TTY delay
	B					
	C					
	D					
	E					
1	BF					

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTRUCTION OPERATION	MNEMONIC INSTRUCTION OPERAND	TITLE Tsunami Tide II DATE Sept 76 COMMENTS
1	C0	A8	4 Bit serial	LD	R8	load 4 bit word into ACC
	1	F4		CMA		complement ACC, load into R8
	2	B8		XCH	R8	
	3	52		JMS		Output fist bit after clock pulse
	4	4C			Clock	is received.
	5	52		JMS		Jump to delay
	6	10			Write	
	7	52		JMS		
	8	59			Delay	
	9	52		JMS		Output second bit after clock
	A	4C			Clock	pulse is received.
	B	52		JMS		Jump to delay
	C	10			Write	
	D	52		JMS		
	E	59			Delay	
1	CF	00				
1	D0	00				Output third bit after clock
	1	52		JMS		pulse is received.
	2	4C			Clock	Jump to delay
	3	52		JMS		
	4	10			Write	
	5	52		JMS		
	6	59			Delay	
	7	00				
	8	00				Output fourth bit after clock
	9	52		JMS		pulse is received.
	A	4C			Clock	Jump to delay
	B	52		JMS		
	C	10			Write	
	D	52		JMS		
	E	59			Delay	
1	DF	CO		BBL		

TITLE Tsunami Tide II DATE Sept 76

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTRUCTION OPERATION	MNEMONIC INSTRUCTION OPERAND	COMMENTS
1	E0	2B	Memory write	SRC	RB	Select chip 0 Reg (10's), char (1's)
	1	E9		RDM		read 1000's data and place
	2	B5		Xch	R5	in R5
	3	AA		LD	RA	
	4	F5		RAL		Select RA 00XX rotate left
	5	F5		RAL		twice. Set carry rotate right
	6	FA		STC		twice 01XX replace in RA
	7	F6		RAR		
	8	F1		CLC		
	9	F6		RAR		
	A	BA		Xch	RA	
	B	2B		SRC	RB	select chip 1 Reg (10's), char (1's)
	C	E9		RDM		read 100's data and place in R4
	D	B4		Xch	R4	
	E	BA		Xch	RA	
1	EF	F5		RAL		select RA 01XX rotate left
1	F0	F5		RAL		twice rest set carry rotate right
	1	F1		CLC		set carry rotate right 10XX
	2	F6		RAR		replace in RA.
	3	FA		STC		
	4	F6		RAR		
	5	BA		Xch	RA	
	6	2B		SEC	RB	select chip 2, Reg (10's), char (1's)
	7	E9		RDM		read 10's data and place in R3
	8	B3		Xch	R3	
	9	BA		Xch	RA	select Ra 10XX rotate left
	A	F5		RAL		twice set carry rotate right
	B	F5		RAL		set carry rotate right 11XX
	C	FA		STC		replace in RA
	D	F6		RAR		
	E	FA		STC		
1	FF			RAR		

HEXADECIMAL PAGE ADR	LINE ADR	INSTR	LABEL	MNEMONIC INSTRUCTION OPERATION	OPERAND	TITLE Tsunami Tide II — DATE Sept 76 — COMMENTS
2	00	BA		Xch	RA	
	1	2B		SRC	RB	Select chip 3, Reg (10's), char (1's)
	2	E9		RDM		read 1's data and place in R2
	3	B2		Xch	R_2	
	4	BA		Xch	RA	
	5	F5		RAL		Select RA 11XX rotate left
	6	F5		RAL		twice clear carry rotate right clear
	7	F1		CLC		carry rotate right to be
	8	F6		RAR		in original format 00XX
	9	F1		CLC		
	A	F6		RAR		
	B	BA		Xch	RA	
	C	CO		BBL		
	D					
	E					
2	F					
2	10	A8	Write[1]	LD	R8	Load T data for R8 to ACC
	1	00				Designate IO 3 as output parts
	2	00				
	3	2E		FLM	P7	TD_8 TD_4 TD_2 TD_1
	4	33			33	
	5	00				write T data IO 3
	6	00				
	7	2F		SRC	P7	
	8	E2		WRR		
	9	F1		CLC		Rotate data one bit to right
	A	F6		RAR		and store in R8.
	B	F1		CLC		
	C	B8		Xch	R8	0 X X X eventually will shift
	D	CO		BBL		out the four bits
	E					
2	1F					

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTRUCTION OPERATION	MNEMONIC INSTRUCTION OPERAND	TITLE Tsunami Tide II DATE Sept 76 COMMENTS
2	20	F0	Parity	CLB		clear R9 (Parity), Carry, ACC
	1	B9		XCH	R9	
	2	F0		CLB		
	3	A8		LD	R8	load 4 bit word into ACC
	4	F6		RAR		
	5	1A		JCN	Carry = 1	check for ist bit for 1
	6	28			2R	
	7	69		INC	R9	
	8	F6	2R	RAR		
	9	12		JCN	Carry = 1	check for 2nd bit for 1
	A	33			3R	
	B	B9		Xch	R9	
	C	1C		JCN	ACC = 1	
	D	31			Clear 1	
	E	F2		IAC		
2	2F	42		JUN		
2	30	32			Xch 1	
	1	F0	Clear 1	CLB		
	2	B9	Xch 1	Xch	R9	
	3	F6		RAR		check for 3rd bit for 1
	4	12		JCN	Carry = 1	
	5	3E			4R	
	6	B9		Xch	R9	
	7	1C		JCN	ACC = 1	
	8	3C			clear 2	
	9	F2		IAC		
	A	42		JUN		
	B	3D			Xch 2	
	C	F0	Clear 2	CLB		
	D	B9	Xch 2	Xch	R9	
	E	F6		RAR		Check 4th bit for 1
2	3F	12		JCN	Carry = 1	

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTRUCTION OPERATION	MNEMONIC INSTRUCTION OPERAND	TITLE Tsunami Tide II Parity 2/2 — DATE Sept 76 — COMMENTS
2	40	49			5R	check for 4th bit for 1
	1	B9		Xch	R9	
	2	1C		JCN	ACC = 1	
	3	47			clear 3	
	4	F2		IAC		
	5	42		JUN		
	6	48			Xch 3	
	7	FO	clear 3	CLB		
	8	B9	Xch 3	Xch	R9	↓
	9	A9	5R	LD	R9	load parity into ACC and rotate
	A	F6		RAR		right to get it into carry location
	B	CO		BBL		↓
	C	2E	clock1	FLM	PO	Select I/O Port 1 for 100Hz clock in
	D	11			11	↓
	E	2F		SRC	PO	↓
2	4F	FO	No clock	CLB		"1" "0" 100Hz clock signal
	50	EA		RDR	RDR	Detect when clock is "1"
	1	1C		JCN	ACC = 1	
	2	4F		No clock		↓
	3	FO	1 clock	CLB		Detect when clock goes from "1" to "0"
	4	EA		RDR	RDR	
	5	14		JCN	ACC = 0	Remember "0" level is low level
	6	53		1 clock		↓ for microprocessor which is Active State
	7	CO		BBL		
	8					
	9	00	Delay			
	A	00				
	B	00				
	C	00				
	D	00				
	E	00				
	5F	CO		BBL		

HEXADECIMAL			MNEMONIC			TITLE Space[1] - & - CRLF[3] DATE
PAGE ADR	LINE ADR	INSTR	LABEL	INSTRUCTION OPERATION	OPERAND	COMMENTS
2	60	20	Spare[1]	FLM	PO	load 0000 in Ro 1010 R_1
	1	02				
	2	AO		LD	Ro	load 0000 in R8 and call
	3	B8		Xch	R8	4 bit write
	4	51		JUN		
	5	CO			4 bit write	
	6	A1		LD	R1	load 0010 in R8 and call
	7	B8		Xch	R8	4 bit write
	8	51		JMS		
	9	CO			4 bit write	
	A	CO		BBL		
	B					
	C	20	CRLF[3]	FLM	PO	load 1101 in Ro 0000 R_1
	D	DO			DO	
	E	AO		LD	Ro	load 1101 in R8 and call
	F	B8		Xch	R8	4 bit write
2	70	51		JMS		
	1	CO			4 bit wirte[2]	
	2	A1		LD	R_1	load 0000 in R8 and call
	3	B8		Xch	R8	4 bit write
	4	51		JMS		
	5	CO			4 bit write[2]	
	6	20		FLM	PO	load 1010 in Ro 1001 in R_1
	7	A8			A8	
	8	AO		LD	Ro	load 1010 in Ro 1010 in R_1
	9	B8		Xch	R8	4 bit write
	A	51		JMS		
	B	CO			4 bit Write[2]	
	C	A1		LD	R_1	load 1000 in R8 and call
	D	B8		Xch	R8	4 bit write.
	E	51		JMS		
	F	CO			4 bit Write[2]	

HEXADECIMAL			MNEMONIC			TITLE Tsunami Tide II	DATE
PAGE ADR	LINE ADR	INSTR	LABEL	INSTRUCTION OPERATION	INSTRUCTION OPERAND	COMMENTS	
2	80	CO		BBL			
	1						
	2						
	3						
	4						
	5						
	6						
	7						
	8						
	9						
	A						
	B						
	C						
	D						
	E						
	F						
	0						
	1						
	2						
	3						
	4						
	5						
	6						
	7						
	8						
	9						
	A						
	B						
	C						
	D						
	E						
	F						