United States Department of the Interior

Geological Survey

Office of Earthquake Studies

Menlo Park, California

An Interrogable Data Collection Node (DCN): A Microprocessor Based System for Collection and Transmission of Low Sample Rate Geophysical Data

By

Reese Cutler*

M.J.S. Johnston

Open-File Report 1981-762

*Cutler Digital Design, 2215 Sun Mor, Mountain View, California

Abstract

A microprocessor-based digital telemetry system for the acquistion of low-frequency geophysical data from remote field sites has been designed and tested. The field unit, referred to hereafter as a data collection node (DCN), is built in modular form for easy selection of operating functions, expansion of solid-state memory and re-configuration for different field requirements. A general purpose version of this DCN that responds to manual or computer generated telephone calls data has collected and transmitted deformation data for several months at a field site near the San Andreas fault. Within the digitization errors these data faithfully reproduce those obtained with the standard U.S.G.S. digital telemetry system. Average power dissipation for this application was less than 500 mw depending on the number of channels monitored.

Table of Contents

Introduction

Data collection systems of many kinds have been designed for the collection, storage, and transmission of both high and low sample rate data. Unusual problems are encounted in the field of earthquake research with the particular requirements for large-scale geophysical data collection. Field conditions can be extreme and maintenence almost non-existent. Few sites selected for geophysical reasons have power or shelter, yet, in order to monitor the slow deformations of the earth's crust accurate, stable and reliable data collection is required over periods of many years. The requirements for high reliability and stability with low power consumption and the need for immediate access to data from widely dispersed arrays of instruments has spawned the development of several low frequency digital telemetry systems (Roger et. al., 1977; Cutler and Johnston, 1978, Nickerson, 1979). These systems allow collection, transmission and reception of data to a common data center.

The most recent and powerful development concerns the introduction of microprocessor based data collectors and receivers. The use of microprocessors permits these systems to replicate the operation of the various existing fixed-function telemetry systems. The important difference is that their functions are software rather than hardware controlled. This allows easy alteration of system parameters and control of both the mode of operation and data collection from a common data collection center.

This note describes such a data collection system, here termed a data collection node or DCN, whose particular characteristic for low frequency data collection are:

1) low power consumption
2) solid state memory for high reliability
3) modular hardware design for easy adaption to a new collection requirement and easy field repair (e.g., an increase in memory in increments of 2048 sixteen bit data can be accomplished by plugging extra memory modules into the communication bus.
4) input ports for up to 15 channels of analog data and one channel of 16 bit parallel digital data.
5) compatability with telephone and radio telemetry for one or two-way communication and data flow to a base operator or computer.

Figure 1 shows a block diagram of this system. Although hardware meeting the functional requirements listed here has existed for some time, only recently have dramatic reductions in power consumption, size, complexity, and cost of microprocessors made possible the widespread use of versatile telemetry with geophysical field instrumentation.

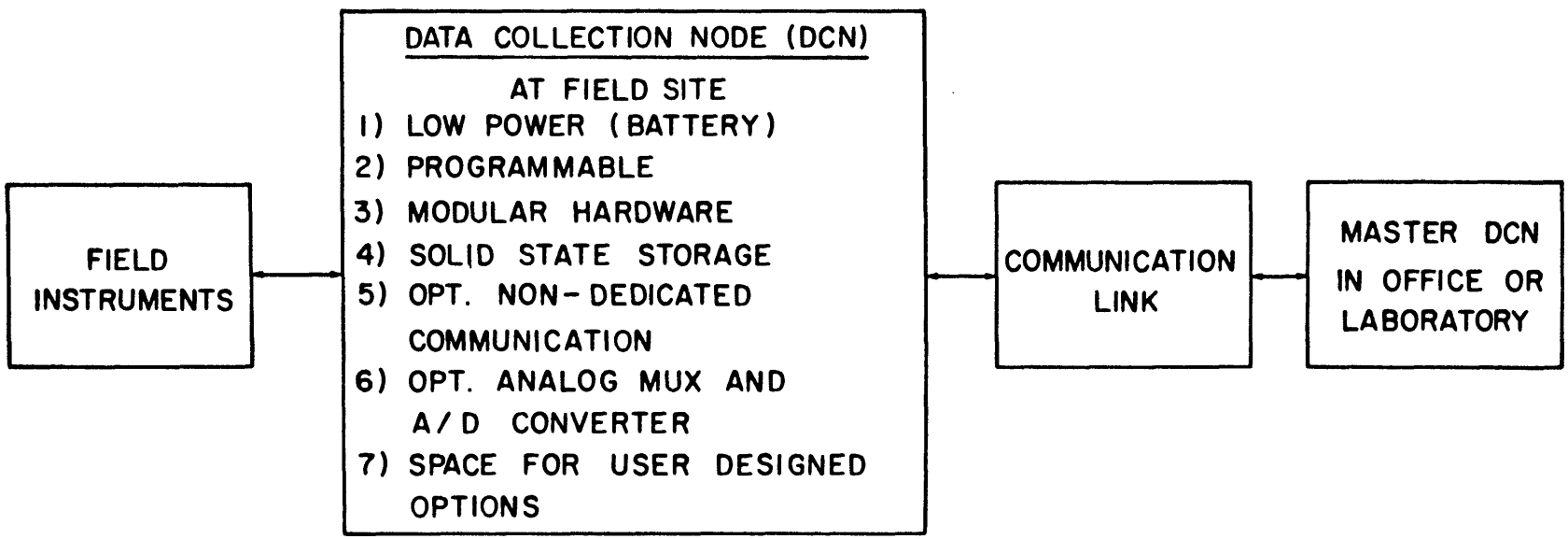


Figure 1: Block diagram showing layout and design requirements of a data collection node (D.C.N.) for geophysical data collection.

DCN Design Considerations

The fundamental units of the D.C.N. are displayed in Figure 2. Modularity is accomplished with the use of a common communication bus. All functional parts are grouped on modules that plug into the bus and have access to all control and data information. Because of the low power requirements of available components, the power supply module contains 5V rechargable batteries with a 2 amp-hr capacity which will drive the device, in normal operation, for well over a year. The computer module presently used is a COSMAC CDP1802. Control programs are stored in non-volatile read-only-memory (R.O.M.'s) in the program module while random-access memory (R.A.M.'s) provides expandable solid state data (typically in units of 4096 8-bit data) storage in the data storage modules. Other necessary circuitry for bus termination, internal clock control, etc. is included in a separate control module.

Optional modules that can be added in order to tailor the system to a particular field application include:

1) an analog input module which contains a multiplexer to expand the number of analog input channels and an analog-to-digital converter.
2) a digital input module to allow the acceptance of digital field data.
3) a switched power supply module which provides current to attached devices only when it is required in order to reduce the total power dissipated.

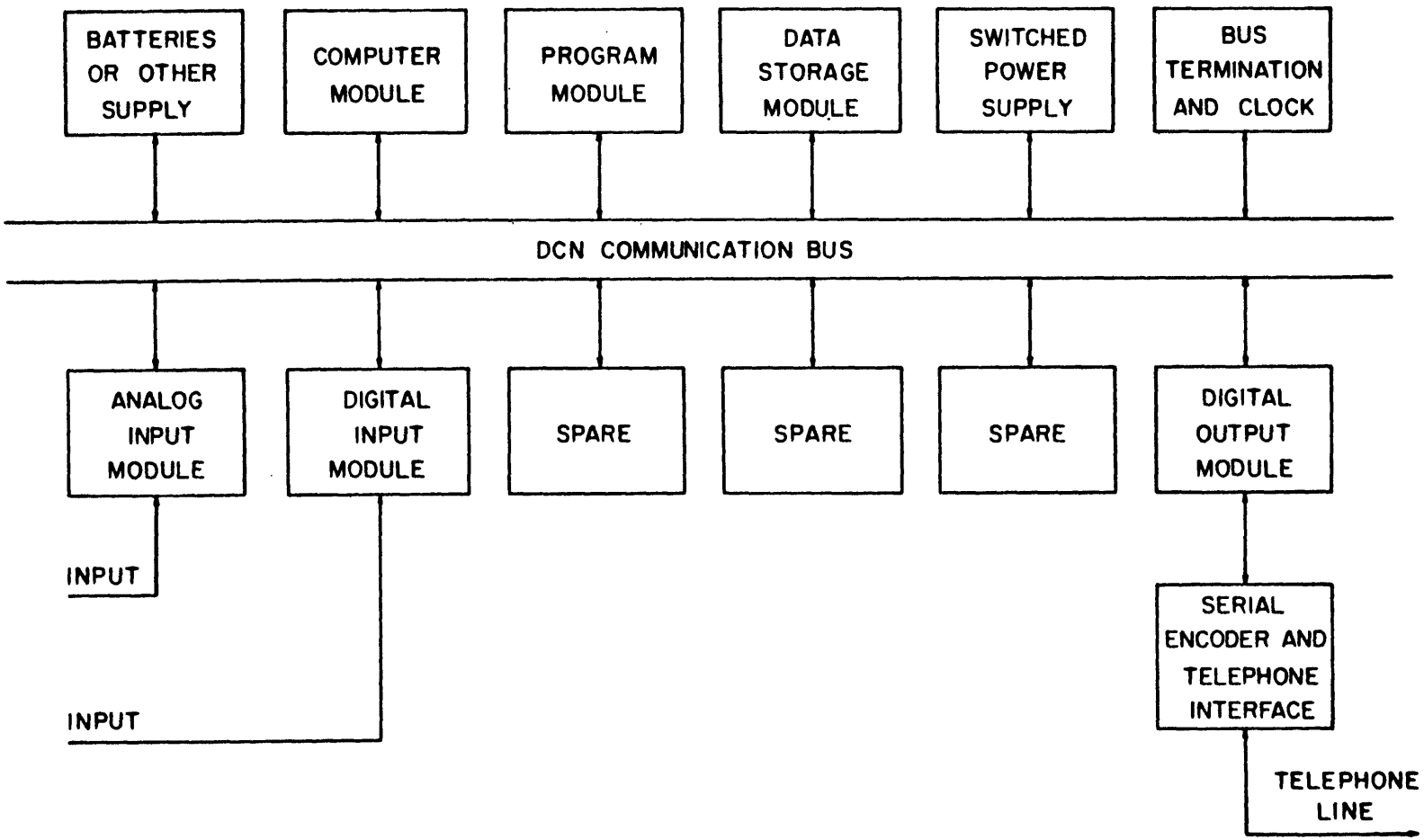


Figure 2: Block diagram showing the modular units of a D.C.N.

4) a digital output control module which controls an input/output communication link and if necessary, controls the operation of the field instrumentation.

These options, or otners that might be needed, can be simply added at any of the many parallel inputs to the communication bus. One example might be the addition of more on-site solid-state memory to provide insurance against the loss of the communication link for an extended period of time. Another example is the addition of specialized programs in a ROM module to do real-time data analysis or testing.

In summary, customizing a D.C.N. for a particular field application requires:

1) Definition of the functions required. For example, on receipt of a computer-controlled phone call, the D.C.N. might be required to switch on a number of instruments, take a series of measurements, check these measurements for previously identified anomalous behavior, determine a mean value and transmit this value back to the base computer.

2) Selection of the appropriate set of modules to provide these functions. Note tnat the program module may require the addition of a special purpose program to several of the general purpose data collection programs. In fact, each particular application will probably have a particular program module.

Application of the DCN to Tilt and Strain Data Collection

Following prototype development of this system (Roger et. al., 1978) a version of the DCN configured for either manual or automatic call-up and data transfer was built and operated for several months collecting tilt data at a site near the San Andreas fault. The tiltmeter is a liquid level mercury type. It's two orthogonal components are 5 m long and are orientated in directions N 73 E and N 17 W respectively. The tiltmeter location is 37.79°N, 122.235°W. This instrument is presently monitored with standard U.S.G.S. low frequency digital telemetry (Rogers et. al., 1976) so that it was possible to check the operation of the DCN by comparing data obtained with both systems after transmission to Menlo Park, California.

The block diagram of this DCN telemetry system including the particular module options chosen is shown in Figure 3. The circuitry is described in detail in Appendix A. The computer module uses a standard general purpose analog data collection program which is described in detail in Appendix B and listed in Appendix C. Besides sampling and storing data from up to 16 analog inputs, this program produces averages of the data and stores these data averages in memory. When called by telephone the program controls transmission of a fixed amount of data. In this case parameters are set in a look-up table to allow selection of:

1) the number of analog channels to be sampled.
2) the number of seconds per sample period.
3) the number of sample periods over which the averages is performed.

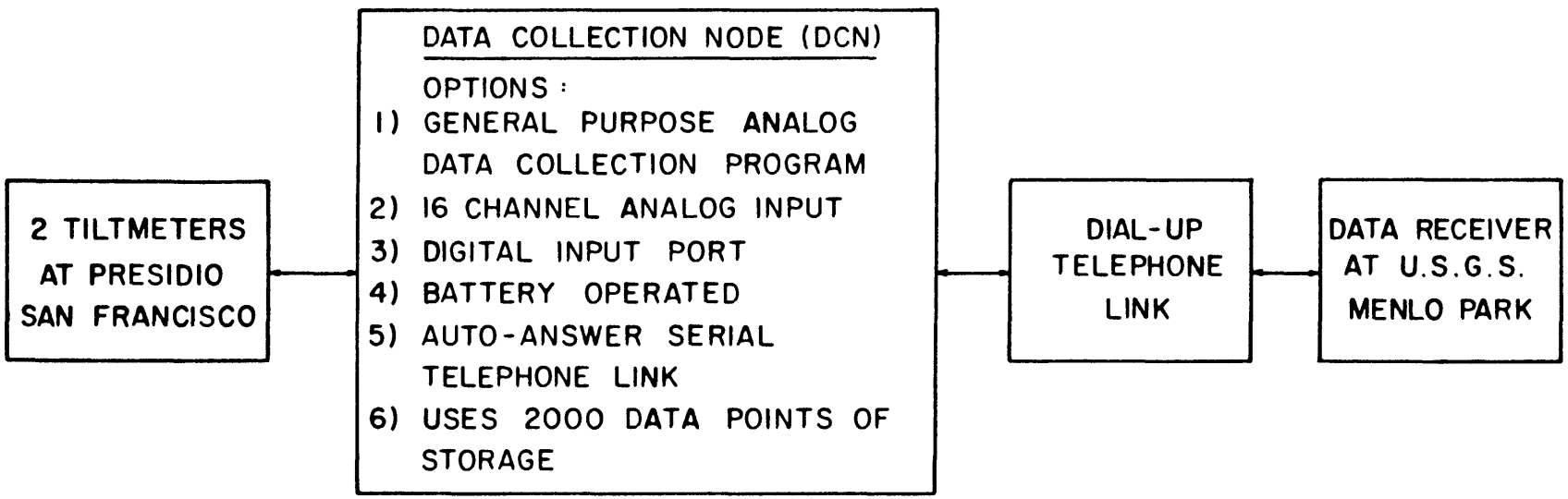


Figure 3: Block diagram of D.C.N. telemetry system and module options chosen for telemetry test at Presidio tiltmeter site.

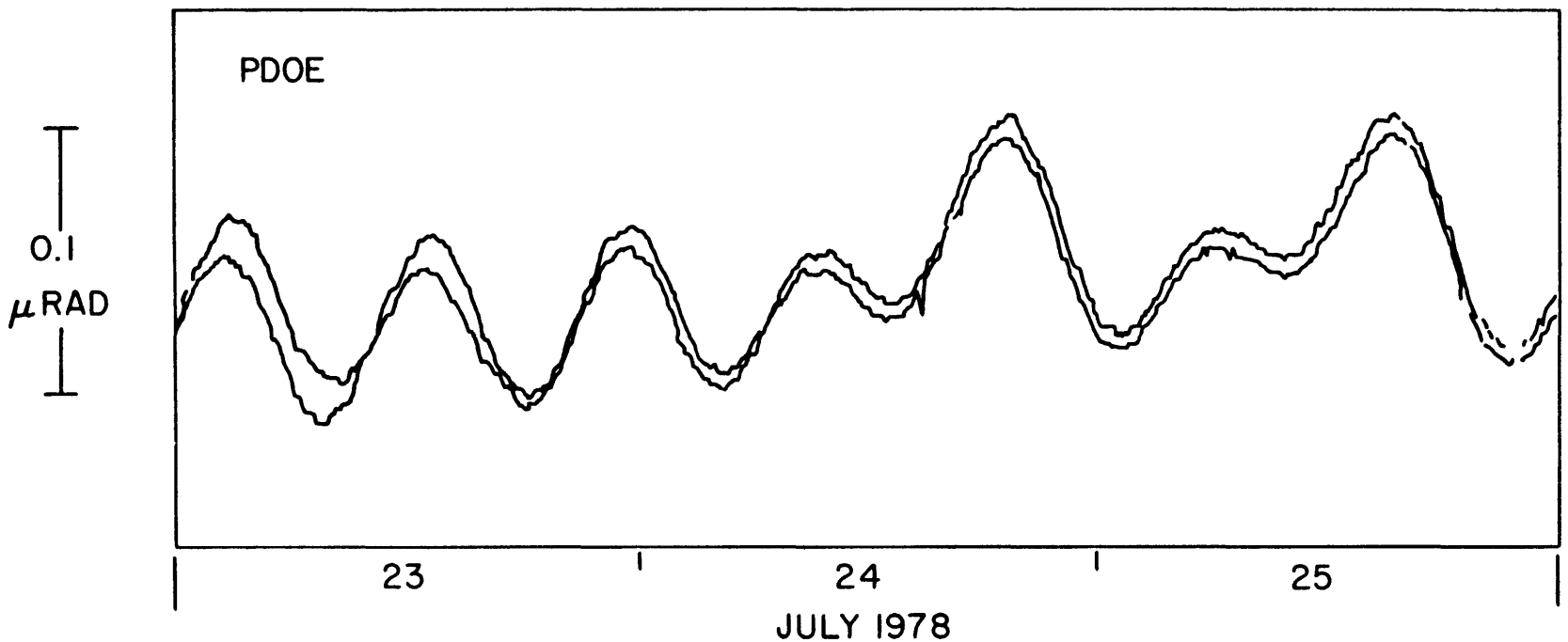


Figure 4: Detailed 3-day comparison between the U.S.G.S, digital tetlmetry system and the D.C.N. telemetry system. Samples were taken every 10 minutes with both systems. The noise on the data is least-significant-bit-error. The traces are offset by 0.01 uradian to allow comparison.

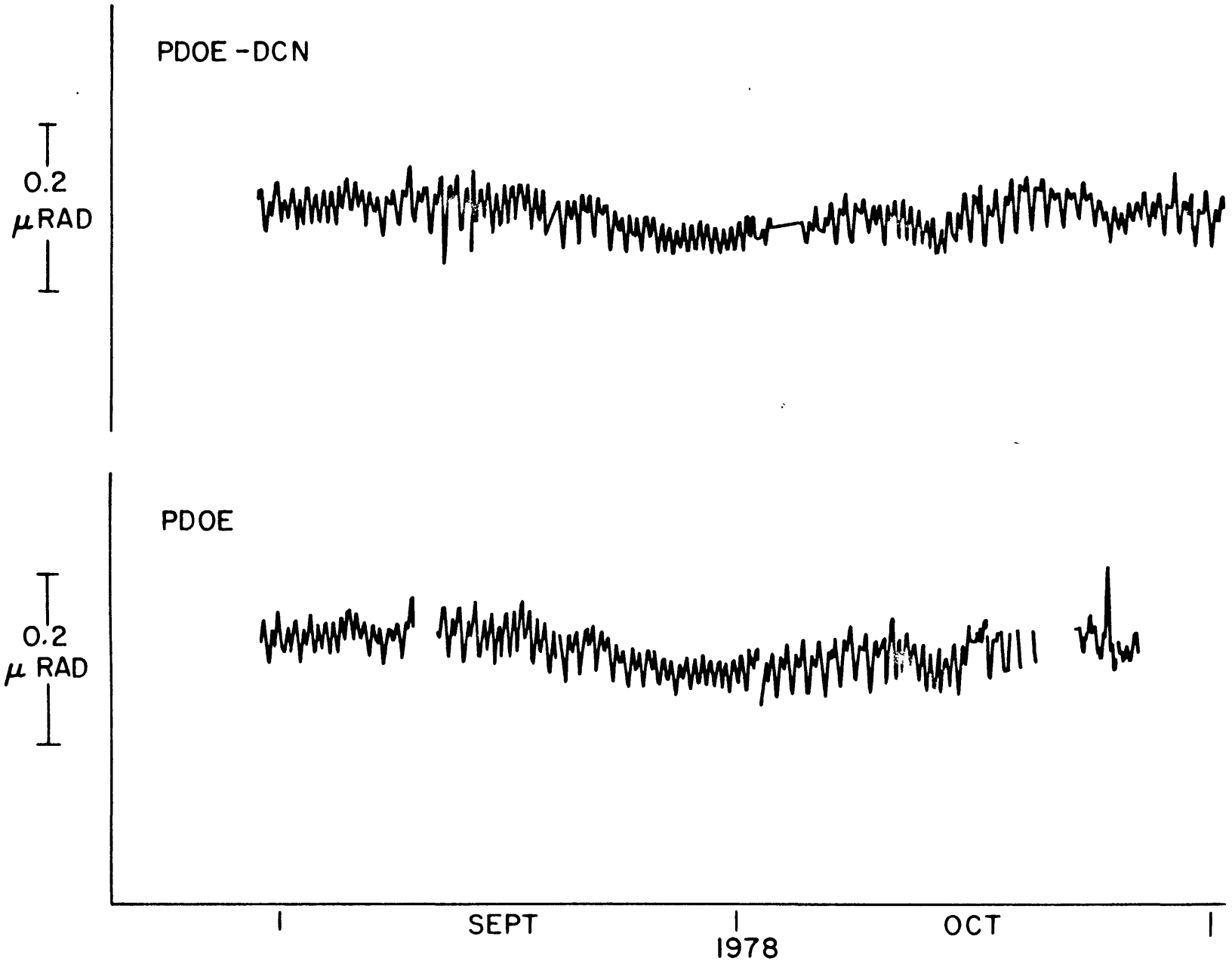


Figure 5: Two month comparison between hour averages form the U.S.G.S. digital telemetry system those from the D.C.N. telemetry system.

4) the number of raw data samples to be transmitted.

5) the number of averages to be transmitted.

Figure 4 shows three days of individual 10-minute data samples from the tilt component PDOE as recorded by the standard U.S.G.S. low frequency telemetry (lower plot) and the DCN telemetry system (upper plot). The records are offset by 0.01 μradians to facititate comparison. The periodic character of the data is of course due to the earth tides.

Figure 5 shows a longer term comparison between the two systems. Hour averages computed by the DCN from the raw data and transmitted to Menlo Park are shown in the upper plot. The lower plot shows hour averages computed from the data individually transmitted to Menlo Park with the standard U.S.G.S. telemetry.

References

Cutler, R., and Johnston, M.J.S., 1978, A Dial-up telmetry Systen for Low Frequency Geophysical Data, Trans. Am. Geophys. Un., 59, 1131.

Nickerson, R.F., 1979, Cross-A datalogging and telemetry system. Trans. Am. Geophys. Un., 60, 889.

Roger, J., Cutler, R. and Varon, M., 1978, A Prototype Design for Microprocessor Based Digital Telemetry Transmitter for Low Frequency Data, U.S. Geological Survey Open-File Report, 78-674.

Roger, J., Johnston, M.J.S., Mortensen, C.E., and Myren, G.D., 1977, A multichannel Digital Telemetry System for low Frequency Geophysical Data, U.S. Geological Survey Open-File Report 77-490

Figure Captions

Figure 1: Block diagram showing layout and design requirements of a data collection node (D.C.N.) for geophysical data collection.

Figure 2: Block diagram showing the modular units of a D.C.N.

Figure 3: Block diagram of D.C.N. telemetry system and module options chosen for telemetry test at Presidio tiltmeter site.

Figure 4: Detailed 3-day comparison between the U.S.G.S. digital tetlmetry system and the D.C.N. telemetry system. Samples were taken every 10 minutes with both systems.

Figure 5: Two month comparison between hour averages form the U.S.G.S. digital telemetry system those from the D.C.N. telemetry system.

APPENDIX A

CIRCUIT DETAILS

Tne Dcn Bus (refer to logic drawing 1)

Communication between all modules of the DCN is over a set of 72 electrical connections which are called, collectively, the DCN communication bus. Eacn of the 72 connections is made available to each module. For the purpose of this aescription, the 72 lines can be divided into the following catagories: power and ground, normal data transfer, interrupt and external flags, bus control and direct-memory-access, service control, and special microprocessor lines.

Two lines are reserved for the nominal +5V supply, and a corresponding 2 lines are reserved for grounds. Six lines are reserved for the switched power supplies: two for +15VSW, two for-15VSW, and two for +5VSW. These six lines are only valid if there is a switched power supply module, and if it has been turned on.

At any time in tne normal operation of the DCN one module is designated as the bus master. This module is responsible for setting up the correct bus control signals for data transfers. At present, the only module capable of bus mastership is the computer module.

Normal data transfers proceed as follows. Read operation: BMRDL is asserted-low, and theproper address lines are asserted (BAD15 through BADØ). Next, BTPB is asserted-hign. For the duration of BTPB the addressed location should assert its contents onto the data lines BD7 through BDØ. When BTPB goes low the read operation ends. Write operation: BMWRL is asserted-low, the proper address lines are asserted. At the same time that BTPB is

asserted-high, the bus master asserts the date lines BD7 through BDØ to the value that is to be written. Half way through BTPB, BMWRL is de-asserted. Normally this change of state is used to load the value on the data lines into the addressed location. The write operation ends with the de-assertion of BTPB.

To simplify the decoding for input and output devices, the top 256 bytes of the address space are reserved for I/O. There is a bus signal that indicates addressing of this block of memory (BDEVL). Input and output devices use this signal to simplify their address decoding task. BDEVL is asserted-low, asynchronously, whenever the eight high order address lines are high.

There are four external flags associated with the CDP1802 microprocessor: EF1L, EF2L, EF3L, and EF4L. They are normally high and are active-low. When more than one device is allowed to drive these lines, the devices in question should not actively hold the flag line in question is a de-asserted state (high)--there is a resistor pull-up to do this. For an example of proper interface to the external flags see the analog input module description.

There is one interrupt line (INTL which is active-low) that can be used by any module to initiate an interrupt. As with the external flags, modules should not actively hold the interrupt line in a de-asserted state; there is a resistor pull-up to do this.

To simplify interrupt circuitry on each module there are special control lines for servicing interrupts. The top byte of memory is designated as the interrupt buffer. Writing into this location sets interrupt enable flags. Reading from this location gives access to the state of interrupts, and then

clear the interrupt flags that are on. INTREAD directs interrupt circuitry to assert the interrupt state on the appropriate bits of the data lines. Whenever INTLDL makes the transition from being asserted to being de-asserted (rising edge), interrupt circuitry loads the value of the appropriate data line into an interrupt enable buffer. Finally INTCLR asynchronously clears interrupts, after a system reset, and after interrupt status has been read.

Bus mastership is requested through the use of the daisy-chaned signals BREQIN and BREQOUT, and granted through the use of the daisy-chaned signals BGIN and BGOUT. The computer module is the default bus master, and must reside to the right of all devices requesting bus control, with all intermediate sockets in use. Other devices may request control, and will be granted it with highest priority to the devices physically closest to the computer module.

DMAIL and DMAOL and direct memory access control lines specific to the CDP1802 microprocessor and are available on the bus. For more information see the DCP1802 documentation and refer to the computer module drawings.

"Service control" is a grab bag term to describe the lines that perform various and special bus functions. There is a one meganertz clock (MHZ), from which the whole system timing is derived. There is a line which enables or disables the computer module clock: CLKENL (enables the normal clock when active-low). There is a clock line (XCLOCKL) that can be used to replace the normal computer module clock whenever CLKENL is not asserted. There is a general reset request line, RSTRQL, which causes BRESET and BRESETL to be asserted.

Finally there are seven DCP1802 control lines that are also made available. BSC1 and BSC0 reflect the state of the microprocessor. BN2, BN1 and BNØ reflect the state of an 1802 input/output instruction. BTPA is an 1802 timing pulse, and BQ is the output of an 1802 flip-flop. See the CDP1802 hardware literature, and the computer module description for more information.

BUS TERMINATION AND CLOCK MODULE (refer to logic drawing 2)

This module does many DCN communication bus housekeeping chores: resistor pull-up or pull-down of bus lines, reset circuitry, I/O device decode, interrupt servicing control, one meganertz system clock, and a one second clock with external flag, and interrupt capability.

In general bus lines are either tied to +5V through a 100 Kohm resistor or tied to ground through a 100 Kohm resistor. This is to avoid the possibility that certain lines will be floating, and cause an increase in power consumption, or an illegal logic condition.

A reset request (RSTRQL active-low) shorts the input of a schmidt trigger (loc. C-() to ground, thereby driving BRESET and BRESETL active (high and low respectively). The RC network in front of the schmidt trigger is included to allow switch bounce on RSTRQUL, and to insure that the reset lines are active long enough. This module includes a switch that asserts RSTRQL, so that the DCN can be reset manually.

Input/output decoding is simplified with the generation of BDEVL (loc. B-15), that goes active-low whenever BAD15 through BAD8 are all active-high.

Interrupt service lines INTREAD and INTLDL are only asserted when all address lines are active-high (loc. D, E-9, 12). INTREAD, also requires that

BMRDL be active-low, while INTLDL requires that BMWRL is asserted-low. INTCLR is asserted on the falling edge of INTREAD, and cleared when the first non input/output address is put on the address lines.

There is a one megahertz clock, MHZ (loc. H, I, J-5, 6), which goes on the bus, and which drives a divide by 1,000,000 chain to produce a one second clock. The "one second" flip-flop (loc. G-13) is set once a second. If it is on, it holds EF3L to ground (by opening an analog gate, 1/4 IC5), and if the interrupt enable flip-flop is also on, it holds INTL to ground (by opening two analog gates in series, 1/2 IC5).

The bus request and bus grant daisy-cnain is jumpered to allow other devices to use it.

COMPUTER MODULE (refer to logic drawing 3)

This module interfaces the RCA CDP1802 microprocessor to the DCN bus, and provides bus mastership control.

A BRESETL asserted-low forces the processor into the reset state. The following lines go directly from the bus into tne appropriate CDP1802 inputs: INTL, DMAIL, DMAOL, EF1L, EF2L, EF3L and EF4L (loc. E,F.G-7).

If CLKENL is asserted-low and OXLOCKL (active-low) is high, tnen the microprocessor clock is generated by the selected output of the divider (IC12, loc. H,I-4) which is driven by tne one megahertz system clock MHZ.

If tne bus is controlled by this module (hence, there are no bus requests) all the following CDP1802 signals are asserted onto the DCN bus through tri-state buffers (IC1, 2, 3): BTPA, BTPB, BSC1, BSCØ, BRDL, BMWRL, BN2, BN1, BNØ, and BAD7 through BADØ. The high order address lines need to be latched,

and are also only asserted if no bus request has been granted (uses a tri-state register, IC7, 8). The value of the address lines BAD15 through BAD8 is present on the CDP 1802 address lines during TPA and is loaded into the tri-state register on the falling edge of TPA. An eight bit tranceiver is used (IC4, 5) to allow two way data bus transmission between the microprocessor data bus, D7 through Dø, and the bus data lines BD7 through BDø.

A bus request, BREQIN, active-high causes the bus grant flip flop (loc. A-4, 5) to turn on at the next falling edge of the CDP1802 control signal TPB. The BG is daisy-chained across the bus to the requesting device, and the microprocessor buffers onto the bus are all turned off. The bus grant signal also forces the microprocessor into a wait state. As soon as the bus request input is de-asserted, the bus grant flip-flop is cleared, and the microprocessor regains control of the bus.

PROGRAM MODULE (refer to logcic drawing 4)

The read only memory capacity of this module is 2048 bytes of contiguous storage. The module uses four 512 by 8 bit read only memory packages (IC12, 13, 14, 15). The address lines to these ROM arrays is generated by buffering BAD8 through BADø. Select lines (ROMEN3L through ROMENøL) are generated with the use of four 2 to 4 decorders (IC1, 2). Jumper selection on the module allows for the placement of the read only memory in one of 32 2K address space slots. Notice that if the module is placed in the highest address slot, it does not respond if the very highest 256 bytes are addressed (BDEVL inhibits the decoder chain in this event). Notice also that this module responds only when BMRDL is asserted-low; and the date is placed from the module onto BD7

through BDø only during BTPB.

The bus request and bus grant daisy-chain is jumpered to allow other devices to use it.

STORAGE MODULE (refer to logic drawings 5-7)

There are four functional sections of this 4096 by 8 bit random access memory module: address buffers, address decoder, data tranceiver, and memory array.

Since the address lines have to go to 32 different 1024 X 1 RAM packages (IC1-IC32, logic drawings 6, 7), the bus address lines BAD9 through BADø are buffered (IC38, 39 logic drawing 5, loc. B, C., D-6, 7, 8). The high order address lines are decoded using 2 to 4 decoders (IC33, 34). The module is jumper locatable into one of sixteen 4K slots in the address space of the machine. The memories are enabled during BTPB, and they are inhibited if the 256 byte I/O buffer is addressed.

The data tranceivers (IC36, 37) allow the two way communication between the bus data lines BD7 through BDø, and the local data lines MI7 through MIø and MO7 through MOø. The bus control line BMRDL determines the direction of data flow, and the local enable line RAMEN allows data flow when this module is selected.

The bus request and bus grand daisy-chain is jumpered to allow other devices to use it.

DIGITAL INPUT MODULE (refer to logic drawing 8)

Each digital input module allows the input of sixteen bits of digital information. The module is arranged to allow connection to the sixteen bits

with either screw down terminals, or with dual-in-line sockets. The module also allows access to tne following bus signals through screw down terminals: BQ, EF1L, EF2L, EF3L, and EF4L.

There are two major functions on the module. A series of 2 to 4 decoders accomplishes the address decoding (by taking advantage of the I/O select line BDEVL - IC2, 3). The actual buffer for the digital inputs is made from a tri-state sixteen to eitht multiplexer (IC4, 5).

The module has the option that the digital inputs can be tied up to +5V with 100 Kohm resistors. This allows the digital input to drive the actual inputs with an open collector transistor stage, and not worry about matching logic levels. A special case of this kind of use occurs when the optional resistors are used and dual-in-line switch arrays are inserted into the dual-in-line sockets, making the module a switch register.

Since tne module allows input of 16 bits, but the data lines can only hnadle eight bits at a time, the full sixteen bits of data must be input in byte slices. This also means that each module uses two of the 255 I/O locations available to it. Note: the location of the module in the 255 byte I/O address space is jumper selectable.

The bus request and bus grant daisy-chain is jumpered to allow other devices to use it.

DIGITAL OUTPUT MODULE (refer to logic drawings 9, 10)

The digital output module is really an enlarged version of the digital input module. It allows the user to output sixteen bits with the feature that the user can read the value of the bits that have been output. It means tnat much of the circuitry is the same between digital input and output modules.

There is a sixteen to eight multiplexer (IC4, 5) that makes the output data available to the bus data lines. The address decoding uses a series of 2 to 4 decoders, which are enabled by BDEVL and produce write enable (IOWENL) and read enable (IORENL) control lines. IOWENL enables a write operation into the output register.

The output register is sixteen bits worth of data in four integrated circuits (IC6, 7, 8, 9). The outputs of these registers go to the input multiplexer, the dual-in-line sockets, an the screw down terminals. Since there are sixteen bits in the module and the data lines of the DCN bus can handle only eight bits, this module takes up two I/O locations.

There are two screw down terminals that signal the outside that a new eight bits has been loaded in the register. They are labelled H for the line corresponding to the high order byte, and L for the line corresponding to the low order byte. The linew H or L go active-high after the write operation is completed, and remain high until the module is deselected.

As with the digital input module BQ, EF4L, EF3L, EF2L, and EF1L are also accessable through screw down terminals.

The bus request and bus grant daisy-chain is jumpered to allow other devices to use it.

SWITCHED POWER SUPPLY MODULE (refer to logic drawings 9, 10)

The switched power supply is really just an optional part of the digital ouput module. It uses the least significant bit of the output port to turn on a network of transistors that provides +5VSW, a switched 5 volt supply to the DCN bus. The +5VSW is also directed into a DC to DC converter whose outputs drive tneDCN bus supplies, +15VSW and -15VSW.

ANALOG INPUT MODULE (refer to logic drawing 11)

This part of the DCN can be divided into six sections: the analog multiplexer, the analog to digital converter, the buffer between the A/D output and BD7 through BDØ, the address decoder, the channel select and control logic, and the interrupt logic.

The analog multiplexer (IC16) takes its sixteen inputs form sixteen screw down terminals, or from two dual-in-line sockets (not shown in the logic drawing). Since the multiplexer is only operational when the switched power supply is on, the channel select and enable control linew (CH3B, CH2B, CH1B, CHØB and ENMUXB) are buffered and asserted only when the power supply is on.

The analog to digital converter is preceded with all low pass filter (IC15). The analog multiplexer output goes into the filter, and trhe filter output goes into the analog to digital converter. Since the analog to digital converter is also powered by the switched power supply, its control signal, TRIGB is also buffered and asserted only when power is on.

The digital outputs of the analog to digital converter are made available to the DCN through a sixteen to eight digital multiplexer (IC10, 11). The twelve lines from the converter must be tied through 100 Kohm resistors to ground in order to keep the multiplexer inputs from floating when the switched supply is off. The other four bits of the multiplexer are supplied by a channel register (IC8), that also selects which of the sixteen analog inputs is to be digitized.

The address decoder is enabled by an address in the I/O address range (where BDEVL goes active-low). An array of 2 to 4 decoders (IC3, 4) produce

the write enable (WENL) and read enable (RENL) control lines. This module's address is jumper selectable to any of the 127 two byte slots in the I/O address space. When the DCN attempts to write in either of the two I/O byte locations associated with this module, the value on the bus data lines BD3 through BDØ is loaded into the channel register. Then, if the switched power supply is on, a trigger signal (TRIG) is generated which starts the analog to digital conversion. Since this trigger is not wanted until after the channel register is loaded, an extra flip-flop is necessary (1/2 IC7).

Interrupt and flag circuitry includes three flip-flops and four analog gates. The first flip-flop (1/2 IC5) holds the status of the analog to digital conversion. Whenever this flip-flop makes the transition from not ready to ready, it sets the interrupt flip-flop (IC5, loc. G-12, 13). The RDY control line also enables an analog gate (IC1, loc. I-14) which asserts an active-low on the bus flag line EF3L. The interrupt is passed to the bus interrupt line, INTL, if the interrupt enable flip-flop (IC7 loc. H-13) is also set. This is accomplisned by opening the two analog gates (IC1 loc. H-14, 15) to short INTL to ground. Finally, special bus interrupt control lines, INTREAD, INTCLR, and INTLDL allow the processor to simply read and clear the interrupt bit (in this case from BD6), and allow the processor to set the interrupt enable bit (again from BD6).

COMMUNICATION MODULE (refer to logic drawing 12)

Communication on the telephone is accomplished using a telephone data access arrangement (CBT or 1001D). It is a standard phone interface whih

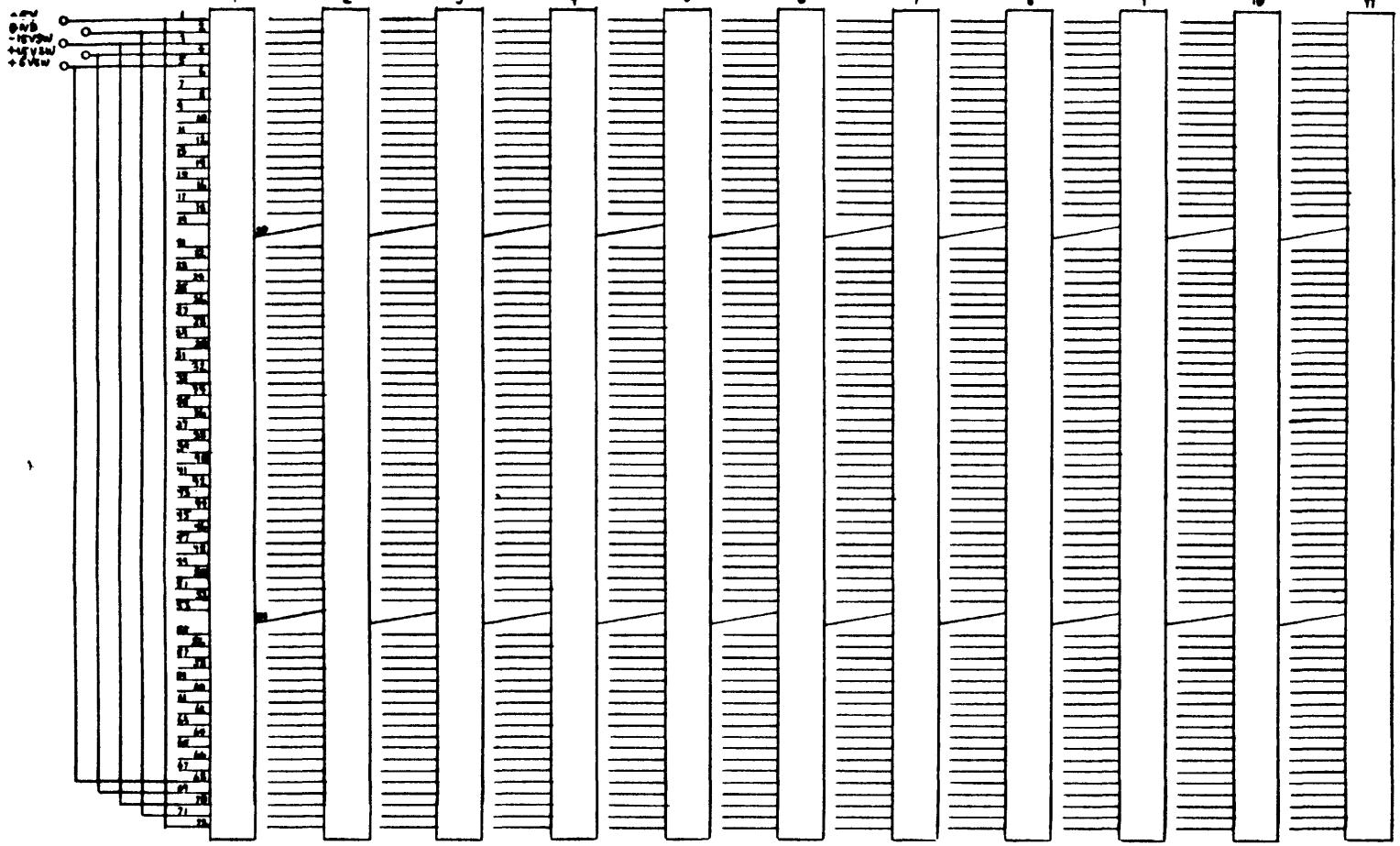
draws no power when not in use. This module interfaces with the DAA on one side and a digital output module on the other. Functionally there is a parallel to serial converter, a voltage controlled oscillator (VCO), a standby DAA power supply, a ring and off-hook detector, and an off-nook request driver.

When the control signal XMIT (which enters the module through a screw-down terminal) goes active-high, it turns on a trigger oscillator. This oscillator keeps requesting a transmission from a parallel to serial converter module (Larse Send). When tne status output of this module indicates that the transmission has begun, the trigger oscillator turns off. Parallel input to the parallel to serial converter comes from a digital output module and connects through a set of dual-in-line sockets. The output of the converter goes into a VCO (see USGS open file report α for more complete details of the oscillator, or see drawing 13). The outputs of the VCO ago directly to the DT and DR inputs of the data access arrangement. The VCO and the parallel to serial converter are powered by the DCN switched power supply.

Tne DAA stanaby power supply is provided to allow ring detection while the DCN switched power supply is no on. Three 7.8 volt NiCad batteries are used. One of tne batteries has a center tap installed, so that when in series the three are configured as a $\pm$ 11.7V supply. A simplified battery configuration is shown in the drawing *EFGH-13, 14). This battery arrangement, through diodes D1 and D4, insures the DAA power supplies $\pm$ V2 at $\pm$11V. If the switched powersupply is on, the NiCad batteries are recharged, and $\pm$V2 goes to about $\pm$13.6V.

If the DAA is receiving a telephone call, the RI output of the DAA will be switching frm an open state to a -V2 state at a frequency of 40 hertz for two

seconds out of every six seconds. This signal is translated into CMOS levels with the resistor-transistor network (R8, R9, R10, Q2 loc. C-1, 3). The series of one-shots insures that the right signal is of adequate frequency and duration to be a ring and not a line transient. If so, the off-hook flip-flop (IC2 loc. D10) is set. This action causes another resistor-transistor network (ABC-13, 14, 15) to assert to -V1 the two DAA control signals OH and DA, which opens the telephone communication and connects the DT and DR inputs to the telephone line. Finally, the DAA will respond with another control signal, CCT, which assures that the connection operation is complete. This signal is shifted to CMOS signal levels and gated wtih the output of the off-hook flip-flop to give the status signal TRDYL. When this line goes active-low, it means that tne communication link has been established and transmision can begin.



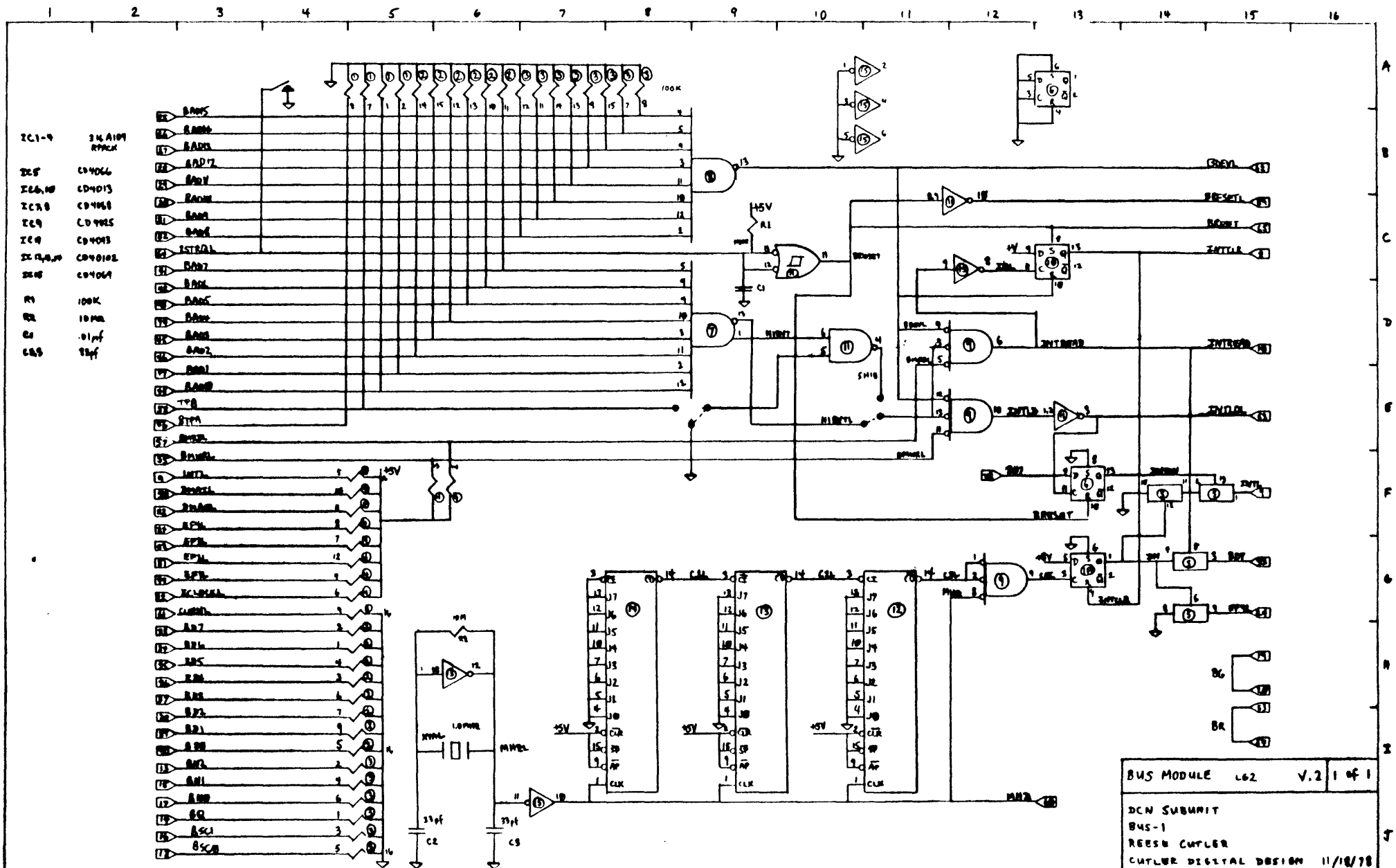
SOCKET PIN DEFINITIONS

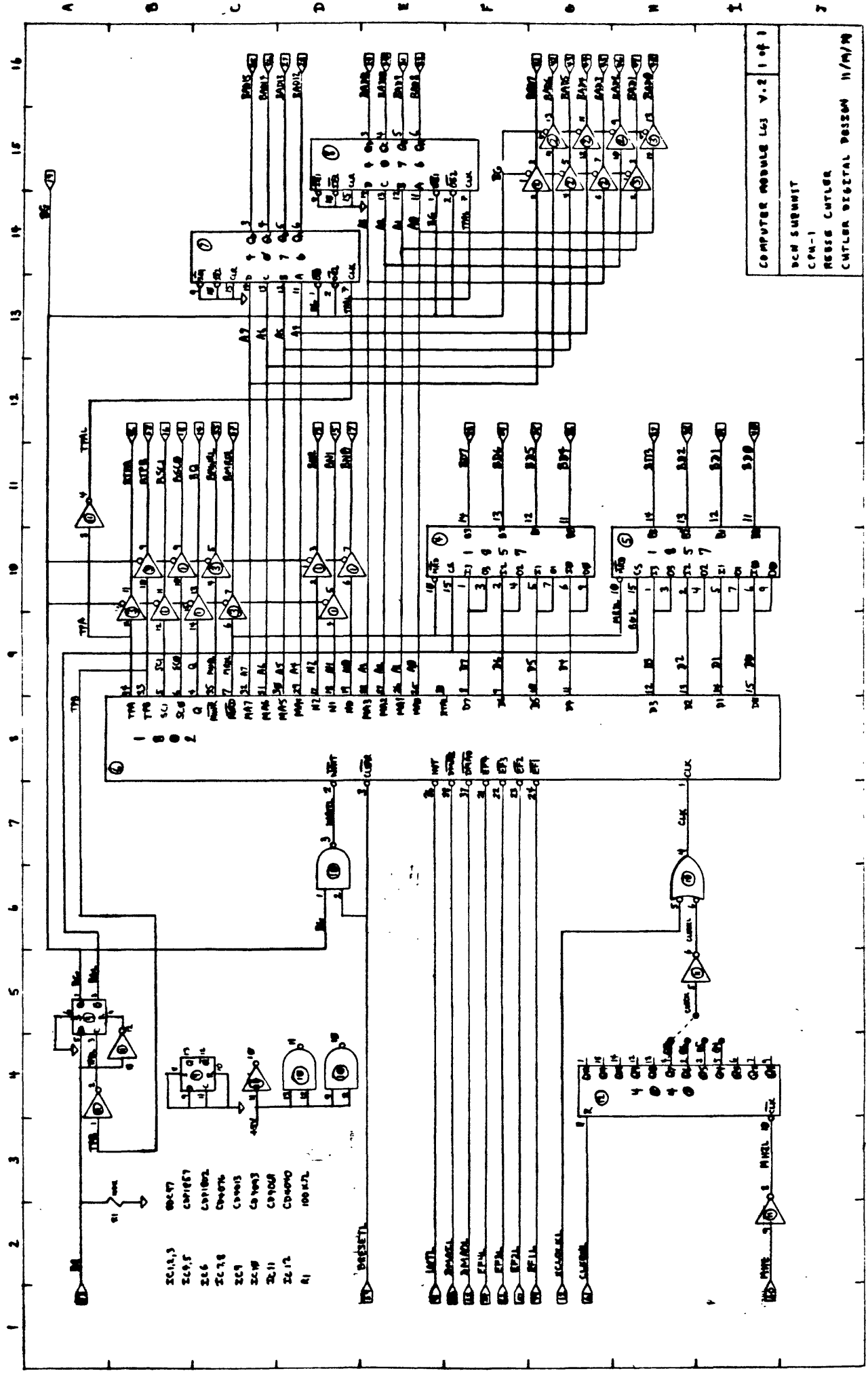
1	+5V	GROUND	2
3	-15VSW	+15VSW	4
5	+5VSW	—	6
7	—	INTCLR	8
9	INTL	INTREAD	10
11	—	XCLOCKL	12
13	BN2	BQ	14
15	BN1	BSC1	16
17	BN0	BSC0	18
19	BSOUT	BSIN	20
21	—	EF3L	22
23	DMAOL	EF4L	24
25	BAD15	BAD14	26
27	BAD13	BAD12	28
29	BAD11	BAD10	30
31	BAD9	BAD8	32
33	BD7	BD6	34
35	BD5	BD4	36
37	BD3	BD2	38
39	BD1	BD0	40
41	BAD7	BAD6	42
43	BAD5	BAD4	44
45	BAD3	BAD2	46
47	BAD1	BAD0	48
49	EF1L	DMAIL	50
51	EF2L	—	52
53	BREQEN	BREQOUT	54
55	BMWRL	BTPA	56
57	BMRDL	BTPB	58
59	BRESETL	MHZ	60
61	CLKENL	BDEVL	62
63	INTLDL	RSTRQL	64
65	BRESET	—	66
67	—	+5VSW	68
69	+15VSW	-15VSW	70
71	GROUND	+5V	72

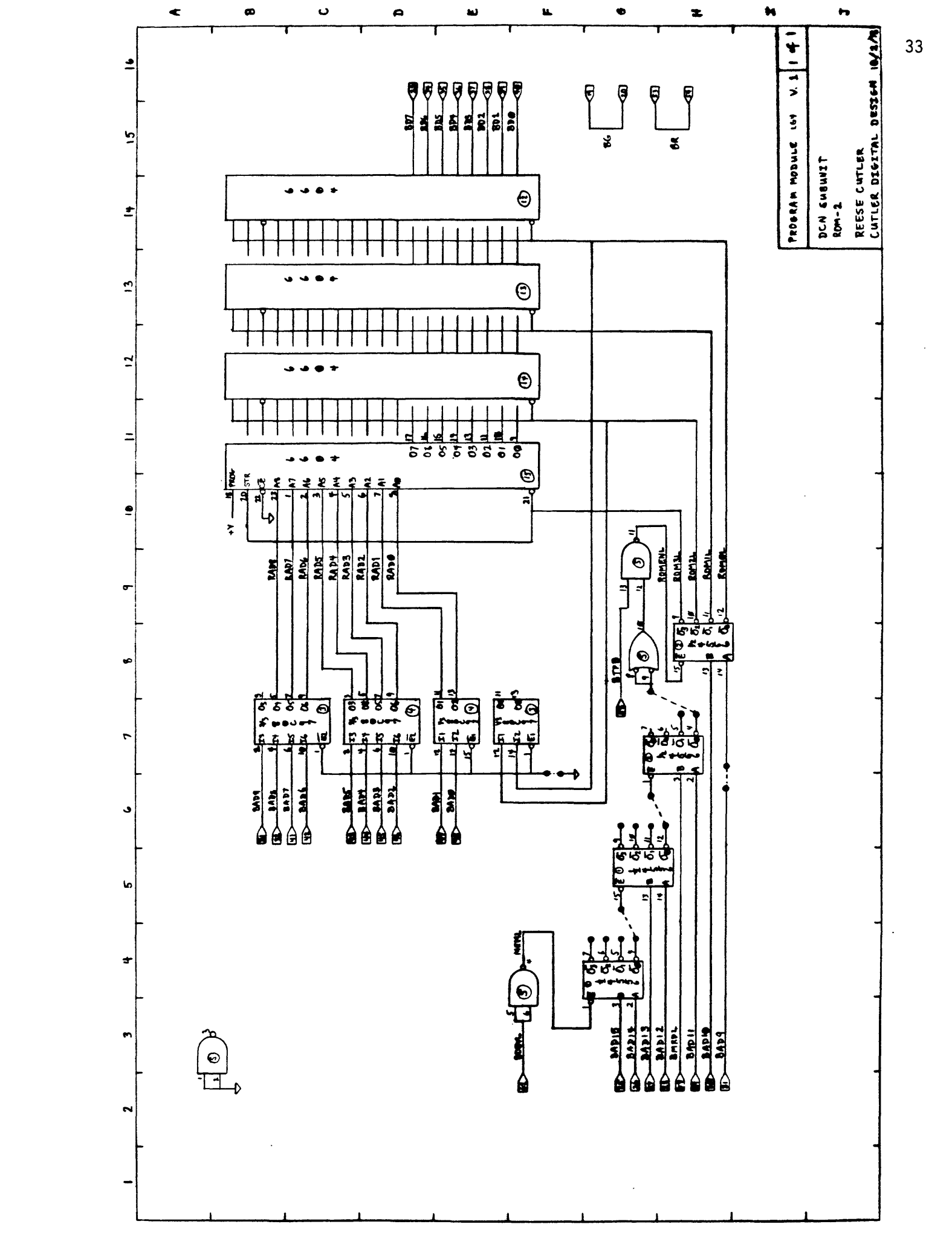
DCN BUS	LGI	V. 1	1 of 1

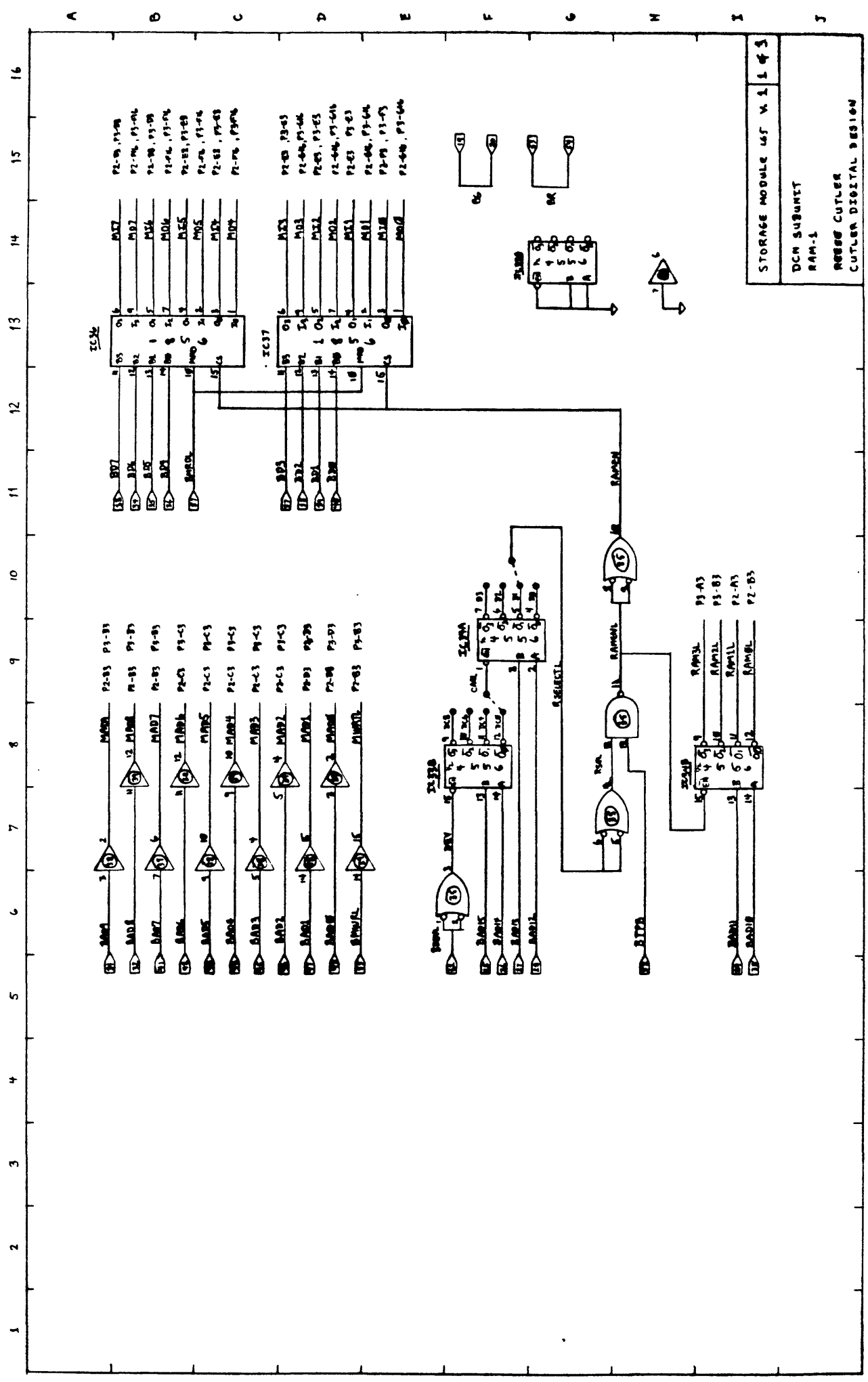
DCN SUBUNIT
BP-1

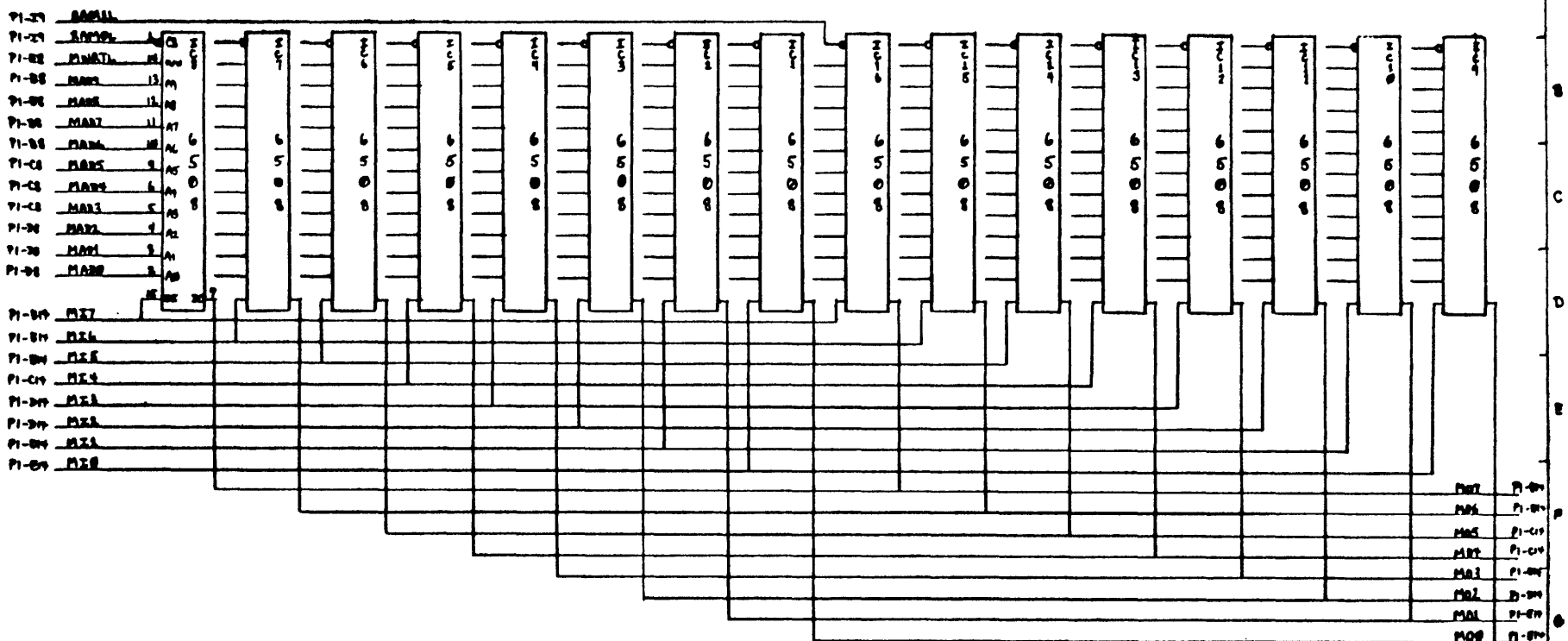
REESE CUTLER
CUTLER DIGITAL DESIGN 10/1/78


IC1-9 3 1K A109 RPACK
IC5 CD4066
IC6,10 CD4013
IC7,8 CD4068
IC9 CD4085
IC11 CD4093
IC12,13,14 CD40102
IC15 CD4069
R1 100K
R2 10MEG
C1 .01mf
C2,3 33pf
+5V
100K
10M
1.0MHZ
33pf
33pf
BUS MODULE L62 V.2 1 of 1
DCN SUBUNIT
BUS-1
REESE CUTLER
CUTLER DIGITAL DESIGN 11/18/78


COMPUTER MODULE (CM) V.2
DCM SUBUNIT
CPM-1
REESE CUTLER
CUTLER DIGITAL DESIGN

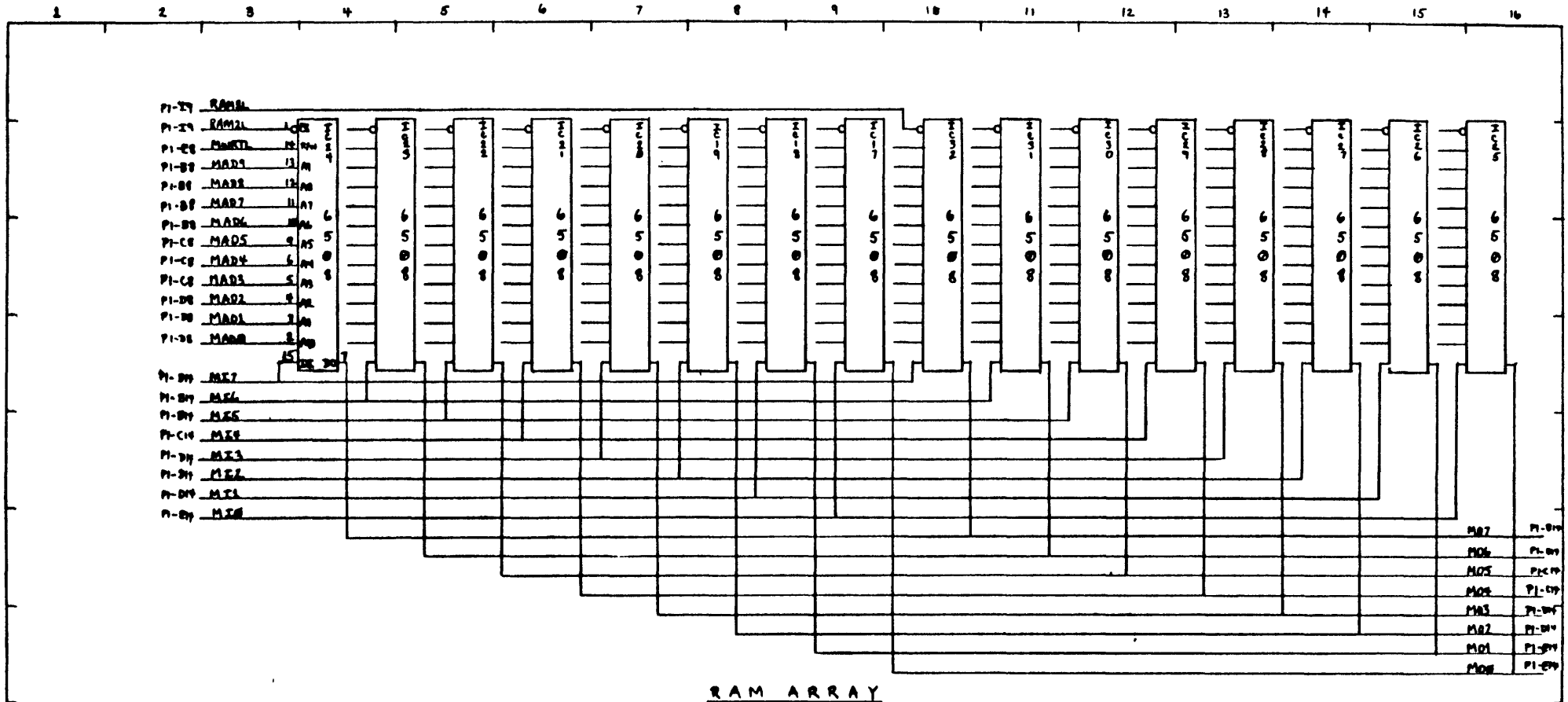

PROGRAM MODULE 1&V V.1 1 of 1
DCN 6UBUNIT
ROM-2
REESE CUTLER
CUTLER DIGITAL DESIGN 10/1/76


STORAGE MODULE 4K V1 1 of 3
DCN SUBUNIT
RAM-1
ROGER CUTLER
CUTLER DIGITAL DESIGN



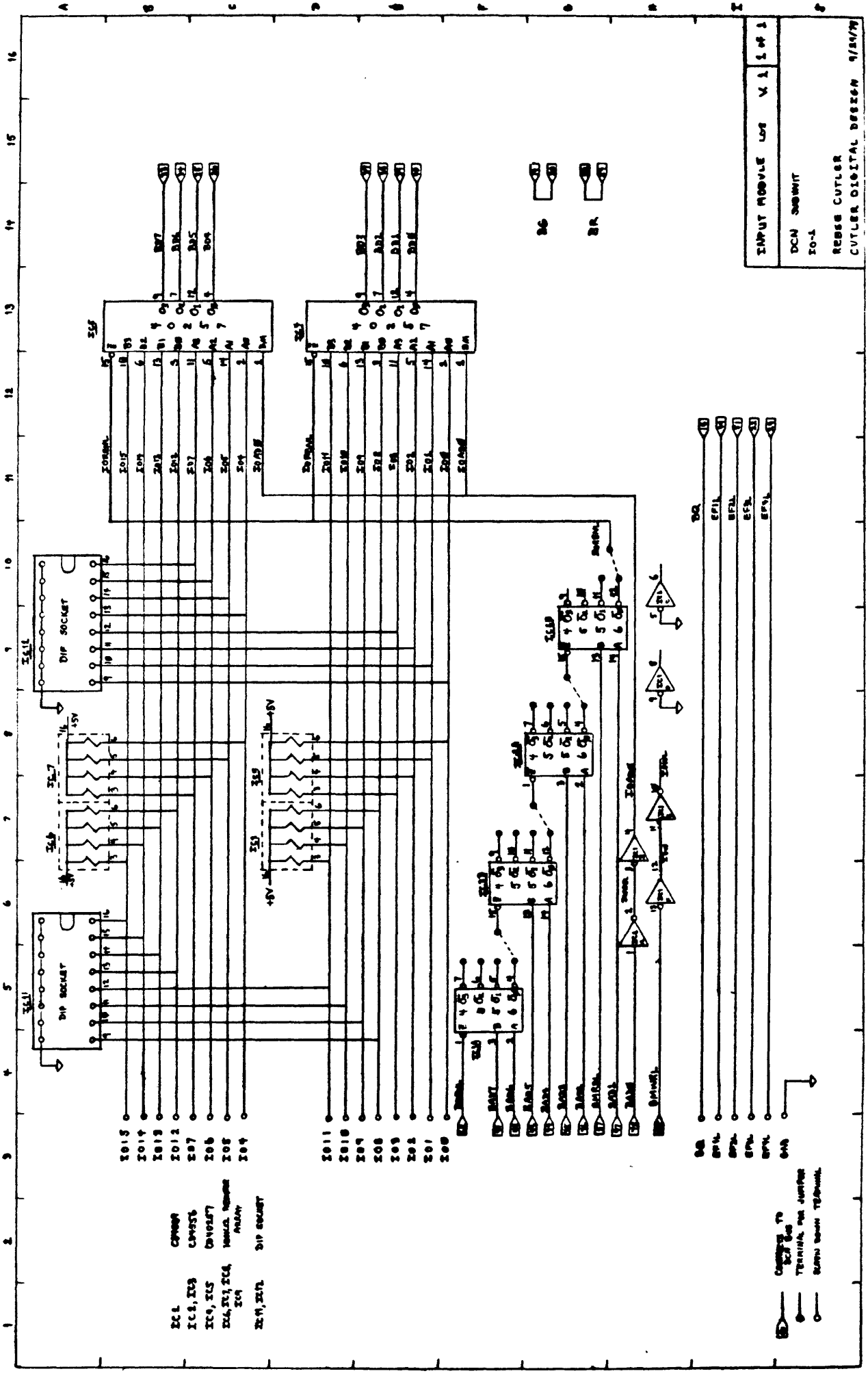
RAM ARRAY

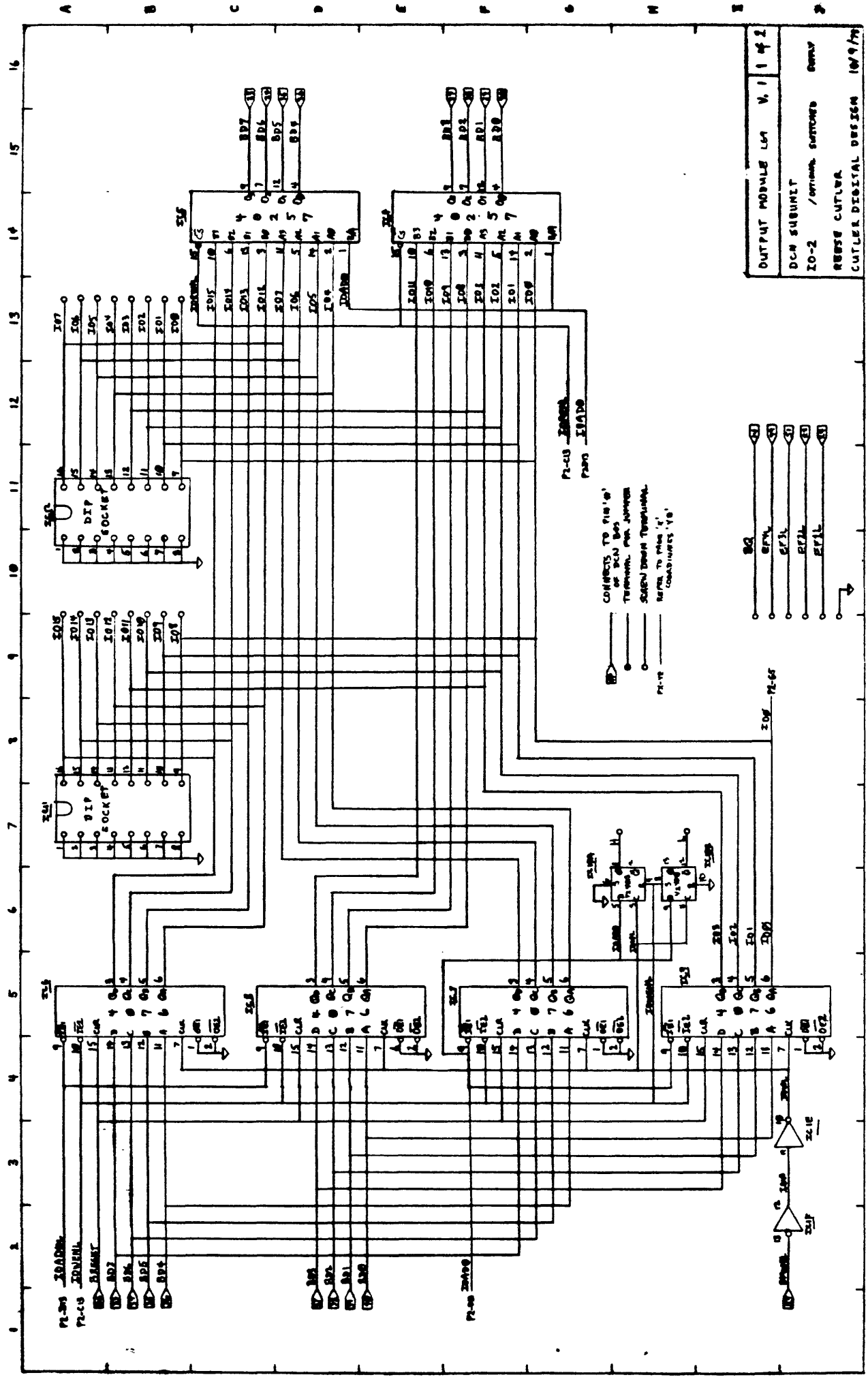
STORAGE MODULE 4K	V. 1	2 of 3
DCN SUBUNIT RAM-1		
REESE CUTLER CUTLER DIGITAL DESIGN		

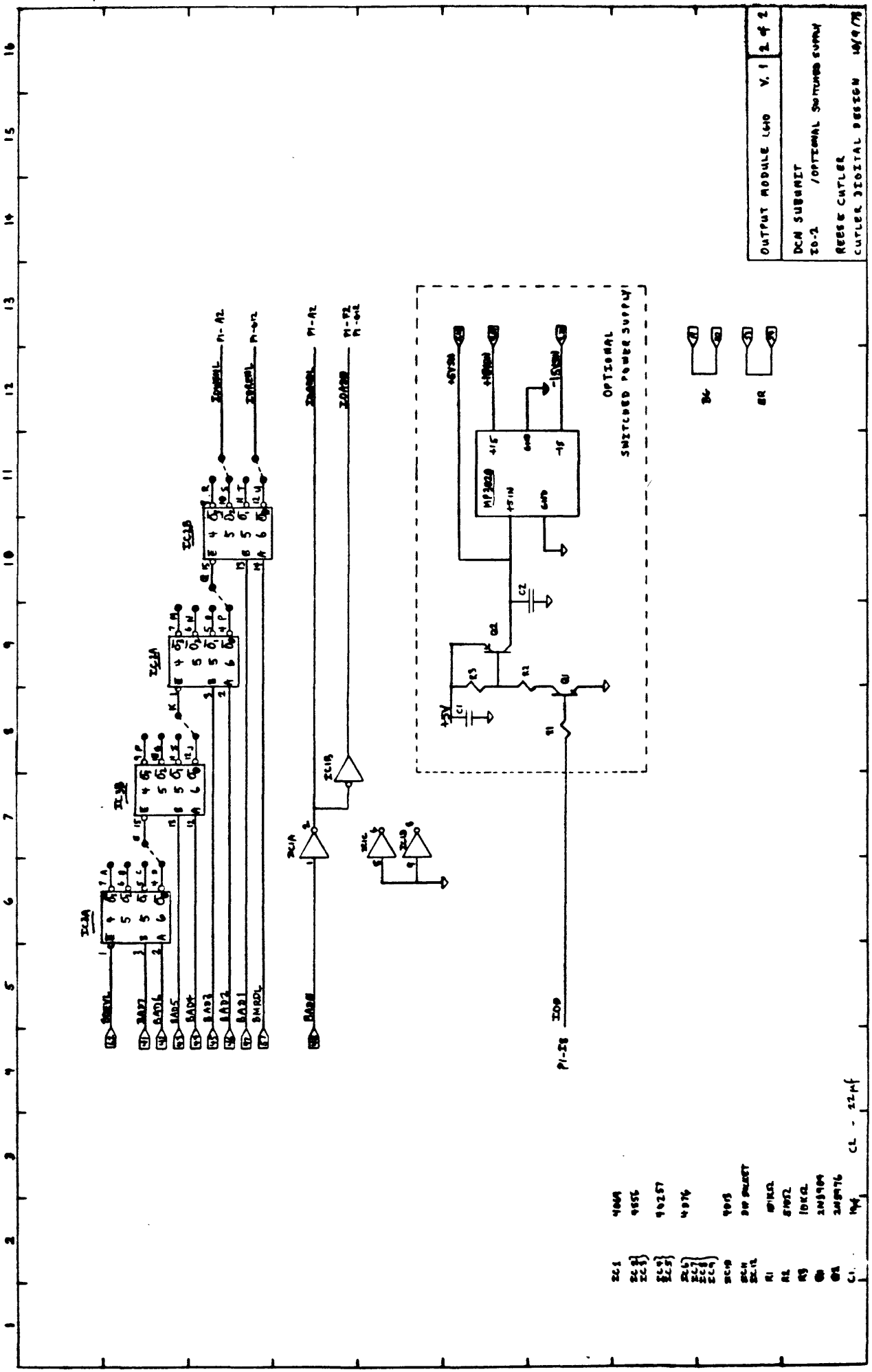


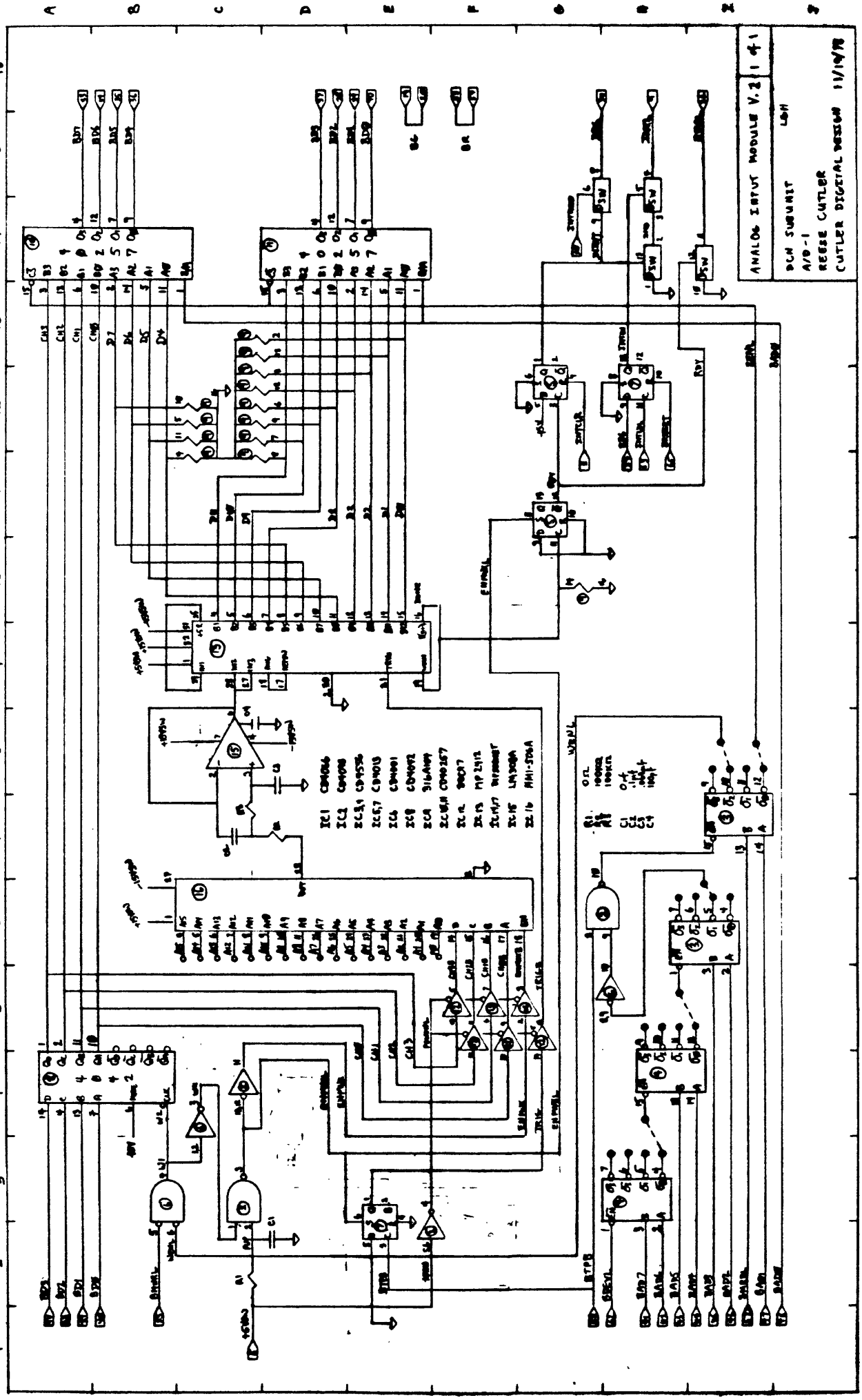
RAM ARRAY

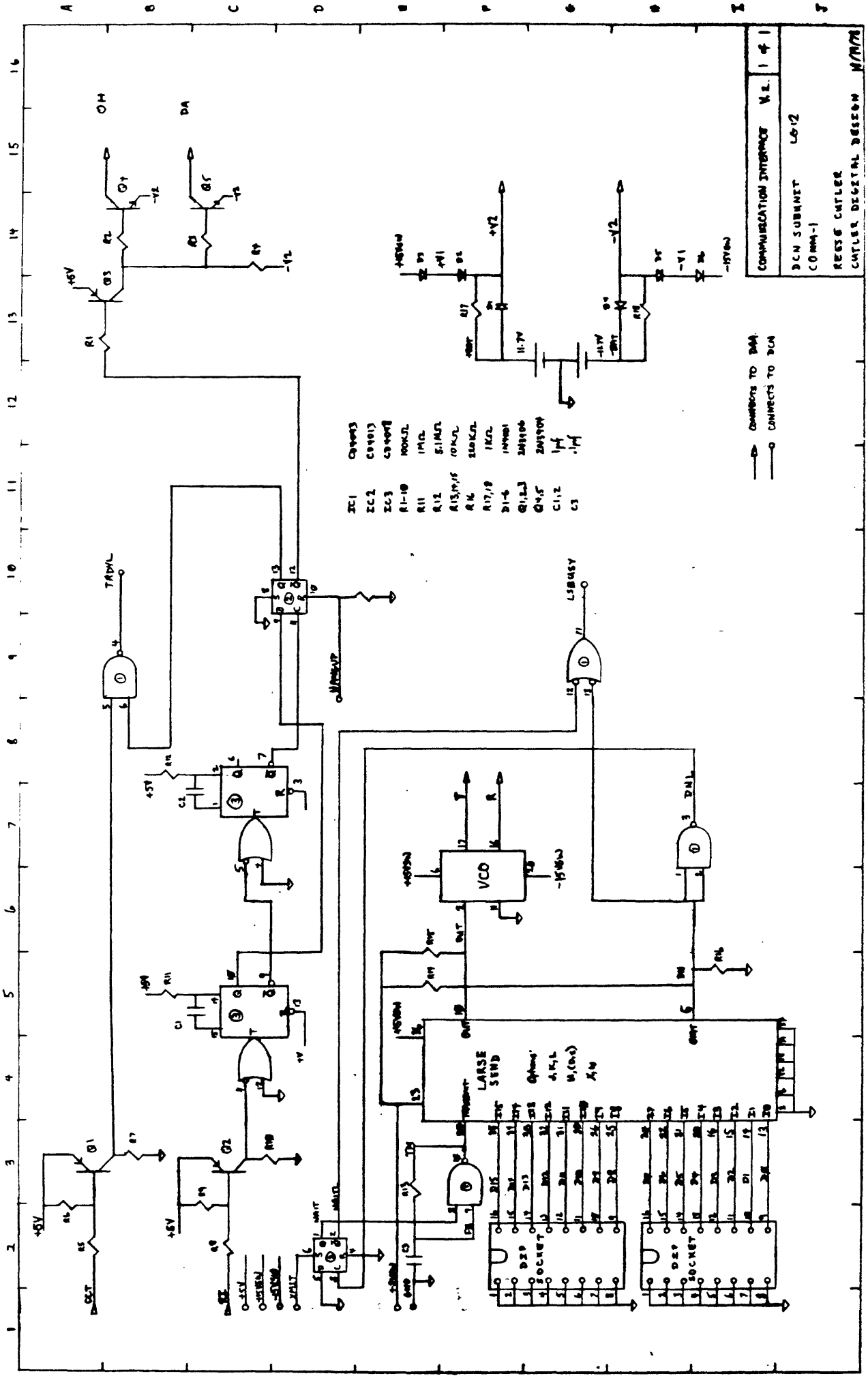
STORAGE MODULE LG7 V. 1	3 of 3
DCN SUBUNIT RAM-L	
REESE CUTLER CUTLER DIGITAL DESIGN	

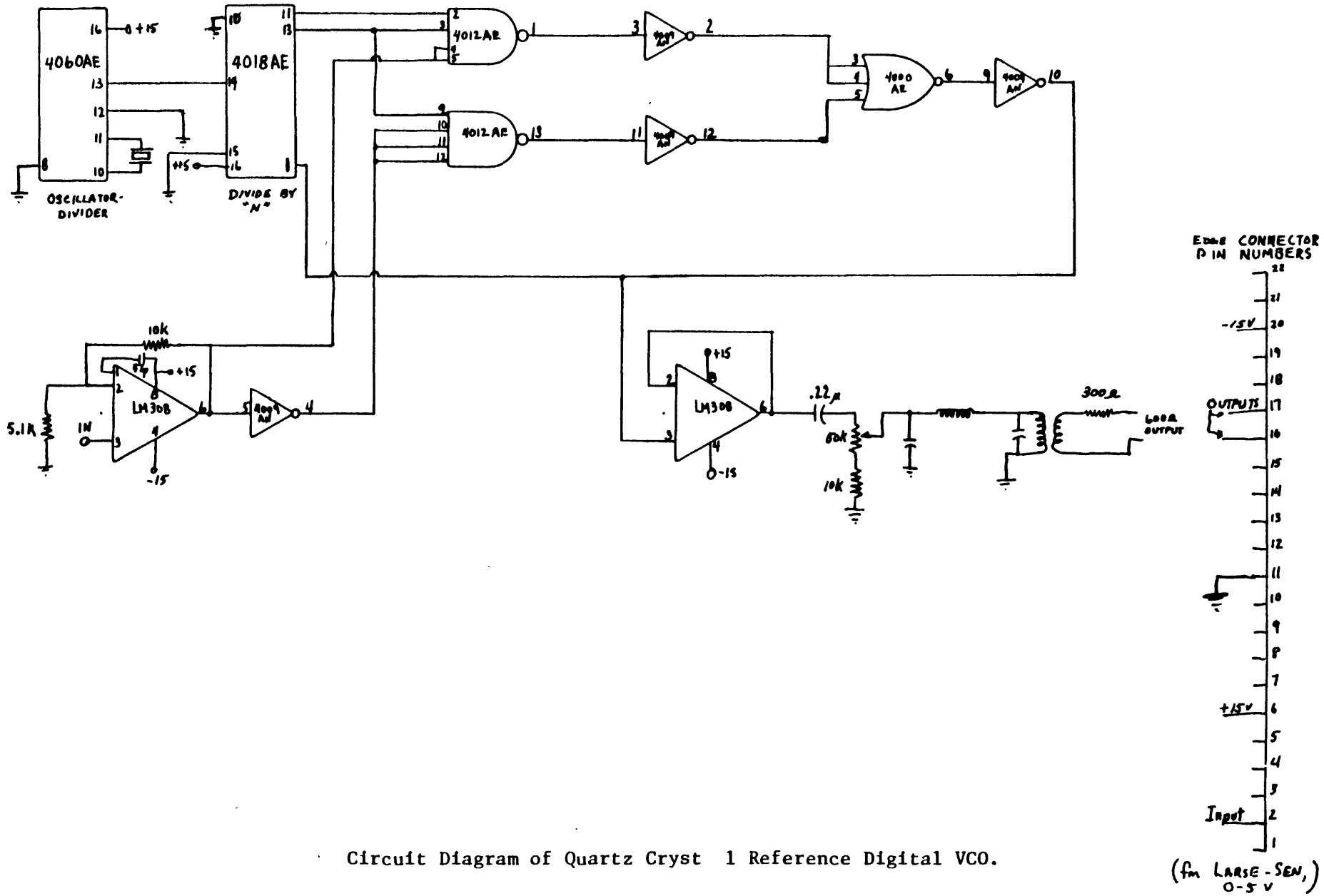

INPUT MODULE
DCN 308417
I0-1
REESE CUTLER
CUTLER DIGITAL DESIGN 9/24/79
DIP SOCKET
DIP SOCKET
+5V
+5V
+5V
I015
I014
I013
I012
I07
I06
I05
I04
I011
I010
I09
I08
I03
I02
I01
I00
DB
EF1L
EF2L
EF3L
EF4L
EF5L
BR


OUTPUT MODULE
DCM SUBUNIT
IO-2
REESE CUTLER
CUTLER DIGITAL DESIGN


OUTPUT MODULE LH0 V. 1
2 of 2
DCN SUBUNIT
IO-2 /OPTIONAL SWITCHED SUPPLY
REESE CUTLER
CUTLER DIGITAL DESIGN 14/9/78
OPTIONAL
SWITCHED POWER SUPPLY
M12020
+15
-15
+5VDC
GND
+12V
C1
C2
Q1
Q2
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
IC10
IC11
IC12
IC13
IC14
IC15
IC16
IC17
IC18
IC19
IC20
IC21
IC22
IC23
IC24
IC25
IC26
IC27
IC28
IC29
IC30
IC31
IC32
IC33
IC34
IC35
IC36
IC37
IC38
IC39
IC40
IC41
IC42
IC43
IC44
IC45
IC46
IC47
IC48
IC49
IC50
IC51
IC52
IC53
IC54
IC55
IC56
IC57
IC58
IC59
IC60
IC61
IC62
IC63
IC64
IC65
IC66
IC67
IC68
IC69
IC70
IC71
IC72
IC73
IC74
IC75
IC76
IC77
IC78
IC79
IC80
IC81
IC82
IC83
IC84
IC85
IC86
IC87
IC88
IC89
IC90
IC91
IC92
IC93
IC94
IC95
IC96
IC97
IC98
IC99
IC100
IC101
IC102
IC103
IC104
IC105
IC106
IC107
IC108
IC109
IC110
IC111
IC112
IC113
IC114
IC115
IC116
IC117
IC118
IC119
IC120
IC121
IC122
IC123
IC124
IC125
IC126
IC127
IC128
IC129
IC130
IC131
IC132
IC133
IC134
IC135
IC136
IC137
IC138
IC139
IC140
IC141
IC142
IC143
IC144
IC145
IC146
IC147
IC148
IC149
IC150
IC151
IC152
IC153
IC154
IC155
IC156
IC157
IC158
IC159
IC160
IC161
IC162
IC163
IC164
IC165
IC166
IC167
IC168
IC169
IC170
IC171
IC172
IC173
IC174
IC175
IC176
IC177
IC178
IC179
IC180
IC181
IC182
IC183
IC184
IC185
IC186
IC187
IC188
IC189
IC190
IC191
IC192
IC193
IC194
IC195
IC196
IC197
IC198
IC199
IC200
IC201
IC202
IC203
IC204
IC205
IC206
IC207
IC208
IC209
IC210
IC211
IC212
IC213
IC214
IC215
IC216
IC217
IC218
IC219
IC220
IC221
IC222
IC223
IC224
IC225
IC226
IC227
IC228
IC229
IC230
IC231
IC232
IC233
IC234
IC235
IC236
IC237
IC238
IC239
IC240
IC241
IC242
IC243
IC244
IC245
IC246
IC247
IC248
IC249
IC250
IC251
IC252
IC253
IC254
IC255
IC256
IC257
IC258
IC259
IC260
IC261
IC262
IC263
IC264
IC265
IC266
IC267
IC268
IC269
IC270
IC271
IC272
IC273
IC274
IC275
IC276
IC277
IC278
IC279
IC280
IC281
IC282
IC283
IC284
IC285
IC286
IC287
IC288
IC289
IC290
IC291
IC292
IC293
IC294
IC295
IC296
IC297
IC298
IC299
IC300
IC301
IC302
IC303
IC304
IC305
IC306
IC307
IC308
IC309
IC310
IC311
IC312
IC313
IC314
IC315
IC316
IC317
IC318
IC319
IC320
IC321
IC322
IC323
IC324
IC325
IC326
IC327
IC328
IC329
IC330
IC331
IC332
IC333
IC334
IC335
IC336
IC337
IC338
IC339
IC340
IC341
IC342
IC343
IC344
IC345
IC346
IC347
IC348
IC349
IC350
IC351
IC352
IC353
IC354
IC355
IC356
IC357
IC358
IC359
IC360
IC361
IC362
IC363
IC364
IC365
IC366
IC367
IC368
IC369
IC370
IC371
IC372
IC373
IC374
IC375
IC376
IC377
IC378
IC379
IC380
IC381
IC382
IC383
IC384
IC385
IC386
IC387
IC388
IC389
IC390
IC391
IC392
IC393
IC394
IC395
IC396
IC397
IC398
IC399
IC400
IC401
IC402
IC403
IC404
IC405
IC406
IC407
IC408
IC409
IC410
IC411
IC412
IC413
IC414
IC415
IC416
IC417
IC418
IC419
IC420
IC421
IC422
IC423
IC424
IC425
IC426
IC427
IC428
IC429
IC430
IC431
IC432
IC433
IC434
IC435
IC436
IC437
IC438
IC439
IC440
IC441
IC442
IC443
IC444
IC445
IC446
IC447
IC448
IC449
IC450
IC451
IC452
IC453
IC454
IC455
IC456
IC457
IC458
IC459
IC460
IC461
IC462
IC463
IC464
IC465
IC466
IC467
IC468
IC469
IC470
IC471
IC472
IC473
IC474
IC475
IC476
IC477
IC478
IC479
IC480
IC481
IC482
IC483
IC484
IC485
IC486
IC487
IC488
IC489
IC490
IC491
IC492
IC493
IC494
IC495
IC496
IC497
IC498
IC499
IC500
IC501
IC502
IC503
IC504
IC505
IC506
IC507
IC508
IC509
IC510
IC511
IC512
IC513
IC514
IC515
IC516
IC517
IC518
IC519
IC520
IC521
IC522
IC523
IC524
IC525
IC526
IC527
IC528
IC529
IC530
IC531
IC532
IC533
IC534
IC535
IC536
IC537
IC538
IC539
IC540
IC541
IC542
IC543
IC544
IC545
IC546
IC547
IC548
IC549
IC550
IC551
IC552
IC553
IC554
IC555
IC556
IC557
IC558
IC559
IC560
IC561
IC562
IC563
IC564
IC565
IC566
IC567
IC568
IC569
IC570
IC571
IC572
IC573
IC574
IC575
IC576
IC577
IC578
IC579
IC580
IC581
IC582
IC583
IC584
IC585
IC586
IC587
IC588
IC589
IC590
IC591
IC592
IC593
IC594
IC595
IC596
IC597
IC598
IC599
IC600
IC601
IC602
IC603
IC604
IC605
IC606
IC607
IC608
IC609
IC610
IC611
IC612
IC613
IC614
IC615
IC616
IC617
IC618
IC619
IC620
IC621
IC622
IC623
IC624
IC625
IC626
IC627
IC628
IC629
IC630
IC631
IC632
IC633
IC634
IC635
IC636
IC637
IC638
IC639
IC640
IC641
IC642
IC643
IC644
IC645
IC646
IC647
IC648
IC649
IC650
IC651
IC652
IC653
IC654
IC655
IC656
IC657
IC658
IC659
IC660
IC661
IC662
IC663
IC664
IC665
IC666
IC667
IC668
IC669
IC670
IC671
IC672
IC673
IC674
IC675
IC676
IC677
IC678
IC679
IC680
IC681
IC682
IC683
IC684
IC685
IC686
IC687
IC688
IC689
IC690
IC691
IC692
IC693
IC694
IC695
IC696
IC697
IC698
IC699
IC700
IC701
IC702
IC703
IC704
IC705
IC706
IC707
IC708
IC709
IC710
IC711
IC712
IC713
IC714
IC715
IC716
IC717
IC718
IC719
IC720
IC721
IC722
IC723
IC724
IC725
IC726
IC727
IC728
IC729
IC730
IC731
IC732
IC733
IC734
IC735
IC736
IC737
IC738
IC739
IC740
IC741
IC742
IC743
IC744
IC745
IC746
IC747
IC748
IC749
IC750
IC751
IC752
IC753
IC754
IC755
IC756
IC757
IC758
IC759
IC760
IC761
IC762
IC763
IC764
IC765
IC766
IC767
IC768
IC769
IC770
IC771
IC772
IC773
IC774
IC775
IC776
IC777
IC778
IC779
IC780
IC781
IC782
IC783
IC784
IC785
IC786
IC787
IC788
IC789
IC790
IC791
IC792
IC793
IC794
IC795
IC796
IC797
IC798
IC799
IC800
IC801
IC802
IC803
IC804
IC805
IC806
IC807
IC808
IC809
IC810
IC811
IC812
IC813
IC814
IC815
IC816
IC817
IC818
IC819
IC820
IC821
IC822
IC823
IC824
IC825
IC826
IC827
IC828
IC829
IC830
IC831
IC832
IC833
IC834
IC835
IC836
IC837
IC838
IC839
IC840
IC841
IC842
IC843
IC844
IC845
IC846
IC847
IC848
IC849
IC850
IC851
IC852
IC853
IC854
IC855
IC856
IC857
IC858
IC859
IC860
IC861
IC862
IC863
IC864
IC865
IC866
IC867
IC868
IC869
IC870
IC871
IC872
IC873
IC874
IC875
IC876
IC877
IC878
IC879
IC880
IC881
IC882
IC883
IC884
IC885
IC886
IC887
IC888
IC889
IC890
IC891
IC892
IC893
IC894
IC895
IC896
IC897
IC898
IC899
IC900
IC901
IC902
IC903
IC904
IC905
IC906
IC907
IC908
IC909
IC910
IC911
IC912
IC913
IC914
IC915
IC916
IC917
IC918
IC919
IC920
IC921
IC922
IC923
IC924
IC925
IC926
IC927
IC928
IC929
IC930
IC931
IC932
IC933
IC934
IC935
IC936
IC937
IC938
IC939
IC940
IC941
IC942
IC943
IC944
IC945
IC946
IC947
IC948
IC949
IC950
IC951
IC952
IC953
IC954
IC955
IC956
IC957
IC958
IC959
IC960
IC961
IC962
IC963
IC964
IC965
IC966
IC967
IC968
IC969
IC970
IC971
IC972
IC973
IC974
IC975
IC976
IC977
IC978
IC979
IC980
IC981
IC982
IC983
IC984
IC985
IC986
IC987
IC988
IC989
IC990
IC991
IC992
IC993
IC994
IC995
IC996
IC997
IC998
IC999
IC1000


ANALOG INPUT MODULE V.2
DCM SUBUNIT
A/D-1
REESE CUTLER
CUTLER DIGITAL DESIGN 11/19/78

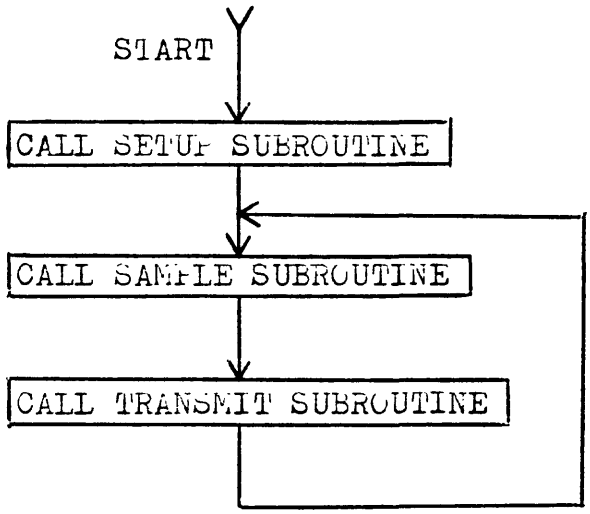

COMMUNICATION INTERFACE
DCN SUBNET
REESE CUTLER
CUTLER DIGITAL DESIGN
VCO
DIP SOCKET
DIP SOCKET
LSBUSY
TAPAL
DNL
OH
DA



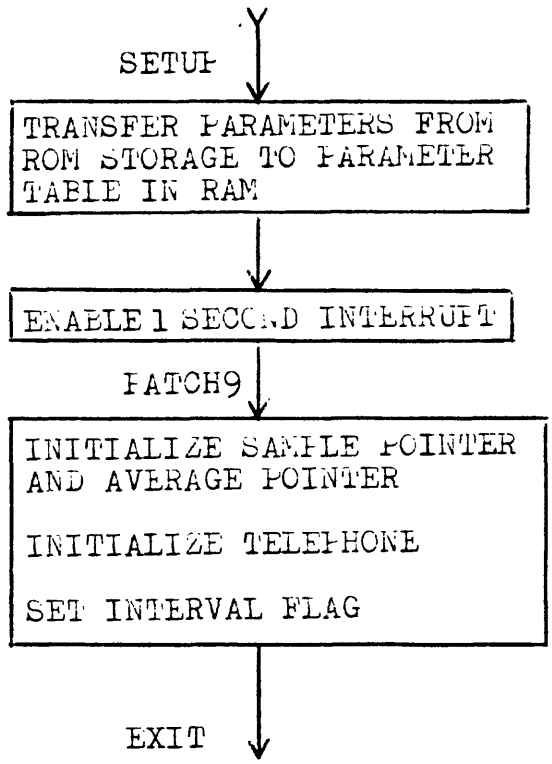
Circuit Diagram of Quartz Cryst 1 Reference Digital VCO.

APPENDIX B

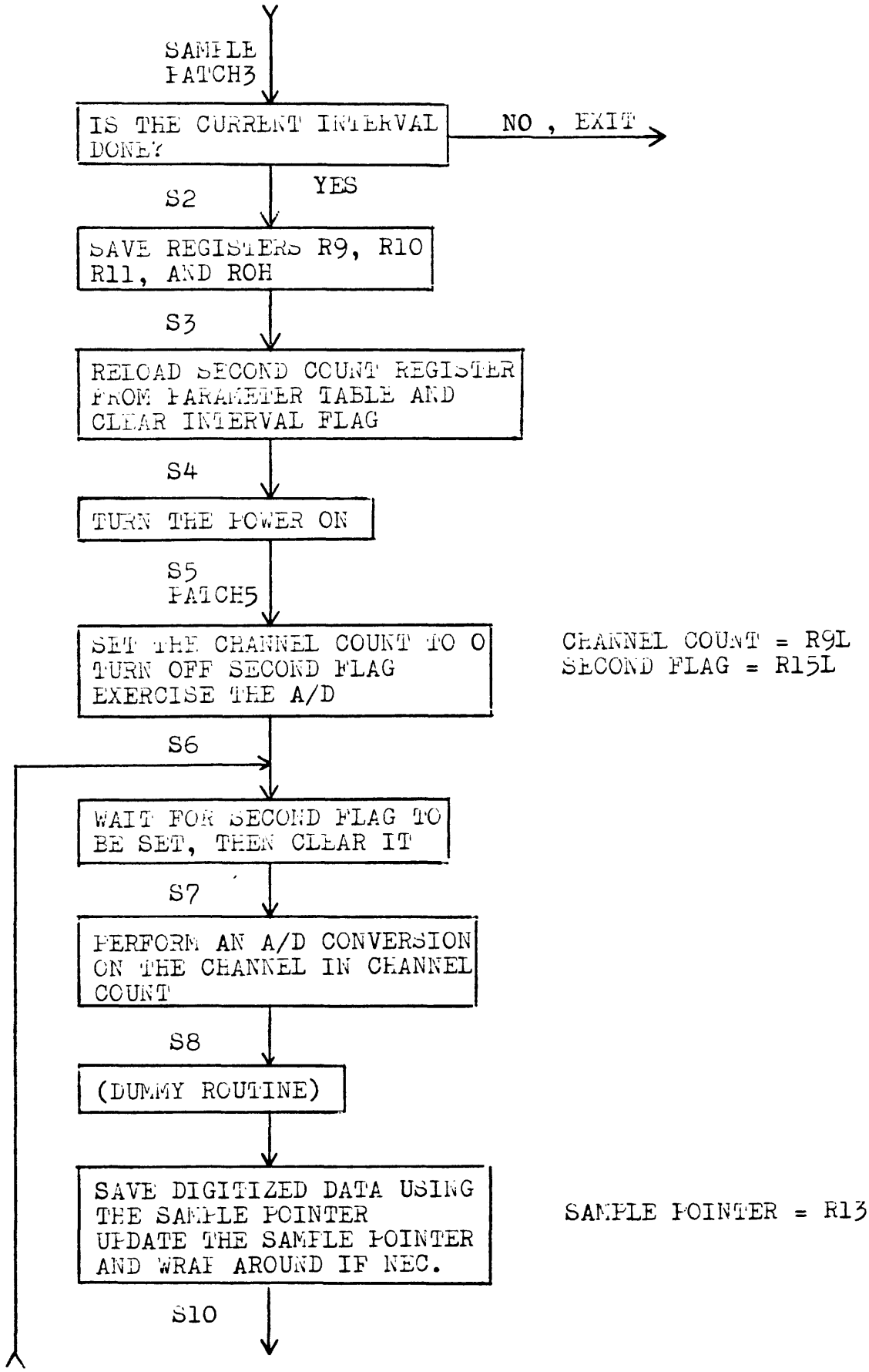
General Purpose Analog Data Collection Program



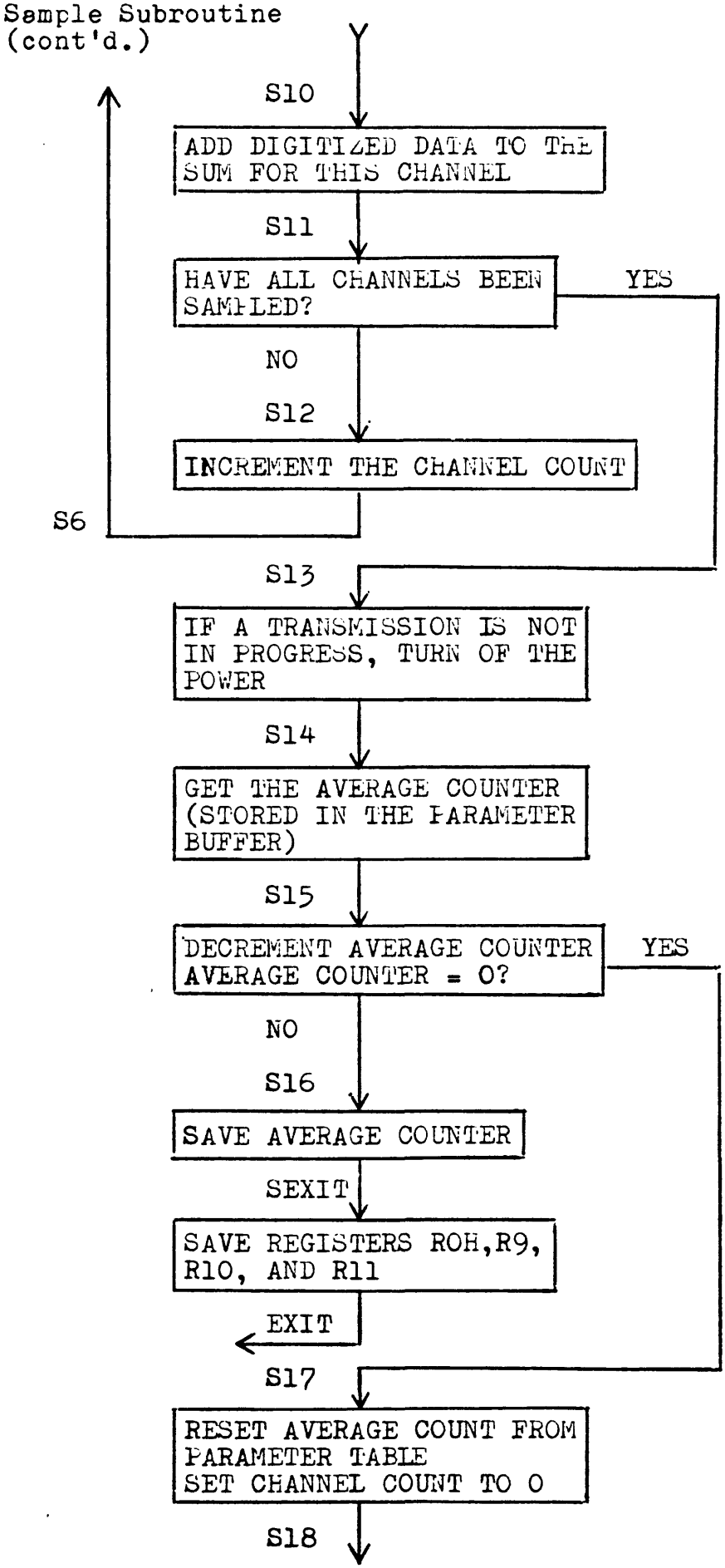
Setup Subroutine



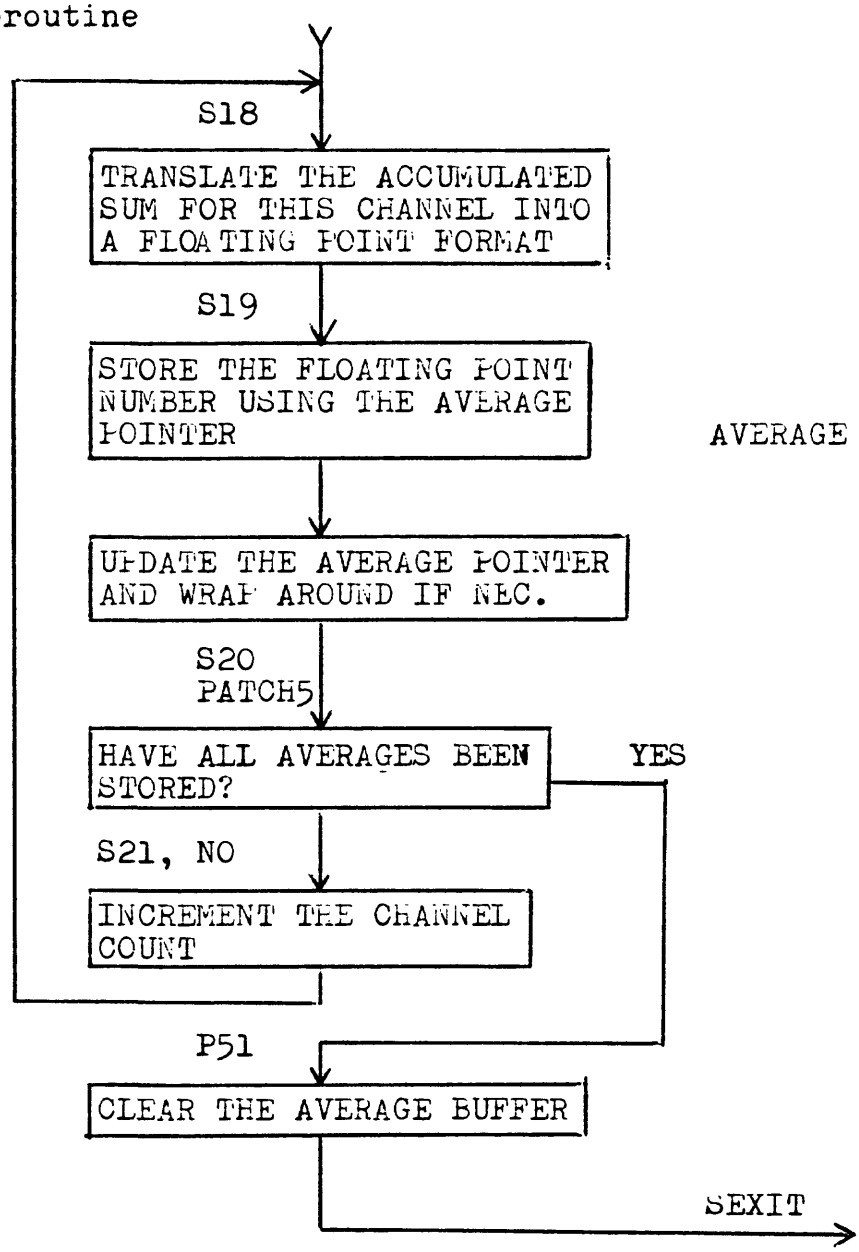
Sample Subroutine

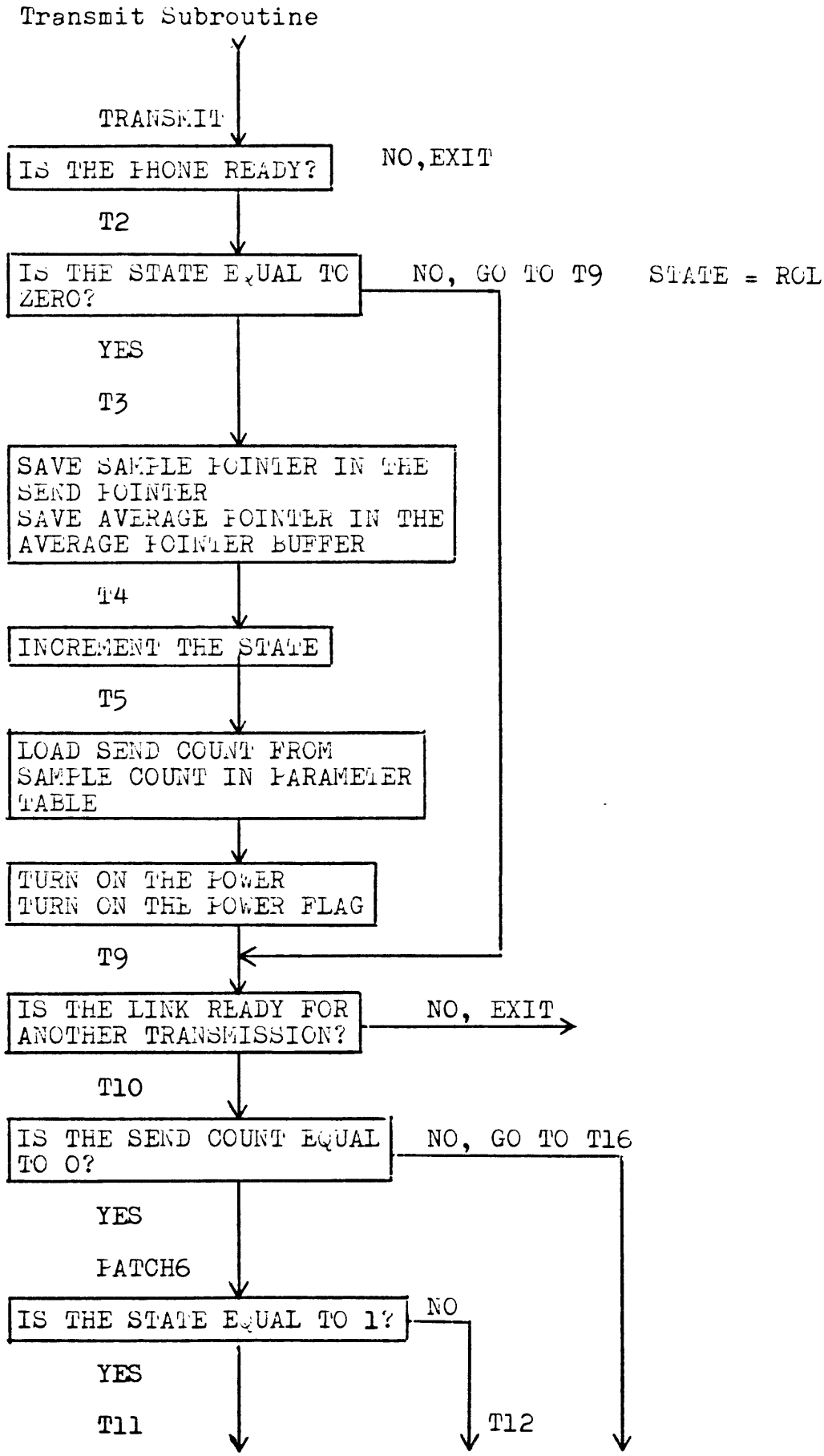


Sample Subroutine
(cont'd.)

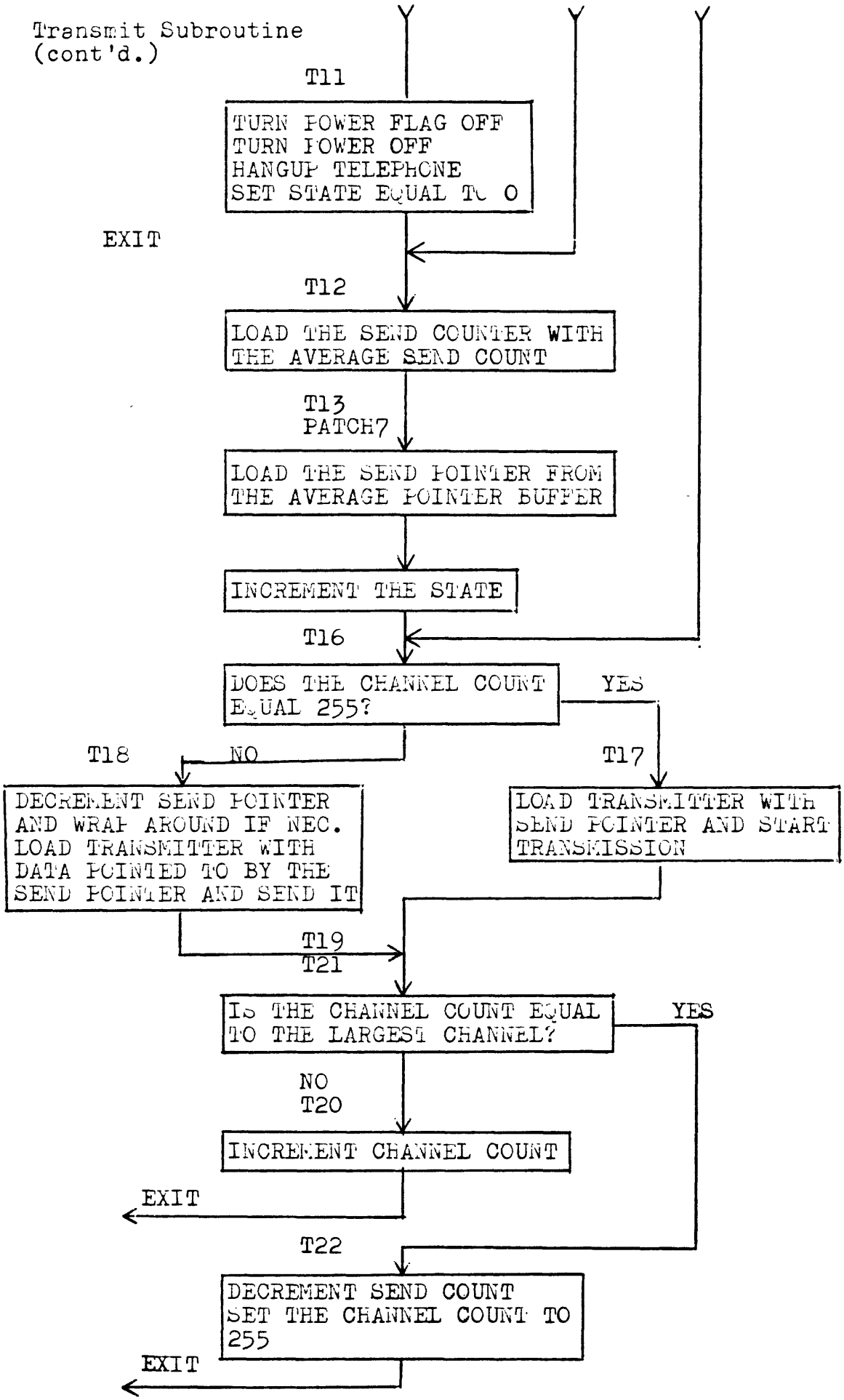


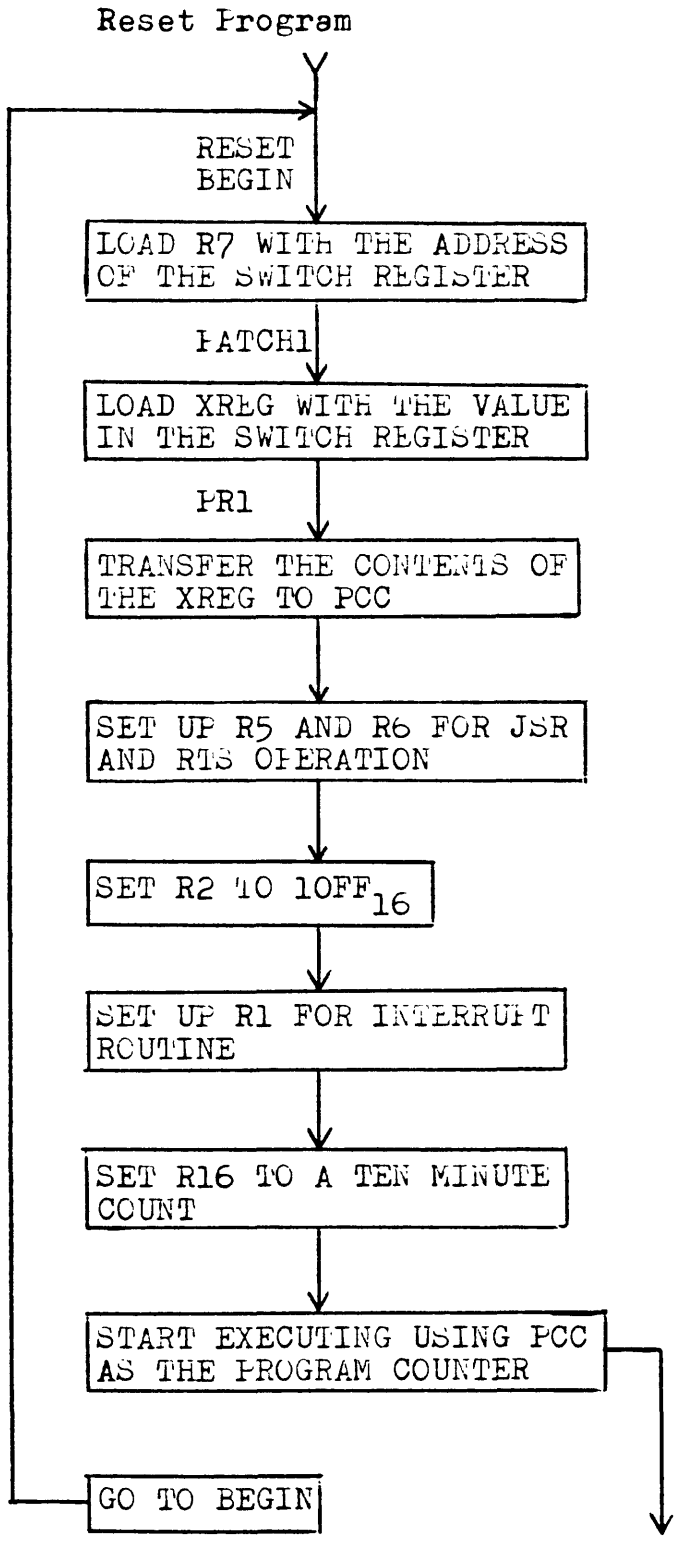
Sample Subroutine
(cont'd.)



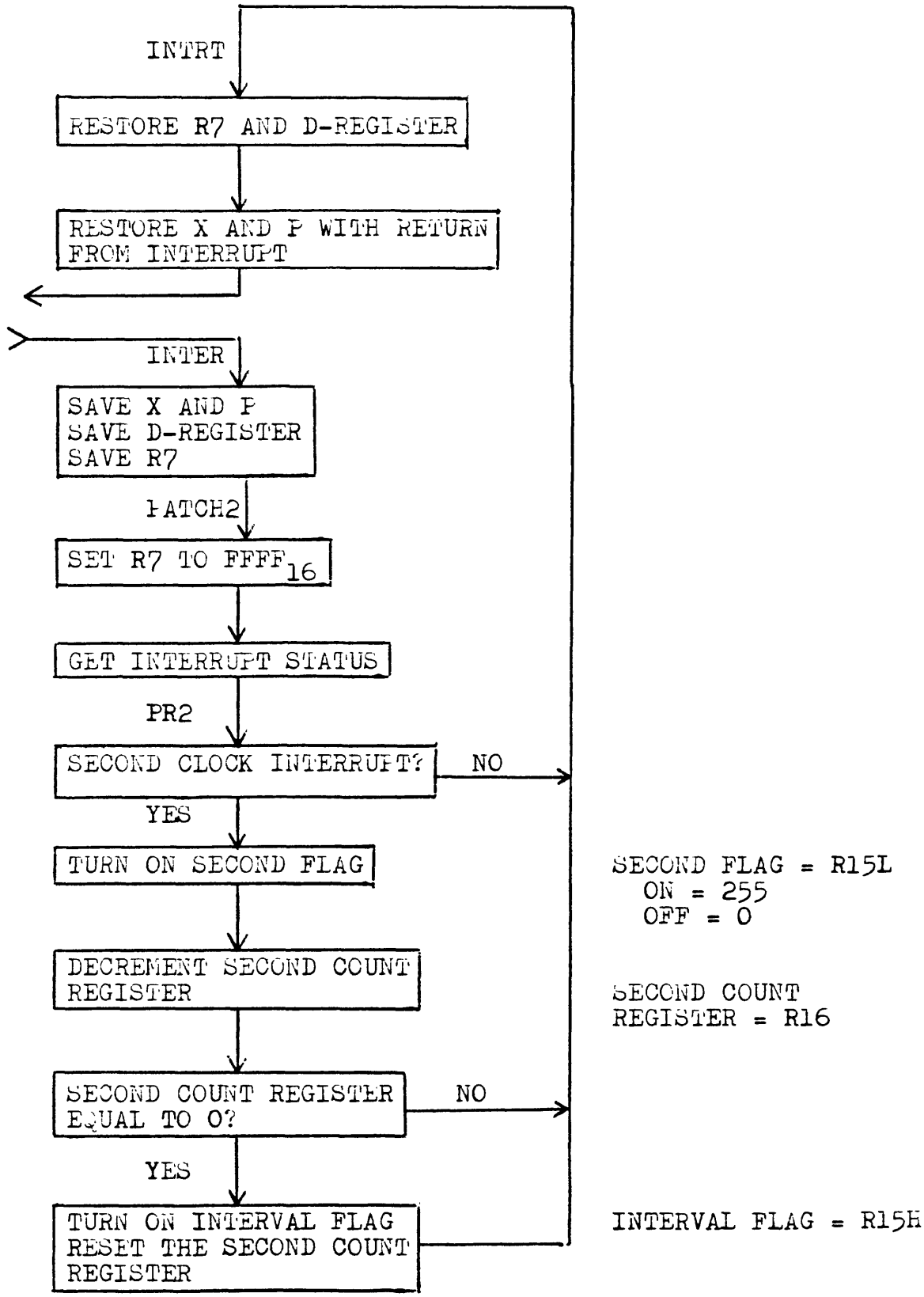

Transmit Subroutine
TRANSMIT
IS THE PHONE READY?
NO,EXIT
T2
IS THE STATE EQUAL TO ZERO?
NO, GO TO T9
STATE = ROL
YES
T3
SAVE SAMPLE POINTER IN THE SEND POINTER
SAVE AVERAGE POINTER IN THE AVERAGE POINTER BUFFER
T4
INCREMENT THE STATE
T5
LOAD SEND COUNT FROM SAMPLE COUNT IN PARAMETER TABLE
TURN ON THE POWER
TURN ON THE POWER FLAG
T9
IS THE LINK READY FOR ANOTHER TRANSMISSION?
NO, EXIT
T10
IS THE SEND COUNT EQUAL TO 0?
NO, GO TO T16
YES
PATCH6
IS THE STATE EQUAL TO 1?
NO
YES
T11
T12

Transmit Subroutine
(cont'd.)

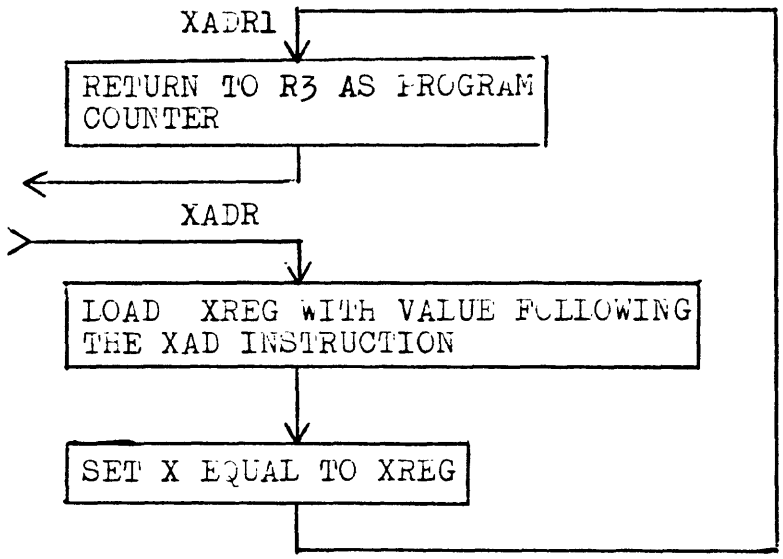



Reset Program
RESET
BEGIN
LOAD R7 WITH THE ADDRESS OF THE SWITCH REGISTER
PATCH1
LOAD XREG WITH THE VALUE IN THE SWITCH REGISTER
XREG = R8
PR1
TRANSFER THE CONTENTS OF THE XREG TO PCC
PCC = R3
SET UP R5 AND R6 FOR JSR AND RTS OPERATION
SET R2 TO 10FF16
R2 = STACK POINTER FOR INT, JSR AND RTS
SET UP R1 FOR INTERRUPT ROUTINE
SET R16 TO A TEN MINUTE COUNT
R16 IS USED BY THE INTERRUPT ROUTINE TO COUNT SECONDS
START EXECUTING USING PCC AS THE PROGRAM COUNTER
GO TO BEGIN

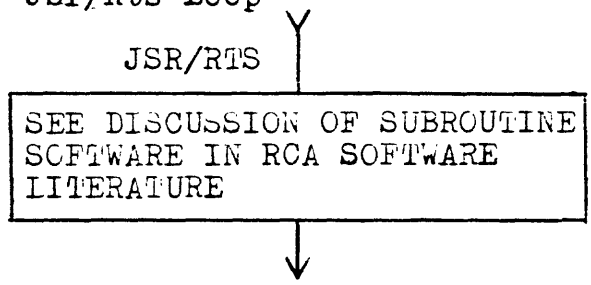
Interrupt Routine



Xadr Loop



Jsr/Rts Loop



APPENDIX C

PROGRAM LISTING

```
0000                    org 0
0000            'set assembeler constants'
0000                    255*256+6 = switches
0000                    0=r0
0000                    1=r1
0000                    2=r2
0000                    3=r3
0000                    4=r4
0000                    5=r5
0000                    6=r6
0000                    7=r7
0000                    8=r8=xreg
0000                    9=r9
0000                    10=ra
0000                    11=rb
0000                    12=rc
0000                    13=rd
0000                    14=re
0000                    15=rf
0000                    r3=pcc
0000                     600=scount
0000            'begin of reset program'
0000                    org     0
0000  F800              ldi     (xadr hi)
0002  B7                phi     r7
0003  F8CC              ldi     xadr
0005  A7                plo     r7
0006  30F7              br      patch1
0008  C4                nop
0009  48        pr1:    lda     xreg
000A  A3                plo     pcc
000B  48                lda     xreg
000C  B3                phi     pcc
000D  F800              ldi     (jsrst hi)          %
000F  B4                phi     r4
0010  F800              ldi     (retst hi)          %
0012  B5                phi     r5
0013  F804              ldi     jsrst
0015  A4                plo     r4
0016  F8E6              ldi     retst
0018  A5                plo     r5
0019  F810              ldi     16          %set up x reg
001B  B2                phi     r2
001C  F8FF              ldi     255
001E  A2                plo     r2
001F  F800              ldi     (inter hi) %set up interrupt reg
0021  B1                phi     r1
0022  F834              ldi     inter
0024  A1                plo     r1
0025  F802              ldi     (scount hi)
0027  BF                phi     rf          %set up sample interval
0028  F858              ldi     scount
002A  AF                plo     rf
002B  D3                sep     r3          %jmp to start of program
002C  3000              br      0
002E            'tp1' is,
002E  42        intrt:  lda     r2          %restore register 7
002F  B7                phi     r7
0030  42                lda     r2
0031  A7                plo     r7
```

```
0032  42              lda     r2
0033  70              ret                     %return from interrupt
0034  22    inter:    dec     r2
0035  78              sav
0036  22              dec     r2
0037  52              stn     r2
0038  22              dec     r2
0039  87              glo     r7
003A  52              stn     r2
003B  22              dec     r2
003C  97              ghi     r7
003D  52              stn     r2
003E  F8FF            ldi     255
0040  3001            br      patch2
0042  FA80    pr2:    ani     128
0044  322E            bz      intrt
0046  F8FF            ldi     255
0048  AE              plo     re
0049  2F              dec     rf
004A  8F              glo     rf
004B  3A2E            bnz     intrt
004D  9F              ghi     rf
004E  3A2E            bnz     intrt
0050  F802            ldi     (scount hi)
0052  BF              phi     rf
0053  F858            ldi     scount
0055  AF              plo     rf
0056  F8FF            ldi     255
0058  BE              phi     re
0059  302E            br      intrt
005C                  org     (5*16+12)
005C  D5      compose: rts                    %get channel
005D  FE              shl
005E  FE              shl
005F  FE              shl
0060  FE              shl                     %shift into ms nibble
0061  73              stxd                    %and save on stack
0062  9A              ghi     ra              %get top byte and save
0063  B9              phi     r9
0064  F6              shr                     %shift and remove garb
0065  FA07            ani     7               %
0067  BA              phi     ra              %save
0068  8A              glo     ra              %shift into bottom byt
0069  76              shrc
006A  AA              plo     ra              %and save
006B  99              ghi     r9              %evaluate sign bit
006C  7E              shlc
006D  3377            bdf     compos1         %no sign inversion
006F  8A              glo     ra
0070  FD00            sdi      0               %subtract value from
0072  AA              plo     ra
0073  9A              ghi     ra
0074  7D00            sdbi    0
0076  BA              phi     ra
0077  9A    compos1: ghi        ra              %tack on channel
0078  FA0F            ani     15
007A  60              irx
007B  F1              orr
007C  FB08            xri     8               %complement sign bit
007E  BA              phi     ra
```

```
007F  D5                  rts
0080          'tp2' is,
0084                      org       (8*16+4)
0084  D7FF02  send:       xad       larse (255 256 tims+2 =larse,)
0087  8A                  glo       ra
0088  58                  stn       xreg
0089  18                  inc       xreg
008A  9A                  ghi       ra
008B  58                  stn       xreg
008C  18                  inc       xreg
008D  08                  ldn       xreg
008E  F902                ori       2
0090  58                  stn       xreg
0091  08                  ldn       xreg
0092  FAFD                ani       (15*16+13)
0094  58                  stn       xreg
0095  08        send1:    ldn       xreg
0096  FA04                ani       4
0098  3295                bz        send1
009A  D5                  rts
00A0                      org       160
00A0  D7FFD4  atod:       xad       atd   (larse +2=atd,)%set up a to d address
00A3  89                  glo       r9                    %get channel
00A4  58                  stn       xreg                    %start conversion
00A5  C4                  nop                             %wait
00A6  C4                  nop
00A7  C4                  nop
00A8  48                  lda       xreg
00A9  AA                  plo       ra                    %save a to d value in r
00AA  08                  ldn       xreg
00AB  BA                  phi       ra
00AC  D5                  rts
00AD  D7FFD0  poweron:    xad       (larse-2)             %set up power switch
00B0  08                  ldn       xreg                    %and turn it on
00B1  F901                ori       1
00B3  58                  stn       xreg
00B4  D5                  rts
00B5  D7FFD0  poweroff:   xad       (larse - 2)         %set up power switch
00B8  08                  ldn       xreg
00B9  FAFE                ani        254                  %and turn it off
00BB  58                  stn       xreg
00BC  D5                  rts
00BD  46        waitit:   lda       r6
00BE  B8                  phi       xreg
00BF  46                  lda       r6
00C0  A8                  plo        xreg
00C1  88        wait1:     glo       xreg
00C2  32C7                bz        wait11
00C4  28        wait22:   dec       xreg
00C5  30C1                br        wait1
00C7  98        wait11:   ghi       xreg
00C8  3AC4                bnz       wait22
00CA  D5                  rts
00CB  D3        xadr1:    sep       r3
00CC  43        xadr:     lda       r3
00CD  B8                  phi       xreg
00CE  43                  lda       r3
00CF  A8                  plo       xreg
00D0  E8                  sex       xreg
00D1  30CB                br        xadr1
```

```
00D3  D3       exita:   sep      r3
00D4  E2       jsrst:   sex      r2
00D5  22                dec      r2
00D6  96                ghi      r6
00D7  73                stxd
00D8  86                glo      r6
00D9  73                stxd
00DA  93                ghi      r3
00DB  B6                phi      r6
00DC  83                glo      r3
00DD  A6                plo      r6
00DE  46                lda      r6
00DF  B3                phi      r3
00E0  46                lda      r6
00E1  A3                plo      r3
00E2  30D3              br       exita
00E4  C4                nop
00E5  D3       exitr:   sep      r3
00E6  96       retst:   ghi      r6
00E7  B3                phi      r3
00E8  86                glo      r6
00E9  A3                plo      r3
00EA  E2                sex      r2
00EB  12                inc      r2
00EC  72                ldxa
00ED  A6                plo      r6
00EE  72                ldxa
00EF  B6                phi      r6
00F0  30E5              br       exitr
00F2: A7       patch2:  plo      r7
00F3  B7                phi      r7
00F4  07                ldn      r7
00F5  3042              br       pr2
00F7  F8FF     patch1:  ldi      (switches hi)
00F9  B8                phi      xreg
00FA  F806              ldi      switches
00FC  A8                plo      xreg
00FD  3009              br       pr1
00FF           'pt3' is
0100                    org      256
0100  D402DA   start:   jsr      setup                %
0103  D4010B            jsr      sample               %
0106  D40200            jsr      transmit             %
0109  3003              br       (start+3)            %
010B  30C3     sample:  br       patch3                   %time interval up
010D  9B       s2:      ghi      rb                   %save important regis
010E  73                stxd                          %
010F  8B                glo      rb                   %
0110  73                stxd                          %
0111  9A                ghi      ra                   %
0112  73                stxd                          %
0113  8A                glo      ra                   %
0114  73                stxd                          %
0115  99                ghi      r9                   %
0116  73                stxd                          %
0117  89                glo      r9                   %
0118  73                stxd
0119  90                ghi      r0                   %
011A  73                stxd                          %
011B  D71000   s3:      xad      pbuf (4096=pbuf)     %
```

```
011E  72          ldxa                              %
011F  BF          phi     rf                        %
0120  72          ldxa
0121  AF          plo     rf                        %
0122  D400AD  s4: jsr     poweron                   %
0125  F800    s5: ldi     0                         %
0127  3000        br      patch4
0129  8E      s6: glo     re                        %
012A  3229        bz      s6                        %
012C  F800        ldi     0                         %
012E  AE          plo     re                        %
012F  D400AD  s7: jsr     atod                      %
0132  D4005C  s8: jsr     compose                   %
0135  9A          ghi     ra                        %
0136  5D          stn     rd                        %
0137  1D          inc     rd                        %
0138  8A          glo     ra                        %
0139  5D          stn     rd                        %
013A  1D          inc     rd                        %
013B  8D          glo     rd                        %
013C  3A48        bnz     s10                       %
013E  D7100B      xad     (pbuf+11)                 %
0141  9D          ghi     rd                        %
0142  F5          sd                                      %
0143  3A48        bnz     s10                       %
0145  60          irx                               %
0146  F0          ldx                               %
0147  BD          phi     rd                         %
0148  D71020  s10: xad     avgb  (pbuf+32=avgb)      %
014B  89          glo     r9                        %
014C  FE          shl                               %
014D  FE          shl                               %
014E  FC20        adi     avgb                      %
0150  A8          plo     xreg                       %
0151  8A          glo     ra                        %
0152  F4          add                               %
0153  58          stn      xreg                     %
0154  18          inc     xreg                      %
0155  9A          ghi     ra
0156  FA0F        ani      15                       %
0158  74          adc                               %
0159  58          stn     xreg                      %
015A  18          inc      xreg
015B  F800        ldi     0                         %
015D  74          adc                               %
015E  58          stn      xreg                     %
015F  D7100C  s11: xad     (pbuf+4)                  %
0162  89          glo     r9                        %
0163  F5          sd
0164  3269        bz      s13
0166  19      s12: inc     r9
0167  3029        br      s6                        %
0169  80      s13: glo     r0                        %
016A  3A6F        bnz     s14                       %
016C  D400B5      jsr     poweroff                  %
016F  E7100E  s14: xad     (pbuf+14)                 %
0172  72          ldxa                              %
0173  BB          phi     rb
0174  F0          ldx                               %
0175  AB          plo     rb
```

```
0176  2B        s15:    dec     rb                  %decrement avg cnt
0177  8B                glo     rb                   %
0178  3A7D              bnz     s16                 %
017A  9B                ghi     rb                  %
017B  3292              bz      s17                 %
017D  8B        s16:    glo     rb                  %
017E  73                stxd                        %
017F  9B                ghi     rb                  %
0180  58                stn     xreg                %
0181  E2        sexit:  sex     r2                  %
0182  60                irx
0183  72                ldxa                        %
0184  B0                phi     r0                  %
0185  72                ldxa                        %
0186  A9                plo     r9                  %
0187  72                ldxa                        %
0188  B9                phi     r9                  %
0189  72                ldxa                        %
018A  AA                plo     ra                  %
018B  72                ldxa                        %
018C  BA                phi     ra                  %
018D  72                ldxa                        %
018E  AB                plo     rb                  %
018F  F0                ldx                         %
0190  BB                phi      rb                 %
0191  D5                rts                         %
0192  D71002   s17:     xad     (pbuf+2)            %
0195  72                ldxa                        %
0196  BB                phi     rb                  %
0197  F0                ldx                         %
0198  AB                plo     rb                  %
0199  D7100E            xad     (pbuf+14)           %
019C  8B                glo     rb                  %
019D  73                stxd                        %
019E  9B                ghi     rb                  %
019F  73                stxd
01A0  F800              ldi     0                   %zero channel count
01A2  A9                plo     r9                  %
01A3  D40287    s18:    jsr     float               %
01A6  9A        s19:    ghi     ra                  %
01A7  5C                stn     rc                  %
01A8  1C                inc     rc                  %
01A9  8A                glo     ra                  %
01AA  5C                stn     rc                  %
01AB  1C                inc     rc                  %
01AC  8C                glo      rc                 %
01AD  3AB9              bnz     s20
01AF  D71009            xad      (pbuf+9)           %
01B2  9C                ghi     rc                  %
01B3  F5                sd
01B4  3AB9              bnz     s20
01B6  60                irx                         %
01B7  F0                ldx                         %
01B8  BC                 phi     rc                  %
01B9  D71004    s20:    xad      (pbuf+4)           %
01BC  89                glo     r9                  %
01BD  C00380            lbr     patch5
01C0  19        s21:    inc     r9                  %
01C1  30A3              br      s18                 %
01C3  9E        patch3: ghi     re
```

```
01C4  3A0D            bnz     s2
01C6  D5              rts
01D0                  org     (256+(13*16))
01D0  A9      patch4: plo     r9
01D1  AE              plo     re
01D2  BE              phi       re
01D3  D400A0          jsr     atod
01D6  3029            br      s6
0200                  org     512                    %
0200  3503    transmit: b2    t2                     %
0202  D5              rts                            %
0203  80      t2:     glo     r0                     %
0204  3A1C            bnz     t9                     %
0206  9D      t3:     ghi     rd                     %
0207  BB              phi     rb                     %
0208  8D              glo     rd                     %
0209  AB              plo     rb                     %
020A  9C              ghi     rc                     %
020B  BA              phi     ra                     %
020C  8C              glo     rc                     %
020D  AA              plo     ra                     %
020E  10      t4:     inc      r0                    %
020F  D71005  t5:     xad     (pbuf+5)               %
0212  72              ldxa
0213  B9              phi      r9                    %
0214  72              ldxa                           %
0215  A9              plo      r9                    %
0216  F8FF            ldi      255                   %
0218  B0              phi      r0                    %
0219  D400AD          jsr      poweron               %
021C  3425    t9:     b1      t10
021E  D5              rts
021F  C4              nop
0220  C4              nop
0221  C4              nop
0222  C4              nop
0223  C4              nop
0224  C4              nop
0225  99      t10:    ghi     r9                     %
0226  3A42            bnz     t16                    %
0228  89              glo     r9                     %
0229  3A42            bnz     t16                    %
022B  C0033E          lbr     patch6
022E  F800    t11:    ldi     0                      %
0230  A0              plo      r0                    %
0231  D400B5          jsr     poweroff               %
0234  7B              seq
0235  7A              req                            %
0236  D5              rts
0237  D71007  t12:    xad     (phuf+7)               %
023A  72              ldxa                           %
023B  B9              phi      r9                    %
023C  72              ldxa                           %
023D  A9              plo      r9                    %
023E  9A      t13:    ghi      ra                    %
023F  C00330          lbr     patch7
0242  90      t16:     ghi     r0                      %
0243  FDFF            sdi     255                     %
0245  3A52            bnz     t18                    %
0247  D7FF03  t17:    xad     (larse+1)              %
```

```
0299  F804          ldi     4               %
029B  FF01  f1:     smi     1                %
029D  58            stn     xreg            %
029E  8A            glo     ra              %
029F  FE            shl
02A0  AA            plo     ra
02A1  9A            ghi     ra
02A2  7E            shlc
02A3  BA            phi     ra
02A4  8B            glo     rb
02A5  7E            shlc
02A6  AB            plo     rb
02A7  9B            ghi     rb
02A8  7E            shlc
02A9  BB            phi     rb
02AA  08            ldn     xreg
02AB  3A9B          bnz     f1              %
02AD  58            stn     xreg            %
02AE  9B    f4:     ghi     rb              %
02AF  3AB4          bnz     f2              %
02B1  8B            glo     rb              %
02B2  32C6          bz      f3              %
02B4  F801  f2:     ldi     1
02B6  F4            add
02B7  58            stn     xreg            %
02B8  9B            ghi     rb              %
02B9  F6            shr
02BA  BB            phi     rb              %
02BB  8B            glo     rb
02BC  76            shrc
02BD  AB            plo     rb
02BE  9A            ghi     ra
02BF  76            shrc
02C0  BA            phi     ra
02C1  8A            glo     ra
02C2  76            shrc
02C3  AA            plo     ra
02C4  30AE          br      f4              %
02C6  08    f3:     ldn     xreg            %
02C7  AB            plo     rb              %
02C8  F804          ldi     4               %
02CA  58    f5:     stn     xreg            %
02CB  8B            glo     rb
02CC  F6            shr
02CD  AB            plo     rb
02CE  9A            ghi     ra
02CF  76            shrc
02D0  BA            phi     ra
02D1  8A            glo     ra
02D2  76            shrc
02D3  AA            plo     ra
02D4  08            ldn     xreg
02D5  FF01          smi     1
02D7  3ACA          bnz     f5
02D9  D5            rts                     %
02DA  D71000  setup: xad    4096            %
02DD  F803          ldi     (pmbf hi)       %
02DF  B9            phi     r9              %
02E0  F800          ldi     pmbf            %
02E2  A9            plo     r9              %
```

```
024A  9B              ghi     rb                      %
024B  FA0F            ani     15                      %
024D  73              stxd                            %
024E  8B              glo     rb                      %
024F  73              stxd
0250  306C            br      t19                     %
0252  8B      t18:    glo     rb                      %
0253  3A65            bnz     t18a                    %
0255  D710CC          xad     (pbuf+12)               %
0258  9B              ghi     rb                      %
0259  F5              sd                              %
025A  3262            bz      t18fin                  %
025C  28              dec     xreg                    %
025D  28              dec     xreg                    %
025E  9B              ghi     rb                      %
025F  F5              sd
0260  3A65                    bnz     t18a                    %
0262  28      t18fin: dec     xreg                    %
0263  FC              ldx                             %
0264  BB              phi     rb                      %
0265  D7FF03  t18a:   xad     (larse+1)               %
0268  C0034F          lbr     patch8
026B  C4              nop
026C  C4      t19:    nop
026D  C4              nop
026E  C4              nop
026F  C4              nop
0270  C4              nop
0271  C4              nop
0272  C4              nop
0273  C4              nop
0274  C4              nop
0275  C4              nop
0276  D71004  t21:    xad     (pbuf+4)                %
0279  90              ghi     r0                      %
027A  F5              sd                              %
027B  3282            bz      t22                     %
027D  90      t20:    ghi     r0                      %
027E  FC01            adi     1                       %
0280  B0              phi     r0
0281  D5              rts                             %
0282  29      t22:    dec     r9                      %
0283  F8FF            ldi     255                     %
0285  B0              phi     r0                      %
0286  D5              rts                             %
0287          'pt4' is,
0287  D71020  float:  xad     avgb                     %
028A  89              glo     r9                       %
028B  FE              shl                              %
028C  FE              shl                             %
028D  FC20            adi      avgb                   %
028F  A8              plo     xreg                    %
0290  72              ldxa                            %
0291  AA              plo     ra                      %
0292  72              ldxa                            %
0293  BA              phi     ra                      %
0294  72              ldxa                            %
0295  AB              plo     rb                      %
0296  F800            ldi      0                      %
0298  BB              phi     rb                      %
```

```
02E3  F80F            ldi     15                  %
02E5  AA              plo      ra                 %
02E6  49      sup1:   lda     r9                  %
02E7  58              stn     xreg                %
02E8  18              inc     xreg                %
02E9  2A              dec     ra                  %
02EA  8A              glo     ra                  %
02EB  3AE6            bnz     sup1            %
02ED  D7FFFF          xad     (64*1024-1)         %
02F0  F880            ldi     (8*16)              %
02F2  58              stn     xreg                %
02F3  7B              seq
02F4  F800            ldi     0
02F6  A0              plo      r0
02F7  AC              plo     rc                  %
02F8  AD              plo     rd                  %
02F9  C00320          lbr     patch9
0300                  org     (3*256)
0300  0258    pmbf:   wrd     600
0302  0006            wrd     6
0304  02              byt     2
0305  00B4            wrd     180
0307  001E            wrd     30
0309  13              byt     19
030A  12              byt     18
030B  18              byt     24
030C  13              byt     19
030D  0006            wrd     6
0320                  org      800
0320  D70309  patch9: xad      (pmbf+9)
0323  48              lda      xreg
0324  BD              phi      rd
0325  08              ldn      xreg
0326  BC              phi      rc
0327  F8FF            ldi      255
0329  BE              phi      re
032A  D5               rts
0330                  org      (pmbf+48)
0330  BB      patch7: phi      rb
0331  8A              glo     ra
0332  AB              plo     rb
0333  10              inc      r0
0334  C00242          lbr      t16
033E                  org      (patch7+14)
033E  80      patch6: glo      r0
033F  FF01            smi      1
0341  C20237          lbz      t12
0344  C00226          lbr      t11
034F                  org      (pmbf+64+15)
034F  2B      patch8: dec      rb
0350  0B              ldn      rb
0351  58              stn      xreg
0352  1B              inc      xreg
0353  2B              dec      rb
0354  0B              ldr      rb
0355  58              stn      xreg
0356  C00260          lbr      t19
0380                  org      (pmbf+(16*8))
0380  F5      patch5: sd
0381  3286            bz      p51
```

```
0383  C0C1C0          lbr       s21
0386  D7105F  p51:    xad       (avgh+63)
0389  F800    p52:    ldi       0
038B  73              stxd
038C  88              glo       xreg
038D  FD1F            sdi       31
038F  3A89            bnz       p52
0391  C0C181          lbr       sexit
```