UNITED STATES DEPARTMENT OF THE INTERIOR

GEOLOGICAL SURVEY

DIGITAL RECORDING SYSTEM FOR TELEMETERED DWWSSN STATIONS

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1. INTRODUCTION

The World-Wide Standardized Seismograph Network (WWSSN) was installed during the early 1960's and used photographic paper as the medium to record the seismic data. The WWSSN network is still a primary system used to obtain world-wide seismic information. During the past several years, significant process has been made in modernizing the global seismic network. The global seismic network consists of both the analog recording network (WWSSN) and the Global Digital Seismograph Network (GDSN). The GDSN is composed of systems as the Seismic Research Observatories (SRO), modified High-Gain Long Period Stations (ASRO), and now the Digital World-Wide Standardized Seismograph Network (DWWSSN) stations. A Digital Recording System (DRS) has been designed for upgrading WWSSN stations to DWWSSN stations.

One objective of recording the WWSSN data in a digital format was to record the WWSSN seismic data on magnetic tapes for computer analysis. The WWSSN stations that are converted to DWWSSN stations with the DRS will continue to record the seismic data on photographic paper, as in the past, as well as record the seismic data in a digital format on magnetic tape. The magnetic tapes are sent to the United States for dissemination to world-wide seismic data users. The photographic records will also be sent back to the United States for microfilm copying. The GDSN digital tapes are processed by the Albuquerque Seismological Laboratory into digital day tapes. A day tape contains all the reporting GDSN stations seismic information for one day on a set of magnetic tapes. Normally, these digital day tapes are available to users in approximately 60 days after being recorded by the GDSN stations.

The DRS modification to WWSSN stations provides additional

improvements by replacing the electo-mechanical clocks with electronic digital time encoders and the solid state amplifier unit. The amplifier unit provides short-period, long-period, and new intermediate-period seismic data channels. This amplifier unit also drives the photographic recording galvanometers directly, which eliminates the LP galvanometer control boxes, and allows the LP galvanometers to be replaced with SP galvanometers, yet still providing the same WWSSN LP response.

The telemetered version of the WWSSN DRS allows many degrees of flexibility in system configuration. It is possible to use the telemetry equipment in conjunction with the WWSSN console or use it as a separate system with a stand-alone time encoder unit. The telemetered version allows the seismometer site to be separated from the central recording site. The remote system and the central system are connected together by a 2400-baud link such as a dedicated four-wire telephone circuit.

The digital data is converted at the central recording system into individual SP, IP, and LP analog channels for analog recording. One helicorder is provided with each DWWSSN system and any one of the converted analog channels may be displayed by switch selection of the desired channel.

2. BACKGROUND

The Digital Recording System (DRS) for telemetered DWWSSN stations uses similar microprocessors, hardware, and electronic subsystems as the regular DWWSSN DRS stations. The major system changes are in the operation and system software modifications. The DWWSSN DRS stations use two microprocessors for commmand and control of the DRS. The telemetered DWWSSN stations use five microprocessors and have a special multichannel digital-to-analog display unit as well as a programmable-current calibrator unit. In addition, the telemetered WWSSN DRS stations can be used a seperate system without the requirement of a WWSSN console for the Digital Time Encoder (DTE) unit. Software has been written for using either the DTE unit or a seperate commercial digital encoder system, such as the Systron Donner model 8110 Digital Clock with the digital options.

The initial requirement of the DWWSSN DRS was to only record the WWSSN seismic information, that is one short-period (SP) data channel and three long-period (LP) data channels. Early in the development cycle, the amplifier design took advantage of the broadband characteristics of the WWSSN LP seismomters and provided both the LP as well as intermediate-period (IP) data from one LP seismometer. This increased the number of data channels from four to nine; three LP channels, three IP channels, and three SP channels. Normally, only one SP channel (SPV) is recorded at a DWWSSN DRS station.

The final microprocessor selection was determined by capacity, speed, performance, and simultaneous operation with other microprooessor and radom-access memory (RAM) units. The initial four-channel design used a single-board 8080 microprocessor unit and a four-kilobit memory board. With three types of seismic data (SP, IP, and LP), each type having three

channels, and two of these types (IP and SP) requiring event detection programs, a much larger and faster microprocessor system was required. The option for event detection recording for IP and SP data, with pre-event data a requirement, created a unique queuing problem during a large event. As a result of this queuing problem, another microprocessor was assigned the task of queue master and magnetic-tape transport controller. The size the RAM memory board was increased to 16-kilobits in size. This 16-kilobit memory provides temporary storage for two LP records, three IP records, and three SP records in temporary memory. This size of memory provided for up to two pre-event records for IP and SP event recorded operation and eliminated the queuing problem. Normally, only one pre-event record is written for IP and SP events

The selection of the magnetic-tape recorders went from cartridge recorders to reel recorders as the design progressed.

The first analog-to-digital converter was a low cost 14-bit gain-ranged multichannel ADC unit, but it was changed early in the design by the seismic advisory panel's recommendation for a 16-bit straight binary multichannel ADC unit.

3. DWWSSN DRS TELEMETERED SYSTEM

3.1 GENERAL

A telemetered WWSSN DRS system, as shown in figure 3.1, consists of two major systems: a central system, and a remote system. The amplifier assembly and seismometer configuration is shown in figure 3.2. Normally the photographic recording equipment is not used at the remote system. The amplifier assembly is the same unit used with the WWSSN DRS systems and has the capability for providing WWSSN LP photo signals to the WWSSN galvanometers and photographic drum recorders.

The central system consists of: three microprocessors, RAM memory storage, digital time encoder, digital-to-analog display unit, magnetic-tape formatter and tape unit, 2400-baud modem, and control panel - all mounted in a standard 19-inch equipment rack. Microprocessor One has all timing, remote control code transmissions, data formatting, event detection, digital-to-analog display tasks, and overall control functions for both the central and remote system. Microprocessor Two controls the reception of all seismic data information from the remote system. Microprooessor Six controls the digital tape formatter and magnetic-tape recorder. The 16-kilobit RAM memory provides the temporary data storage for the last three short-period (SP) records, the last three intermediate-period (IP) records, and the last two long-period (LP) records. The digital-to-analog units converts all incoming digital data into analog traces for each of the system seismic channels. The control panel contains the necessary system switches for: system configuration, SP event detect parameters, IP event detect

parameters, telemetry line status checking characters, remote calibrations selection, and system start/reset control. The 2400-baud, telephone-line modem is for communication over the four-wire, full-duplex telephone circuit.

The remote system consists of: three microprocessors, 16-bit binary analog-to-digital converter, constant-current calibrations unit, and a 2400-baud modem. Microprocessor Three controls the reception of all of the ADC Codes, Calibration Codes, and Status Codes from the central system via the telephone modem circuit. It passes the appropriate codes to either Microprocessor Four, the ADC and transmission microprocessor, or Microprocessor Five, the calibration processor. Microprocessor Four uses the ADC code data to control the analog-to-digital converter as to type of data conversion, that is SP conversions, SP and IP conversions, or SP and LP conversions. During SP conversions; amplifier saturation (AMP SAT), telemetry status information, and calibration information are transmitted back to the central system. Microprocessor Five is the control for the WWSSN Programmable Current Calibrator which can provide various current levels for: SP daily calibrations, LP daily calibrations, SP step calibrations, LP step calibrations, SP response calibrations, IP response calibrations, LP response calibrations, and LP Photo response calibrations.

The WWSSN DRS telemetered system will process one SP channel, three IP channel, and three LP channels over a standard 2400-baud telephone line. The absolute telephone line delay is critical for successful operation. The maximum two way telephone line delay of 15-milliseconds or less will not cause system failures. This corresponds to approximately 300 circuit miles or less typically. Most telephone companies will only guarantee 50-milliseconds one way delay or 100-milliseconds two way absolute circuit delay. Before installation of this type of system, special telephone line delay tests should be conducted to insure the 15-millisecond or less absolute two way line delay is possible.

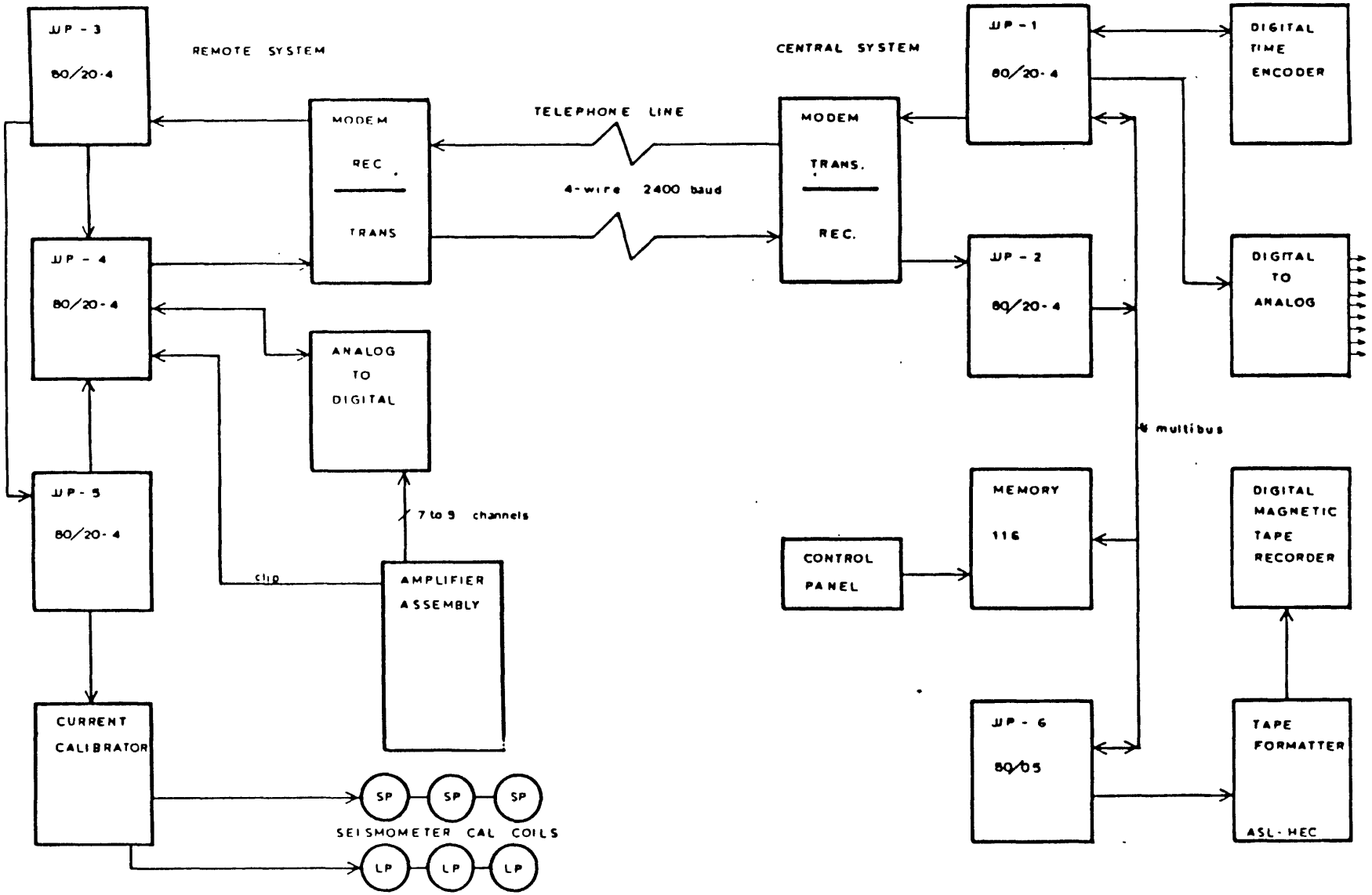


Figure 3.1 DWWSSN DRS TELEMETRY SYSTEM

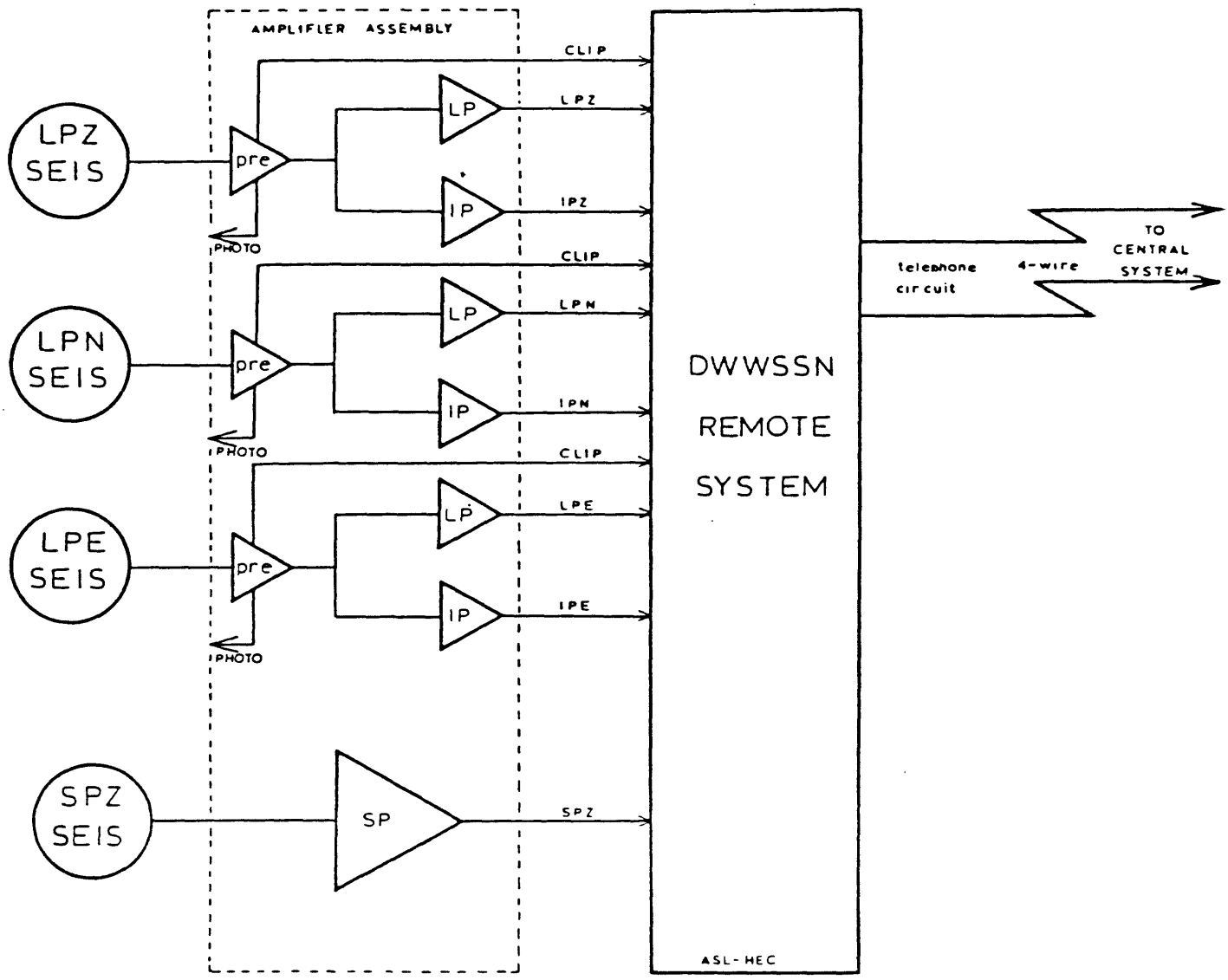


Figure 3.2 DWWSSN Amplifier and Seismometer Configuration

3.2 MICROPROCESSOR ONE

Microprocessor One is an 80/20-4, 8080 Central Processor Unit (CPU) based system. This microprocessor is the primary command and control unit for the entire DWWSSN DRS Telemetry System. Microprocessor One has all the time acquisition, timing control, ADC code transmission, telemetry status code transmission, data record formatting, SP event detection, IP event detection, record write control, DAC control, telemetry status verification, and overall system control. When Microprocessor One malfunctions the entire system malfunctions.

Microprocessor One receives a timing pulse from the Digital Time Encoder (DTE) every 50-milliseconds,which corresponds to a 20-sample-per-second time rate. A DRS time frame is 50-milliseconds in duration. All code transmission, data receiving, ADC verification, DAC functions, data formatting, and event detection must be completed within this time frame. At the beginning of every SP, IP, or LP data record, time information is obtained from the DTE. This time information is part of the header data. Figure 3.3 shows the format of this header information. Figure 3.4 shows the header and data placement within each data record. Records are 1000 words (2000 8-bit bytes) in length containing 10 words of header information and 990 words of binary data. Figure 3.5 shows the various SP, IP, and LP records in temporary memory. The number of records for each type of data provides for one or two pre-event records of SP or IP data at the beginning of event detection mode of recording and eliminates the queuing problem of writing a large number of different records at the same time during large earthquakes.

Four different ADC Codes are transmitted by Microprocessor One to the remote system's Microprocessor Three. The codes and the time sequencing are shown in figure 3.6. The pattern shown in figure 3.6 provides 20 SP conversions, 10 IP conversions, 1 LP, and system status functions for a one-second time frame.

This one-second time frame is repeated every second throughout the recording time period.

After the appropriate ADC Code, Calibration Code, or Telemetry Status is transmitted for the next time frame conversion; Microprocessor One reads header time for beginning new records according to the ADC Code just transmitted. Completed record addresses are sent to the SP, IP, or LP record write mailboxes. If SP or IP event-on flags are not set, no records will be written for this type of data. The first SP or IP set of records written for event detected events will have one pre-event record written first. This record will contain the event-on flag set in bit 4, byte 10 of the header. Microprocessor One will then process the data received from the remote system for the previous time frame. The receiving unit is Microprocessor Two, which stores the received data in a temporary memory location in the 116 RAM memory unit for use by Mioroprocessor One.

Microprocessor One first converts the received data as individual analog channels through the Digital-to-Analog Multiplex System which provides an analog output for each SP, IP, and LP seismic data channel. Next, Microprocessor One formats and stores the received data into appropriate SP, IP, or LP records. After formatting and storing the data, Microprocessor One checks the system configuration for continuous or event detection SP operation and for continuous or event detection IP operation. If the system is configured for either SP or IP event detection mode of operation, the appropriate SP and/or IP event detection algorithm is processed.

The system's configuration and SP or IP event detection settings can be set by front-panel thumbwheel switches as shown in figure 3.7. After the event detection process, Microprocessor One does the house keeping tasks such as Telemetry Status verification, ADC Code errors, and Calibraton Code generation. Then Microprocessor One returns to the beginning of the program to wait for the next 50-millisecond pulse from the DTE to start a new time frame and ADC sequence.

WORD 1	STATION I.D.	
	SAMPLE RATE	
WORD 2	1'S OF YEAR	100'S OF DAYS
	10'S OF DAYS	1'S OF DAYS
WORD 3	10'S OF HOURS	1'S OF HOURS
	10'S OF MINUTES	1'S OF MINUTES
WORD 4	10'S OF SECONDS	1'S OF SECONDS
	100'S OF MILLISEC.	10'S OF MILLISEC.
WORD 5	NUMBER OF CHANNELS PER RECORD	
	SYSTEM STATUS BYTE *	
WORD 6	DIGISWITCH #B (SP EVENT)	
	DIGISWITCH #C (IP EVENT)	
WORD 7	DIGISWITCH #D (CONFIGURATION)	
	CALIBRATON CODE	
WORD 8	ADC CODE ERROR TYPE 1	
	ADC CODE ERROR TYPE 2	
WORD 9	NOT USED	
	NOT USED	
WORD 10	NOT USED	
	NOT USED	

*Bit 0 = not used
Bit 1,2,3 = LP/IP Pre-Amp Saturation V,NS,EW.
Bit 4 = Event On Flag, beginning of event.
Bit 5,6 = not used.
Bit 7 = Calibration On Flag.

Figure 3.3 DRS HEADER RECORD INFORMATION

10 word header	990 words of data
1 10	11 1,000

Figure 3.4 DRS SP, IP, And LP DATA RECORDS (1000 words or 2000 8-bit bytes)

SHORT PERIOD RECORD #1	
0000	2,000
SHORT PERIOD RECORD #2	
2,001	4,000
SHORT PERIOD RECORD #3	
4,001	6,000
INTERMEDIATE PERIOD #1	
6,001	8,000
INTERMEDIATE PERIOD #2	
8,001	10,000
INTERMEDIATE PERIOD #3	
10,001	12,000
LONG PERIOD RECORD #1	
12,001	14,000
LONG PERIOD RECORD #2	
14,0001	16,000

Figure 3.5 DRS 16,000 RAM Memory Map

ADC CODE		TIME PERIOD (50 millisec.)	SP CHANNELS	IP CHANNELS	LP CHANNELS
11		1	1	3	
10		2	1		3
11		3	1	3	
12	*1	4	1		
11		5	1	3	
13	*2	6	1		
11		7	1	3	
12	*1	8	1		
11		9	1	3	
13	*2	10	1		
11		11	1	3	
12	*1	12	1		
11		13	1	3	
13	*2	14	1		
11		15	1	3	
12	*1	16	1		
11		17	1	3	
13	*2	18	1		
11		19	1	3	
12	*1	20	1		

*1 Time frame for CAL and AMP-SAT information being returned from remote system.

*2 Time frame for TELEMETRY STATUS information being sent and received.

Figure 3.6 DRS TELEMETRY ONE SECOND SEQUENCE SCHEDULE

Switch Position	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Switch T(Telemetry Test Value)	0	1	2	3	4	5	6	7	8	9	X don't use	X don't use	X don't use	X don't use	X don't use	X don't use
Switch B (SP event detection constants)																
KSP	2.67	3.20	2.46	3.20	3.56	2.46	3.05	3.56	2.46	2.91	3.20	3.56	2.29	2.67	3.20	4.00
STA SP	16	16	8	8	8	8	8	8	16	16	16	16	32	32	32	32
LTA SP	64	64	64	64	64	128	128	128	128	128	128	128	128	128	128	128
Switch C (IP event detection constants)	100	200	300	400	500	600	700	800	900	1000	1600	2200	2800	3600	4200	4800
Switch D	SP Ev.*	All SP	No SP	All SP	No SP	SP Ev.*	--Continuous LP only(no SP, no IP)----------								End of File Mark	
	IP Ev.*	No IP	All IP	All IP	IP Ev.*	No IP										
	All LP	All LP	All LP	All LP	All LP	All LP										

Note: SP off limit = 10 minutes, SP on limit = 30 minutes.

IP off limit = 12 minutes.

*"SP Ev." means only SP events, not continuous SP data, are recorded. (Same meaning for "IP Ev.")

Figure 3.7 THUMBWHEEL SWITCH SETTINGS

Microprocessor One transmits command codes to the remote system from its serial port through the 2400-baud modems and telephone circuit. Time requests and time information are exchanged with the DTE through a parallel port. Digital information is transferred to the Digital-to-Analog Multiplexer unit in a similar manner through a parallel port. Communication between Microprocessor One and Microprocessor Two or Microprocessor Six is by the multibus link to the 116 RAM Memory. Instructions are passed between microprocessors via "MAILBOX" messages placed in the 116 RAM Memory. Microprocessor One has the highest multibus priority, Microprocessor Two the next priority, and Microprocessor Six the lowest priority. The 116 RAM Memory has no processor functions and is a slave unit on the multibus.

The SP event detection algorithm was developed by Dr. L. G.

Holcomb of the USGS. His algorithm uses peak-to-peak data values of the SP seismic data. These peak-to-peak values are stored in a short-term array (STA) and in a long-term array (LTA). This data is first stored in the beginning of the STA array. As new data is received the older data shifts through STA and then through the LTA. The oldest data in the LTA is shifted out and no longer used. The length of these arrays are shown in figure 3.7 as "STA SP" and "LTA SP". These array lengths are decimal numbers representing the number of stored peak-to-peak values. The selection of thumbwheel Switch B will select one of the 16 different SP event-detection constants sets for STA, LTA, and KSP.

The LTA average data value multiplied by KSP will be compared with the the STA average data value. When the STA average exceeds the LTA * KSP average product, an event-on is declared. The LTA array is frozen for the duration of the event and only the STA values are allowed to change during the event. This algorithm will use the KSP * LTA average product to determine when the event (STA average) does not exceed the test value for ten minutes to declare the event-off condition.

The IP event detector uses IP event-detection constants selected by Switch C. This IP event detector is very simple in that any time the IPZ data value exceeds the IP constant, an IP event-on is declared. The event-off will take place after the IPZ data stays smaller than the IP constant for 12 minutes.

Switch D selects the system configuration as to continuous or event-detected data and to type of seismic data being recorded. All SP, IP, and LP data are being received and displayed at Central System, but only the selected seismic data are being recorded on the magnetic-tape recorder.

The 8080 program listing is presented in appendix A.1.

SECTION 3.3 MICROPROCESSOR TWO

Microprocessor Two is an 80/20-4, 8080 CPU based system. This microprocessor is the primary receiving unit for the DRS central system. Microprocessor Two's function is to receive the 2400-baud data transmission from the remote system through the modems and telephone network. Every 50-millisecond time frame, Microprocessor Two receives two synchronization bytes and nine data bytes. After receiving the eleven bytes, the nine data bytes are transferred to the 116 RAM memory for processing by Microprocessor One. Figure 3.8 shows the temporary storage of these nine data bytes in Microprocessor Two's RAM area. Figure 3.9 shows the transfer location of these nine data bytes into the 116 RAM area. The serial transmission operation of the 80/20-4 units adds one additional parity bit to every eight-bit byte that is transmitted. The time required to receive the eleven bytes of information is 41.25-milliseconds. The two synchronization bytes must be received perfectly before any data bytes will be accepted. These two synchronization bytes define the sync word for proper frame start operation.

The first data byte is the ADC Code associated with this data frame. The next two data bytes are the single SP vertical data. Depending upon what data frame and ADC Code, the next six data bytes will be either: IPV, IPNS, IPEW, or LPV, LPNS, LPEW, or CALIBRATION CODE, AMP SAT, or TELEMETRY STATUS INFORMATION. In the transmission of CALIBRATION CODE, AMP SAT, OR TELEMETRY STATUS, unused data bytes are transmitted as zeros.

The 8080 program listing is presented in appendix A.2.

UP-2	RAM	
ADDRESS	BYTE #	TYPE OF DATA
38FF	BYTE 1	ADC CODE.
3900	BYTE 2	MSB SP.
3901	BYTE 3	LSB SP.
3902	BYTE 4	MSB LPV, LPV, AMP SAT, TEL STAT.
3903	BYTE 5	LSB LPV, IPV, CAL CODE.
3904	BYTE 6	MSB LPNS, IPNS.
3905	BYTE 7	LSB LPNS, IPNS.
3906	BYTE 8	MSB LPEW, IPEW.
3907	BYTE 9	LSB LPEW, IPEW.

Figure 3.8 MICROPROCESSOR TWO RAM RECEIVE AREA

UP-2 RAM ›››››››	TRANSFER TO ›››››	116 MEMORY RAM
ADDRESS	BYTE #	ADDRESS
38FF	BYTE 1	FF00.
3900	BYTE 2	FF01
3901	BYTE 3	FFO2
3902	BYTE 4	FF03
3903	BYTE 5	FF04
3904	BYTE 6	FFO5
3905	BYTE 7	FF06
3906	BYTE 8	FF07
3907	BYTE 9	FF08

Figure 3.9 MICROPROCESSOR TWO RAM TRANSFER TO 116 RAM

SECTION 3.4 MICROPROCESSOR THREE

Microprocessor Three is an 80/20-4, 8080 CPU based system. This microprocessor is the primary receiving unit for the DRS remote system. Microprocessor Three's function is to receive the 2400-baud, command-control code transmission from the central system through the modems and telephone network. At the beginning of every 50-millisecond time frame, Microprocessor Three receives two synchronization bytes and two command-code bytes. After receiving the four bytes, the ADC Codes and TELEMETRY STATUS are transferred to Microprocessor Four. Calibration codes are transferred to Microprocessor Five. Transfer of information between Microprocessors Three, Four, and Five is accomplished by parallel port to parallel port communication rather than the multibus communication. With the multibus technique, microprocessors can exchange information with "SLAVE" units such as 116 RAM memory boards but not directly with other microprocessors or "MASTERS".

The 8080 program listing is presented in appendix A.3.

SECTION 3.5 MICROPROCESSOR FOUR

Microprocessor Four is an 80/20-4, 8080 CPU based system. This microprocessor is the primary transmitting unit for the DRS remote system. Microprocessor Four's function is analog-to-digital conversion of the appropriate seismic channels and transmission of the 2400-baud data to the central system through the modems and telephone network. Every 50-millisecond time frame, Microprocessor Four receives one or two command code bytes for proper ADC conversion. The second byte transfer occurs during the "13" ADC conversion time period and is the TELEMETRY STATUS byte that was received from the central system and will be echo transmitted back to the central system for telemetry verification. Figure 3.10 shows the Microprocessor Four's RAM location of transmitted data bytes. Two synchronization bytes are transmitted first to provide proper frame start operation. The serial transmission operation of the 80/20-4 units adds one additional parity bit to every eight-bit byte that is transmitted. The time required to transmit the eleven bytes of information is 41.25-milliseconds. The first data byte is the ADC Code associated with this data frame. The next two data bytes are SP vertical data. Depending upon what data frame and ADC Code, the next six data bytes will be either: IPV, IPNS, IPEW, or LPV, LPNS, LPEW, or CALIBRATION CODE, AMP SAT, or TELEMETRY STATUS INFORMATION. In the transmission of CALIBRATION CODE, AMP SAT, OR TELEMETRY STATUS, unused data bytes are transmitted as zeros.

In addition to digitized seismic data being transmitted back to the central system, other status information is transmitted back during certain ADC-Code time frames. The TELEMETRY STATUS information is echo transmitted back during the ADC-Code-13 time frame. Every ADC-Code-12 time frame has the CALIBRATION and

AMPLIFIER SATURATION information transmitted back to the central system. Any calibration in progress by the Remote Programmable Current Calibrator will be identified by calibration code number. The LP and IP preamplifier sections are monitored for saturation or clipping conditions. Preamplifier saturation or non-saturation information is transmitted back to the central system.

The 8080 program listing is presented in appendix A.4.

UP-4	RAM	
ADDRESS	BYTE #	TYPE OF DATA
38FF	BYTE 1	ADC CODE.
3900	BYTE 2	MSB SP.
3901	BYTE 3	LSB SP.
3902	BYTE 4	MSB LPV, LPV, AMP SAT, TEL STAT.
3903	BYTE 5	LSB LPV, IPV, CAL CODE.
3904	BYTE 6	MSB LPNS, IPNS.
3905	BYTE 7	LSB LPNS, IPNS.
3906	BYTE 8	MSB LPEW, IPEW.
3907	BYTE 9	LSB LPEW, IPEW.

Figure 3.10 MICROPROCESSOR FOUR RAM RECEIVE AREA

SECTION 3.6 MICROPROCESSOR FIVE

Microprocessor Five is an 80/20-4, 8080 CPU based system. This microprocessor is the control unit for the DWWSSN Programmable Current Calibrator. Calibration Codes are activated, from the central system, by operator selection of the desired levels and types of calibration from the front panel thumbwheel switches and manually pressing the "ACTIVATE SWITCH". These Calibration Codes are transmitted to the remote system's Microprocessor Three. Microprocessor Three then passes the Calibration Codes to Microprocessor Five, whioh uses these Calibration Codes to select one of 29 calibration programs. The Programmable Current Calibrator uses these 29 programs to synthesize: step, daily sine, and full frequency response calibration signals for DWWSSN SP, IP, LP, LPP (photo) equipment. One of these codes is "ABORT", which immediately terminates any calibration in process. This function allows the central system operator to stop calibrations in the event of seismic activity or wrong calibrations.

The Programmable Current Calibrator has nine calibration functions. These funotions are:

* LP Step
* SP Step
* LP Daily (LP, IP, LPP Sine)
* SP Daily (SP Sine)
* LP Response
* SP Response
* IP Response
* LPP Response
* ABORT

An operator can initiate calibrations by selecting one of the eight calibration functions or the ABORT function and the appropriate current level with the six thumbwheel switches (S1, S2, S3, S4, S5, or S6). The calibration sequence is activated by the operator pressing the "ACTIVATE SWITCH" next to the first six switches within the Calibrator Control area of the central system control panel. See figure 3.11 and figure 3.12 for the calibrator control switch layout.

Within 200-milliseconds after calibration activation, the CAL WORD is transmitted with every "ADC-CODE-12" transmission from the central system to the remote system. The ADC Code sequence is shown in figure 3.6.

Table 3.1 shows the various function types, current levels, switch positions, ADC Codes, and run times for all possible commands of the current calibrator. Specific information on each function type is presented in tables 3.2 through 3.9.

Due to the size of the Current Calibrator program the flow charts and the 8080 program listing are presented in a separate USGS report.

Another use of the calibrator is in trouble shooting the DRS TELEMETRY SYSTEM. All Calibration Codes, selected by the central system operator, are transmitted to and displayed on the remote calibrator panel as to type of calibration and the calibration level. This display will verify the central system transmit, half the modem and telephone circuit, and the remote system receive circuits. Receiving the TELEMETRY STATUS at the central system verifies the other half of the system circuits. Activation of the "ABORT" function will cause all of the displays on the remote system calibrator panel to blink. As long as the central system operator holds the activation button down in the "ABORT" function the lights will blink. Using this characteristic, it is possible for the central system operator to signal to personnel at the remote system. Predetermined code patterns can be used to indicate such items as: start test, signal received, data no good, and so on. When there is no

telephone or radio communication between the central and remote systems, this provides some means of exchanging instruotions. It is also possible for the remote system personnel to signal the central system by the use a battery or some voltage souroe (one to ten volts) applied to a predetermined ADC seismio channel input.The central system operator can monitor the predetermined seismic channel on the system helicorder and observe the signal level pattern. During the initial checkout of the Berkeley - Jamestown installation, the above techniques were used with good success.

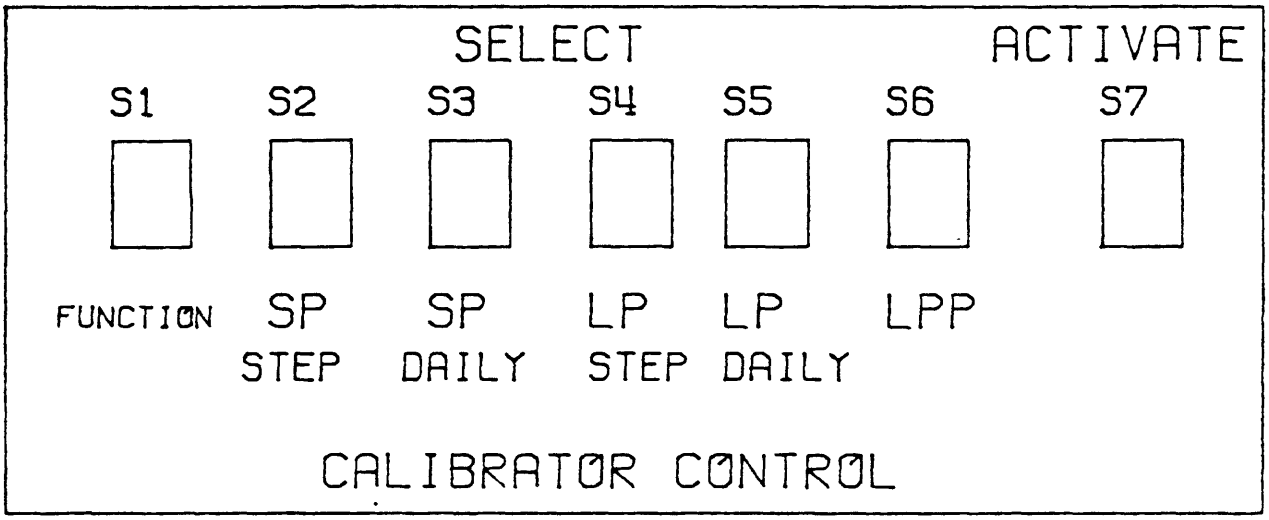


FIGURE 3.11 CALIBRATOR CONTROL SWITCH LAYOUT

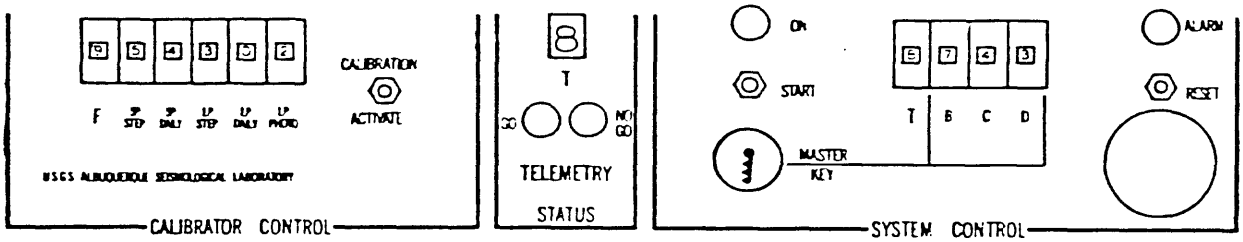


Figure 3.12 CENTRAL SYSTEM'S CONTROL PANEL

FUNCTION TYPE		CURRENT MILLIAMPS	SWITCH POSITIONS	ADC CODE	RUN TIME
ABORT		ABORT	S1=1,S4=0	E0	
LP STEP		0.1	S1=1,S4=1	25	5 MINUTES
LP STEP		0.2	S1=1,S4=2	24	5 MINUTES
LP STEP		0.4	S1=1,S4=3	23	5 MINUTES
LP STEP		0.8	S1=1,S4=4	22	5 MINUTES
LP STEP		1.6	S1=1,S4=5	21	5 MINUTES
LP STEP		3.2	S1=1,S4=6	20	5 MINUTES
SP STEP		ABORT	S1=2,S2=0	E0	
SP STEP		0.8	S1=2,S2=1	83	80 SEC.
SP STEP		1.6	S1=2,S2=2	82	80 SEC.
SP STEP		3.2	S1=2,S2=3	81	80 SEC.
SP STEP		6.4	S1=2,S2=4	80	80 SEC.
LP DAILY		ABORT	S1=3,S5=0	E0	
LP DAILY	*1	LPP=.293	S1=3,S5=1	26	9 MINUTES
LP DAILY	*1	LPP=.585	S1=3,S5=2	27	9 MINUTES
LP DAILY	*1	LPP=1.17	S1=3,S5=3	28	9 MINUTES
LP DAILY	*1	LPP=2.34	S1=3,S5=4	29	9 MINUTES
LP DAILY	*1	LPP=4.68	S1=3,S5=5	2A	9 MINUTES
	*1 LP=0.506 IP=78.960				
SP DAILY		ABORT	S1=4,S3=0	E0	
SP DAILY		0.531	S1=4,S3=1	88	1 MINUTE
SP DAILY		1.061	S1=4,S3=2	87	1 MINUTE
SP DAILY		2.122	S1=4,S3=3	86	1 MINUTE
SP DAILY		4.244	S1=4,S3=4	85	1 MINUTE
SP DAILY		8.488	S1=4,S3=5	84	1 MINUTE
LP SWEEP		0.506	S1=5	4B	79 MINUTES 54 SEC.
SP SWEEP		8.488	S1=6	89	16 MINUTES 5 SEC.
IP SWEEP		78.96	S1=7	40	48 MINUTES 59 SEC.
LPP SWEEP		ABORT	S1=8,S6=0	E0	
LPP SWEEP		293	S1=8,S6=1	2B	51 MINUTES 59 SEC
LPP SWEEP		.585	S1=8,S6=2	2C	51 MINUTES 59 SEC.
LPP SWEEP		1.17	S1=8,S6=3	2D	51 MINUTES 59 SEC.
LPP SWEEP		2.34	S1=8,S6=4	2E	51 MINUTES 59 SEC.
LPP SWEEP		4.68	S1=8,S6=5	2F	51 MINUTES 59 SEC.
ABORT			S1=9	E0	
ABORT			S1=10	E0	
ABORT			S1=13	E0	
ABORT			S1=14	E0	
ABORT			S1=15	E0	
TEST1			S1=11	E1	
TEST2			S1=12	E2	

TABLE 3.1 CALIBRATOR THUMBWHEEL SWITCH SETTINGS

LP STEP FUNCTION (S2=1 AND S4=1 TO 6)

CURRENT LEVELS MA ZERO-PEAK	DURATION MINUTES	NUMBER OF CYCLES	SWITCH S4 SETTING
0.1	5	1	1
0.2	5	1	2
0.4	5	1	3
0.8	5	1	4
1.6	5	1	5
3.2	5	1	6

TABLE 3.6.2 LP STEP FUNCTION

SP STEP FUNCTION (S1= A2 AND S2=1 TO 4)

CURRENT LEVELS MA ZERO-PEAK	DURATION SECONDS	NUMBER OF CYCLES	SWITCH S2 SETTING
0.8	80	4	1
1.6	80	4	2
3.2	80	4	3
6.4	80	4	4

SP STEP DURATION IS ON FOR 10 SECONDS AND OFF FOR 10 SECONDS.
THERE ARE FOUR REPETITIONS OF ON-OFF CYCLES.

TABLE 3.3 SP STEP FUNCTION

LP DAILY (LPP/LP/IP) SINE FUNCTION (S1=3 AND S6=1 TO 5)

	CURRENT LEVELS MA PEAK-PEAK		PERIOD SECONDS	DURATION MINUTES	NUMBER OF CYCLES	SWITCH S6 SETTING
	0.2925	LPP	15	3	12	1
SWITCH	0.5850	LPP	15	3	12	2
SELECTABLE	1.170	LPP	15	3	12	3
LEVELS	2.340	LPP	15	3	12	4
	4.680	LPP	15	3	12	5
FIXED	0.506	LP	25	5	12	
LEVELS	78.960	IP	1	1	60	

LP DAILY SIGNAL DURATION IS 9 MINUTES TOTAL

TABLE 3.4 LP DAILY (LPP/LP/IP) SINE FUNCTION

SP DAILY (SINE) FUNCTION (S1=4 AND S3=1 TO 5)

	CURRENT LEVELS MA PEAK-PEAK	PERIOD SECONDS	DURATION MINUTES	NUMBER OF CYCLES	SWITCH S3 SETTING
	0.531	1	1	60	1
SWITCH	1.061	1	1	60	2
SELECTABLE	2.122	1	1	60	3
LEVELS	4.244	1	1	60	4
	8.488	1	1	60	5

SP DAILY SIGNAL DURATION IS 1 MINUTE TOTAL

TABLE 3.5 SP DAILY SINE FUNCTION

LP FREQUENCY RESPONSE FUNCTION (FREQUENCY SWEEP S1=5)

CURRENT LEVEL MA PEAK-PEAK	PERIOD SECONDS	DURATION MINUTES	NUMBER OF CYCLES	PERIOD CODE
0.506	500	25	3	13
0.506	200	10	3	12
0.506	100	10	6	11
0.506	80	8	6	10
0.506	60	6	6	9
0.506	50	5	6	8
0.506	40	4	6	7
0.506	30	3	6	6
0.506	25	2.92	7	5
0.506	20	2	6	4
0.506	15	2	8	3
0.506	10	1	6	2
0.506	8	1.07	8	1

LP RESPONSE RUN TIME IS 79 MINUTES AND 54 SECONDS.

TABLE 3.6 LP FREQUENCY RESPONSE FUNCTION

SP FREQUENCY RESPONSE FUNCTION (FREQUENCY SWEEP S1=6)

CURRENT LEVEL MA PEAK-PEAK	PERIOD SECONDS	DURATION MINUTES	NUMBER OF CYCLES	PERIOD CODE
8.488	10	1	6	16
8.488	8	1	8	15
8.488	6	1	10	14
8.488	5	1	12	13
8.488	4	1	15	12
8.488	3.2	1	19	11
8.488	2	1	30	10
8.488	1.5	1	40	9
8.488	1	1	60	8
8.488	0.8	1	75	7
8.488	0.7	1	86	6
8.488	0.6	1	100	5
8.488	0.5	1	120	4
8.488	0.4	1	150	3
8.488	0.3	1	200	2
8.488	0.2	1	300	1

SP RESPONSE RUN TIME IS 16 MINUTES AND 5 SECONDS.

TABLE 3.7 SP FREQUENCY RESPONSE FUNCTION

IP FREQUENCY RESPONSE FUNCTION (FREQUENCY SWEEP S1=7)

CURRENT LEVEL MA PEAK-PEAK	PERIOD SECONDS	DURATION MINUTES	NUMBER OF CYCLES	PERIOD CODE
78.96	100	10	6	19
78.96	80	8	6	18
78.96	60	6	6	17
78.96	40	4	6	16
78.96	30	3	6	15
78.96	25	2.5	6	14
78.96	20	2	6	13
78.96	15	1.5	6	12
78.96	10	1	6	11
78.96	8	1.33	10	10
78.96	6	1	10	9
78.96	4	1	15	8
78.96	3	1	20	7
78.96	2	1	30	6
78.96	1.5	1	40	5
78.96	1	1	60	4
78.96	0.8	1	75	3
78.96	0.6	1	1	2
78.96	0.5	1	1	1

IP RESPONSE RUN TIME IS 48 MINUTES AND 59 SECONDS.

TABLE 3 8 IP FREQUENCY RESPONSE FUNCTION

LPP FREQUENCY RESPONSE FUNCTION (FREQUENCY SWEEP S1=8 AND S6=1 TO 5)

CURRENT LEVEL MA PEAK-PEAK	PERIOD SECONDS	DURATION MINUTES	NUMBER OF CYCLES	PERIOD CODE
2*I	200	10	3	13
2*I	100	10	6	12
2*I	80	8	6	11
2*I	60	5	5	10
2*I	40	4	6	9
2*I	30	3	6	8
I	25	2.92	7	7
I	20	2	6	6
I	15	2	8	5
I	10	1	6	4
I	8	1.07	8	3
I	6	1	10	2
I	5	1	12	1

CURRENT I	SWITCH S6 SETTING	ADC CODE
I=0.2925	1	2B
I=0.5850	2	2C
I=1.1700	3	2D
I=2.3400	4	2E
I=4.6800	5	2F

LPP RESPONSE RUN TIME IS 51 MINUTES AND 59 SECONDS.

TABLE 3.9 LPP FREQUENCY RESPONSE FUNCTION

SECTION 3.7 MICROPROCESSOR SIX

Microprccessor Six is an 80/05 microprocessor unit, which is an 8085 CPU based system. This microprocessor is the magnetic-tape formatter and magnetic-tape controller. The 8085 CPU microprocessor was used because it has faster CPU operational speed than the 8080 CPU units. This faster speed is required for the fast operational speed of the magnetic-tape units.

Microprocessor Six monitors the SP, IP, and LP Record Pointer mailboxes in the 116 RAM memory for addresses of records to be written on magnetic tape. Microprocessor Six scans the one LP, three SP, and three IP Record Pointer "MAILBOXS" for the end-of-record addresses. When Microprocessor Six finds a mailbox that is not zero data value, it extracts the address information and replaces it with zeros. These mailboxes are listed in table 5.1 (RAM locations FE86 through FE93).

Because of the possibility of event detected recordings for SP or IP data, three mailboxes were provided for each type. The three mailboxes for each type of data provides either one or two pre-event records to be written at the beginning of event detected events. Normally only one pre-event record is written.

Microprocessor Six transfers the appropriate record data from the 116 RAM memory to the magnetic-tape formatter, which in turn transfers the data to the magnetic-tape transport.

During system checkout, the only way to test these mailbox locations is to remove Microprocessor Six. This is because it scans these mailboxes at a very fast rate, removes the address data, and resets the mailboxes to zero. The 8085 program listing is presented in appendix A.5.

4. DWWSSN DRS TELEMETERED SYSTEM ASSEMBLY INFORMATION

4.1 GENERAL

The WWSSN DRS Telemetry System uses 80/20-4 microprocessor units for five of the six system microprocessors. The sixth is an 80/05 microprocessor which was seleoted because of the higher speed required for the controller of the magnetic-tape formatter unit. Each microprocessor is custom configured for its function by switch and jumper set-up. There are approximately 150 jumpers on an 80/20-4 board. Specific operation such as port input or output, RAM address, EPROM type, and many special operational assignments are setup by jumper selection. Operational success depends upon every jumper being correct. Not all board functions are required by a particular processor so some jumpers are not critical, in fact they can be treated as "DON'T CARES".

4.2 ASSEMBLY INFORMATION

The factory installed jumpers for an 80/20-4 microprocessor board are shown in table 4.1. Table 4.2 through table 4.6 present the respective 80/20-4 microprocessor jumper changes or additions to the initial jumper list. Table 4.7 presents the jumper list for the single 80/05 microprocessor board. Table 4.8 presents the jumper list for the 116 memory board. This 116 memory board is a combination memory board and I/O input/output board that must be configured for proper operation.

Table 4.9 shows the SBC 655 chassis with its B-N priority jumper and the proper slot assignment for each of the microprocessors or memory boards. The two SBC 655 chassis have

been modified in several ways. One change is to disable the front panel interrupt switch and use it for activation of the Digital Time Encoder (DTE) ready relay. Other changes are special TTL +5 volt power connector used by the Calibrator Unit and DTE ready relay assembly.

Table 4.10 through table 4.16 show the respective I/O input/out terminators for all ports. The SN74125 must be installed in a special plug-in carrier and modified for use in the 80/05 terminator plug-in. The write clock pulse from the magnetic-tape formatter is echo transmitted back to the formatter as a data-available strobe, as well as entering the 80/05 for sequencing of the data to be written on magnetic tape.

The 901 terminator device provides four 220/330 ohm pull-up/pull-down circuits per terminator pack. The 902 provides four, one kilohm pull-up circuits per pack. The solid terminator devices are plug-in carrier units that are jumpered straight through for all data bit lines.

Table 4.17 through table 4.24 presents the respective microprocessor port wire/cable assignments. Table 4.25 and table 4.26 presents the SBC 116 memory board port wire/cable assignments. Microprocessor Two does not have any port assignments.

Table 4.28 presents the RS232C port wire/cable assignments for Microprocessor One, Two, Three, and Four. These RS232C ports are connected to the 2400-baud digital modems. The 2400-baud modems are connected to a dedicated four-wire telephone circuit. The transmit modems are hard-wired for continuous transmit. The receive modems are in a continuous receive mode. With a 50-millisecond data frame, a modem's 8.5 or especially the 150-millisecond turn-around / clear-to-send time cannot be tolerated. So continuous transmit and receive techniques were used.

Figure 4.1 shows the modification to the SBC 655 chassis which eliminates the front panel interrupt capability and provides modification for use of this switch as a system "START-UP SEQUENCE SWITCH". Figure 4.2 shows the front panel and chassis interconnect schematic.

DRS TELEMETRY 80/20-4

FACTORY JUMPERS

INSTALLED	NO CONNECTION
16-18	1-2
19-21	3-4
25-45	9-10
26-35	22-23
52-53	135-136
71-72	14,5,15,13
91-92	96,97,90,89
93-94-95	E3 A-B
108-109	
110-111	
112-113	
120-121	
128-129	
137-138	
141-142	
W1 B-E	
W1 A-D	
W1 C-F	
W2 A-C	
W4 B-D	
W4 C-E	
W5 A-B	
W6 B-C	
W7 A-B	
W8 A-C	

"W" SWITCHES CONFIGURED FOR 4K PROM (2708 EPROMS)

TABLE 4.1 80/20-4 FACTORY INSTALLED JUMPERS

DRS TELEMETRY 80/20-4

MICROPROCESSOR ONE
(UP-1)

REMOVE	INSTALL	CHECK CONNECTED	NONE
19-21	20-21	52-53	1-2
71-72	70-71	54-55	3-4
W2 A-C	W2 A-B	56-57	9-10
W4 B-D	W4 A-D	58-59	11-12
W4 C-E	W4 B-E	60-61	4,5,13,15
W7 A-B	W7 A-D	62-63	6,7,8
W8 A-C	W8 A-B	64-65	
*CAP35	31-36	66-67	
*CAP53	36-37	68-69	
*CAP72	37-38	73-74	
	38-39	75-76	
		77-78	
		79-80	
		81-82	
		83-84	
		85-86	
		87-88	
		91-92	
		108-109	
		120-121	
		128-129	

"W" SWITCHES CONFIGURED FOR 8K EPROM (2716 EPROMS)

Note the 80/20-4 should be jumpered
as it comes from the factory.

TABLE 4.2 80/20-4 MICROPROCESSOR ONE JUMPERS

DRS TELEMETRY 80/20-4

MICROPROCESSOR TWO
(UP-2)

REMOVE	INSTALL	CHECK CONNECTED	NONE
16-18	17-18	52-53	1-2
24 TO 50	31-36	54-55	3-4
110-111	36-37	56-57	9-10
112-113	37-38	58-59	11-12
	38-39	60-61	4,5,13,15
	34-27	62-63	6,7,8
	35-26	64-65	
		66-67	
		68-69	
		73-74	
		75-76	
		77-78	
		79-80	
		81-82	
		83-84	
		85-86	
		87-88	
		91-92	
		108-109	
		120-121	
		128-129	
		71-72	

"W" SWITCHES SHOULD BE CONFIGURED FOR 4K EPROM (2708)EPROMS)

Note the 80/20-4 should be initially jumpered as it comes from the factory.

TABLE 4.3 80/20-4 MICROPROCESSOR TWO JUMPERS

DRS TELEMETRY 80/20-4

MICROPROCESSOR THREE
(UP-3)

REMOVE	INSTALL	CHECK CONNECTED	NONE
16-18	17-18	52-53	1-2
24 TO 50	31-36	54-55	3-4
	36-37	56-57	9-10
	37-38	58-59	11-12
	38-39	60-61	4,5,13,15
	34-27	62-63	6,7,8
	35-26	64-65	
		66-67	
		68-69	
		73-74	
		75-76	
		77-78	
		79-80	
		81-82	
		83-84	
		85-86	
		87-88	
		91-92	
		108-109	
		120-121	
		128-129	
		71-72	

"W" SWITCHES SHOULD BE CONFIGURED FOR 4K EPROM (2708)EPROMS)

Note the 80/20-4 should be initially jumpered as it comes from the factory.

TABLE 4.4 80/20-4 MICROPROCESSOR THREE JUMPERS

DRS TELEMETRY 80/20-4

MICROPROCESSOR FOUR (UP-4)

REMOVE	INSTALL	CHECK CONNECTED	NONE
19-21	20-21	51-52	1-2
24 TO 50	31-36	54-55	3-4
52-53	36-37	56-57	9-10
71-72	37-38	58-59	11-12
110-111	38-39	60-61	4,5,13,15
112-113	51-52	62-63	6,7,8
	70-71	64-65	
		66-67	
		68-69	
		73-74	
		75-76	
		77-78	
		79-80	
		81-82	
		83-84	
		85-86	
		87-88	
		91-92	
		108-109	
		120-121	
		128-129	

"W" SWITCHES SHOULD BE CONFIGURED FOR 4K EPROM (2708)EPROMS)

Note the 80/20-4 should be initially jumpered as it comes from the factory.

TABLE 4 5 80/20-4 MICROPROCESSOR FOUR JUMPERS

DRS TELEMETRY 80/20-4

MICROPROCESSOR FIVE
(UP-5)

REMOVE	INSTALL	CHECK CONNECTED	NONE
16-18	24-31	52-53	1-2
19-21	24-26	54-55	3-4
24 TO 50	26-27	56-57	9-10
68-69	27-28	58-59	11-12
93-94	28-29	60-61	6,7,8
110-111	29-30	62-63	5,13,14,15
112-113	30-36	64-65	16,17,18
141-142	36-37	66-67	19,20,21
W2 A-C	37-38	71-72	22-23
W4 B-D	38-39	73-74	32,33,35
W4 C-E	25-34	75-76	40,41,42,43
W7 A-B	52-68	77-78	44,45,46,47
W8 A-C	69-93	79-80	48,49,50
*CAP35	141-143	81-82	68-69
*CAP53	W2 A-B	83-84	92,90,96,97
*CAP72	W4 A-D	85-86	117,118,119
	W4 B-E	87-88	135-136
	W7 A-D	91-92	144-145
	W8 A-B	94-95	W1 H
		120-121	W2 C
		137-138	W3 A-B
		W1 A-D	W4 C
		W1 B-E	W6 A
		WI C-F	
		W5 A-B	
		W6 C-B	

"W" SWITCHES SHOULD BE CONFIGURED FOR 8K EPROM (2716)EPROMS)

Note the 80/20-4 should be initially jumpered as it comes from the factory.

TABLE 4.6 80/20-4 MICROPROCESSOR FIVE JUMPERS

DRS TELEMETRY 80/05

MICROPROCESSOR SIX
(UP-6)

REMOVE	INSTALL	CHECK CONNECTED	NONE
W3 A-B	W4 A-B	W1 A-D	W3 A-B
W3 C-D	W4 C-D	W1 B-C	W3 C-D
W3 E-F	W4 E-F	W2 B-C	W3 E-F
W3* G-H	W4 G-H	W5 A-F	W3 G-H
W7 A-B		W5 E-M	W7 A-B
W8 A-B		W10 A-B	W8 A-B
W11 A-B	W11 B-C	W12 A-B	W5 K,L,N
		W13 A-B	W5 P,R,S
		W6 A-B	W11 A
			W6 C
			W12 C
			W13 C

"W" SWITCHES SHOULD BE CONFIGURED FOR 4K EPROM (2708)EPROMS)

Note the 80/05 should be initially jumpered as it comes from the factory.

TABLE 4.7 80/05 MICROPROCESSOR SIX JUMPERS

DRS TELEMETRY SBC 116

RANDOM ACCESS MEMORY BOARD (MEMORY 116)

REMOVE	INSTALL	CHECK CONNECTED	NONE
30-31	29-30	32-33	15,16,17,18
52-53	53-54	34-35	19,20,21,22
89-90	90-91	36-37	75,76,77,78
S2 1-4	S2 1-2	38-39	95-112
		40-41	96-111
		42-43	97-110
		44-45	98-109
		46-47	99-108
		48-49	100-107
		50-51	101-106
		55-56	102-105
		57-58	103-104
		59-60	
		61-62	
		63-64	
		65-66	
		67-68	
		69-70	
		71-72	
		73-74	
		87-88	
		92-93	
		W1 H-E	W1 A,B,C,D,F
		W2 B-D	W8 A-B
		W2 C-E	
		W3 B-C	
		W4 A-B	
		W5 A-B	
		W6 A-B	
		W7 A-E	
		W9 A-B	
		W10 A-B	

SET S3 1,2,3,4 TO "ON".
SET S3 5,6,7,8 TO "OFF".

SET S4 1,2,4,5,6,7,8, TO "ON".
SET S4 3 TO "OFF".

"W" SWITCHES SHOULD BE CONFIGURED FOR 4K EPROM (2708)EPROMS)

Note the SBC 116 should be initially jumpered as it comes from the factory.

TABLE 4.8 SBC 116 MEMORY BOARD JUMPERS

DRS TELEMETRY SBC 655

SBC 655 SYSTEM CHASSIS CENTRAL RECORDING SYSTEM
(604 CARD CAGE JUMPER B-N)

PRIORITY	SLOT	MICROPROCESSOR	RESET P2 CONNECTOR
1	J2	UP-1	P2 INSTALLLED
2	J3	UP-2	
3	J4	UP-3	
4	J5	116 MEMORY	

SBC 655 CHASSIS REMOTE RECORDING SYSTEM
(604 CARD CAGE JUMPER B-N)

PRIORITY	SLOT	MICROPROCESSOR	RESET P2
N/A	J2	UP-3	P2 INSTALLED
N/A	J3	UP-4	
N/A	J4	UP-5	

NOTE. Priority scheme is for Central recording System only. Remote sysytem does not use "multibus", so no priority is used. Both 655 chassis assemblies are constructed and wired identical.

TABLE 4.9 655 CHASSIS SLOT ASSIGNMENT AND PRIORITY

DRS TELEMETRY
80/20-4 TERMINATORS

MICROPROCESSOR ONE
(UP-1)

CONNECTOR	PORT	TERMINATOR	DEVICE
J1	E4	A1	INTEL 8226
J1	E4	A2	INTEL 8226
J1	E6	A3	902
J1	E6	A4	902
J1	E5	A5	902
J1	E5	A6	902
J2	E8	A7	INTEL 8226
J2	E8	A8	INTEL 8226
J2	EA	A9	SN7437
J2	EA	A10	SN7437
J2	E9	A11	SOLID
J2	E9	A12	SOLID

Note the INTEL 8226 terminators are factory installed.
901 is 220/330 ohm pull-up/pull-down terminating pack.
902 is 1K ohm pull-up terminating pack.

TABLE 4.10 80/20-4 MICROPROCESSOR ONE TERMINATORS

DRS TELEMETRY
80/20-4 TERMINATORS

MICROPROCESSOR TWO
(UP-2)

CONNECTOR	PORT	TERMINATOR	DEVICE
J1	E4	A1	INTEL 8226
J1	E4	A2	INTEL 8226
J1	E6	A3	BLANK
J1	E6	A4	BLANK
J1	E5	A5	BLANK
J1	E5	A6	BLANK
J2	E8	A7	INTEL 8226
J2	E8	A8	INTEL 8226
J2	EA	A9	BLANK
J2	EA	A10	BLANK
J2	E9	A11	BLANK
J2	E9	A12	BLANK

Note the INTEL 8226 terminators are factory installed.
No ports are used as input/output on this microprocessor

TABLE 4.11 80/20-4 MICROPROCESSOR TWO TERMINATORS

DRS TELEMETRY
80/20-4 TERMINATORS

MICROPROCESSOR THREE
(UP-3)

CONNECTOR	PORT	TERMINATOR	DEVICE
J1	E4	A1	INTEL 8226
J1	E4	A2	INTEL 8226
J1	E6	A3	BLANK
J1	E6	A4	BLANK
J1	E5	A5	BLANK
J1	E5	A6	BLANK
J2	E8	A7	INTEL 8226
J2	E8	A8	INTEL 8226
J2	EA	A9	BLANK
J2	EA	A10	BLANK
J2	E9	A11	SOLID
J2	E9	A12	SOLID

Note the INTEL 8226 terminators are factory installed.

TABLE 4.12 80/20-4 MICROPROCESSOR THREE TERMINATORS

DRS TELEMETRY
80/20-4 TERMINATORS

MICROPROCESSOR FOUR
(UP-4)

CONNECTOR	PORT	TERMINATOR	DEVICE
J1	E4	A1	INTEL 8226
J1	E4	A2	INTEL 8226
J1	E6	A3	SN7437
J1	E6	A4	SN7437
J1	E5	A5	902
J1	E5	A6	902
J2	E8	A7	INTEL 8226
J2	E8	A8	INTEL 8226
J2	EA	A9	902
J2	EA	A10	902
J2	E9	A11	901
J2	E9	A12	901

Note the INTEL 8226 terminators are factory installed.
901 is 220/330 ohm pull-up/pull-down terminating pack.
902 is 1K ohm pull-up terminating pack.

TABLE 4.13 80/20-4 MICROPROCESSOR FOUR TERMINATORS

DRS TELEMETRY
80/20-4 TERMINATORS

MICROPROCESSOR FIVE
(UP-5)

CONNECTOR	PORT	TERMINATOR	DEVICE
J1	E4	A1	INTEL 8226
J1	E4	A2	INTEL 8226
J1	E6	A3	902
J1	E6	A4	SN7438
J1	E5	A5	SN7438
J1	E5	A6	SN7438
J2	E8	A7	INTEL 8226
J2	E8	A8	INTEL 8226
J2	EA	A9	SN7408
J2	EA	A10	SN7408
J2	E9	A11	902
J2	E9	A12	902

Note the INTEL 8226 terminators are factory installed.
902 is 1K ohm pull-up terminating pack.

TABLE 4.14 80/20-4 MICROPROCESSOR FIVE TERMINATORS

DRS TELEMETRY
80/20-4 TERMINATORS

MICROPROCESSOR SIX
(UP-6)

CONNECTOR	PORT	TERMINATOR	DEVICE
J1	02	A4	SN7437
J1	02	A5	SN7437
J1	01	A6	SN7437
J1	01	A7	SN7437
J1	03	A8	SN74125 *
J1	03	A9	901
RS232 RECEIVER		A10	BLANK
RS232 DRIVER		A11	BLANK

*SN74125 IS MOUNTED IN SPECIAL CARRIER WITH PINS 3 TO 5 JUMPERED. THE 80/05 BOARD HAS THE RUN BETWEEN A8 PINS 3 TO A8 PIN5 CUT. THE SN74125 HAS PINS 1,2,3,8,9,10,11,12,AND 13 CUTOFF.

Note the 901 is 220/330 ohm pull-up/pull-down terminating pack.

TABLE 4.15 80/05 MICROPROCESSOR SIX TERMINATORS

DRS TELEMETRY
80/20-4 TERMINATORS

MEMORY 116

CONNECTOR	PORT	TERMINATOR	DEVICE
J1	F4	A1	INTEL 8226
J1	F4	A2	INTEL 8226
J1	F6	A3	SN7437
J1	F6	A4	SN7437
J1	F5	A5	902
J1	F5	A6	902
J2	F8	A7	INTEL 8226
J2	F8	A8	INTEL 8226
J2	FA	A9	902
J2	FA	A10	902
J2	F9	A11	902
J2	F9	A12	902

Note the INTEL 8226 terminators are factory installed.
901 is 220/330 ohm pull-up/pull-down terminating pack.
902 is 1K ohm pull-up terminating pack.

TABLE 4.16 116 MEMORY BOARD TERMINATORS

DRS TELEMETRY
80/20-4 WIRE/CABLE

MICROPROCESSOR ONE
(UP-1 CONNECTOR J1)

PORT	BIT	PIN#	WIRE#	PERIPHERAL DEVICE
E4	0	J1-48	47	A0 DAC MUX
E4	1	J1-46	45	A1 DAC MUX
E4	2	J1-44	43	A2 DAC MUX
E4	3	J1-42	41	CARD SELECT STROBE 1 DAC MUX
E4	4	J1-40	39	CARD SELECT STROBE 2 DAC MUX
E4	5	J1-38	37	NOT USED
E4	6	J1-36	35	CLOCK 2 DAC MUX
E4	7	J1-34	33	CHANNEL STROBE DAC MUX
E6	7	J1-32	31	DATA BIT 09 DAC MUX
E6	6	J1-30	29	DATA BIT 10 DAC MUX
E6	5	J1-28	27	DATA BIT 11 DAC MUX
E6	4	J1-26	25	DATA BIT 12 DAC MUX
E6	0	J1-24	23	DATA BIT 16 DAC MUX
E6	1	J1-22	21	DATA BIT 15 DAC MUX
E6	2	J1-20	19	DATA BIT 14 DAC MUX
E6	3	J1-18	17	DATA BIT 13 DAC MUX
E5	0	J1-16	15	DATA BIT 08 DAC MUX
E5	1	J1-14	13	DATA BIT 07 DAC MUX
E5	2	J1-12	11	DATA BIT 06 DAC MUX
E5	3	J1-10	09	DATA BIT 05 DAC MUX
E5	4	J1-08	07	DATA BIT 04 DAC MUX
E5	5	J1-06	05	DATA BIT 03 DAC MUX
E5	6	J1-04	03	DATA BIT 02 DAC MUX
E5	7	J1-02	01	SIGN BIT DAC MUX

DAC MUX is a USGS designed multichannel digital-to-analog system.

Note the odd connector pins are all tied to microprocessor common ground.
All even number wires will connect to the microprocessor common ground.

TABLE 4.17 80/20-4 MICROPROCESSOR ONE WIRE/CABLE ASSIGNMENTS FOR CONNECTOR J1

DRS TELEMETRY
80/20-4 WIRE/CABLE

MICROPROCESSOR ONE
(UP-1 CONNECTOR J2)

PORT	BIT	PIN#	WIRE#	PERIPHERAL DEVICE
E8	0	J2-48	47	DATA0 J5-1 SYSTRON DONNER
E8	1	J2-46	45	DATA1 J5-2 SYSTRON DONNER
E8	2	J2-44	43	DATA2 J5-26 SYSTRON DONNER
E8	3	J2-42	41	DATA3 J5-27 SYSTRON DONNER
E8	4	J2-40	39	DATA4 J5-3 SYSTRON DONNER
E8	5	J2-38	37	DATA5 J5-4 SYSTRON DONNER
E8	6	J2-36	35	DATA6 J5-28 SYSTRON DONNER
E8	7	J2-34	33	DATA7 J5-29 SYSTRON DONNER
EA	7	J2-32	31	NOT USED
EA	6	J2-30	29	NOT USED
EA	5	J2-28	27	BYTE 6 J5-37 SYSTRON DONNER
EA	4	J2-26	25	BYTE 5 J5-12 SYSTRON DONNER
EA	0	J2-24	23	BYTE 1 J5-10 SYSTRON DONNER
EA	1	J2-22	21	BYTE 2 J5-35 SYSTRON DONNER
EA	2	J2-20	19	BYTE 3 J5-11 SYSTRON DONNER
EA	3	J2-18	17	BYTE 4 J5-36 SYSTRON DONNER
E9	0	J2-16	15	50 MSEC. PULSE 20PPS BNC
E9	1	J2-14	13	NOT USED
E9	2	J2-12	11	NOT USED
E9	3	J2-10	09	NOT USED
E9	4	J2-08	07	YEAR1 J5-19 SYSTRON DONNER
E9	5	J2-06	05	YEAR2 J5-20 SYSTRON DONNER
E9	6	J2-04	03	YEAR4 J5-44 SYSTRON DONNER
E9	7	J2-02	01	YEAR8 J5-45 SYSTRON DONNER

Systron Donner is a commercial digital timing system.
CONNECT EVEN NUMBER WIRES TO J5-48,49,50 of the Systron Donner Time Encoder.

Note the odd connector pins are all tied to microprocessor common ground.
All even number wires will connect to the microprocessor common ground.

TABLE 4.18 80/20-4 MICROPROCESSOR ONE WIRE/CABLE ASSIGNMENTS FOR CONNECTOR J2

DRS TELEMETRY
80/20-4 WIRE/CABLE

MICROPROCESSOR THREE
(UP-3 CONNECTOR J2)

PORT	BIT	PIN#	WIRE#	PERIPHERAL DEVICE
E8	0	J2-48	47	UP-4 ADC CONTROL
E8	1	J2-46	45	UP-4 ADC CONTROL
E8	2	J2-44	43	UP-4 ADC CONTROL
E8	3	J2-42	41	UP-4 ADC CONTROL
E8	4	J2-40	39	UP-4 ADC CONTROL
E8	5	J2-38	37	UP-4 ADC CONTROL
E8	6	J2-36	35	UP-4 ADC CONTROL
E8	7	J2-34	33	UP-4 ADC CONTROL
EA	7	J2-32	31	NOT USED
EA	6	J2-30	29	NOT USED
EA	5	J2-28	27	NOT USED
EA	4	J2-26	25	NOT USED
EA	0	J2-24	23	NOT USED
EA	1	J2-22	21	NOT USED
EA	2	J2-20	19	NOT USED
EA	3	J2-18	17	NOT USED
E9	0	J2-16	15	UP-5 CALIBRATOR CONTROL
E9	1	J2-14	13	UP-5 CALIBRATOR CONTROL
E9	2	J2-12	11	UP-5 CALIBRATOR CONTROL
E9	3	J2-10	09	UP-5 CALIBRATOR CONTROL
E9	4	J2-08	07	UP-5 CALIBRATOR CONTROL
E9	5	J2-06	05	UP-5 CALIBRATOR CONTROL
E9	6	J2-04	03	UP-5 CALIBRATOR CONTROL
E9	7	J2-02	01	UP-5 CALIBRATOR CONTROL

ADC system is a commercial ADC unit in a USGS assembly
Calibrator is a USGS designed system.

Note the odd connector pins are all tied to microprocessor common ground.
All even number wires will connect to the microprooessor common ground.

TABLE 4.19 80/20-4 MICROPROCESSOR THREE WIRE/CABLE ASSIGNMENTS FOR CONNECTOR J2

DRS TELEMETRY
80/20-4 WIRE/CABLE

MICROPROCESSOR FOUR
(UP-4 CONNECTOR J1)

PORT	BIT	PIN#	WIRE#	PERIPHERAL DEVICE
E4	0	J1-48	47	2B10 ADC LSBYTE BIT 15
E4	1	J1-46	45	2B9 ADC LSBYTE BIT 14
E4	2	J1-44	43	2B8 ADC LSBYTE BIT 13
E4	3	J1-42	41	2B7 ADC LSBYTE BIT 12
E4	4	J1-40	39	2B27 ADC LSBYTE BIT 11
E4	5	J1-38	37	2B26 ADC LSBYTE BIT 10
E4	6	J1-36	35	2B25 ADC LSBYTE BIT 9
E4	7	J1-34	33	2B24 ADC LSBYTE BIT 8
E6	7	J1-32	31	6B3 CLOCK STROBE
E6	6	J1-30	29	6A12 CHANNEL STROBE
E6	5	J1-28	27	NOT USED
E6	4	J1-26	25	1A6 RA STB ADC CONTROL
E6	0	J1-24	23	1A9 RA1 ADC CONTROL
E6	1	J1-22	21	1B19 RA2 ADC CONTROL
E6	2	J1-20	19	1B10 RA4 ADC CONTROL
E6	3	J1-18	17	1A18 RA8 ADC CONTROL
E5	0	J1-16	15	2A19 ADC MSBYTE BIT 7
E5	1	J1-14	13	2B18 ADC MSBYTE BIT 6
E5	2	J1-12	11	2B15 ADC MSBYTE BIT 5
E5	3	J1-10	09	2A14 ADC MSBYTE BIT 4
E5	4	J1-08	07	2B36 ADC MSBYTE BIT 3
E5	5	J1-06	05	2A35 ADC MSBYTE BIT 2
E5	6	J1-04	03	2B34 ADC MSBYTE BIT 1
E5	7	J1-02	01	2B33 ADC MSBYTE SIGN BIT

DAC MUX is a USGS designed multichannel digital to analog system.

Note the odd connector pins are all tied to microprocessor common ground.
All even number wires will connect to the microprocessor common ground.

TABLE 4.20 80/20-4 MICROPROCESSOR FOUR WIRE/CABLE ASSIGNMENTS FOR CONNECTOR J1

DRS TELEMETRY
80/20-4 WIRE/CABLE

MICROPROCESSOR FOUR
(UP-4 CONNECTOR J2)

PORT	BIT	PIN#	WIRE#	PERIPHERAL DEVICE
E8	0	J2-48	47	UP-3 ADC CODE
E8	1	J2-46	45	UP-3 ADC CODE
E8	2	J2-44	43	UP-3 ADC CODE
E8	3	J2-42	41	UP-3 ADC CODE
E8	4	J2-40	39	UP-3 ADC CODE
E8	5	J2-38	37	UP-3 ADC CODE
E8	6	J2-36	35	UP-3 ADC CODE
E8	7	J2-34	33	UP-3 ADC CODE
EA	7	J2-32	31	UP-5 CALIBRATION STATUS
EA	6	J2-30	29	UP-5 CALIBRATION STATUS
EA	5	J2-28	27	UP-5 CALIBRATION STATUS
EA	4	J2-26	25	UP-5 CALIBRATION STATUS
EA	0	J2-24	23	UP-5 CALIBRATION STATUS
EA	1	J2-22	21	UP-5 CALIBRATION STATUS
EA	2	J2-20	19	UP-5 CALIBRATION STATUS
EA	3	J2-18	17	UP-5 CALIBRATION STATUS
E9	0	J2-16	15	NOT USED
E9	1	J2-14	13	AMP SAT V
E9	2	J2-12	11	AMP SAT N/S
E9	3	J2-10	09	AMP SAT E/W
E9	4	J2-08	07	NOT USED
E9	5	J2-06	05	NOT USED
E9	6	J2-04	03	NOT USED
E9	7	J2-02	01	NOT USED

AMP SAT are amplifier saturation signals from the amplifier system.

Note the odd connector pins are all tied to microprocessor common ground.
All even number wires will connect to the microprocessor common ground.

TABLE 4.21 80/20-4 MICROPROCESSOR FOUR WIRE/CABLE ASSIGNMENTS FOR CONNECTOR J2

DRS TELEMETRY
80/20-4 WIRE/CABLE

MICROPROCESSOR FIVE
(UP-5 CONNECTOR J1)

PORT	BIT	PIN#	WIRE#	PERIPHERAL DEVICE
E4	0	J1-48	47	LP PHOTO-NOT CALIBRATOR
E4	1	J1-46	45	LP-NOT CALIBRATOR
E4	2	J1-44	43	IP-NOT CALIBRATOR
E4	3	J1-42	41	SP-NOT CALIBRATOR
E4	4	J1-40	39	STEP-NOT CALIBRATOR
E4	5	J1-38	37	SINE-NOT CALIBRATOR
E4	6	J1-36	35	FREQ SWEEP-NOT CALIBRATOR
E4	7	J1-34	33	ABORT-NOT CALIBRATOR
E6	7	J1-32	31	SPARE
E6	6	J1-30	29	SRQ CALIBRATOR
E6	5	J1-28	27	NDAC CALIBRATOR
E6	4	J1-26	25	NRFD CALIBRATOR
E6	0	J1-24	23	ATN CALIBRATOR
E6	1	J1-22	21	DAV CALIBRATOR
E6	2	J1-20	19	REN CALIBRATOR
E6	3	J1-18	17	EOI CALIBRATOR
E5	0	J1-16	15	D101 CALIBRATOR
E5	1	J1-14	13	D102 CALIBRATOR
E5	2	J1-12	11	D103 CALIBRATOR
E5	3	J1-10	09	D104 CALIBRATOR
E5	4	J1-08	07	D105 CALIBRATOR
E5	5	J1-06	05	D106 CALIBRATOR
E5	6	J1-04	03	D107 CALIBRATOR
E5	7	J1-02	01	D108 CALIBRATOR

CURRENT CALIBRATOR is a USGS designed
DWWSSN Programmable Current Calibrator

Note the odd connector pins are all tied to microprocessor common ground.
All even number wires will connect to the microprocessor common ground.

TABLE 4.22 80/20-4 MICROPROCESSOR FIVE WIRE/CABLE ASSIGNMENTS FOR CONNECTOR J1

DRS TELEMETRY
80/20-4 WIRE/CABLE

MICROPROCESSOR FIVE
(UP-5 CONNECTOR J2)

PORT	BIT	PIN#	WIRE#	PERIPHERAL DEVICE
E8	0	J2-48	47	L1-NOT CALIBRATOR
E8	1	J2-46	45	L2-NOT CALIBRATOR
E8	2	J2-44	43	L3-NOT CALIBRATOR
E8	3	J2-42	41	P1-NOT CALIBRATOR
E8	4	J2-40	39	P2-NOT CALIBRATOR
E8	5	J2-38	37	P3-NOT CALIBRATOR
E8	6	J2-36	35	P4-NOT CALIBRATOR
E8	7	J2-34	33	P5-NOT CALIBRATOR
EA	7	J2-32	31	UP-5 CALIBRATION STATUS
EA	6	J2-30	29	UP-5 CALIBRATION STATUS
EA	5	J2-28	27	UP-5 CALIBRATION STATUS
EA	4	J2-26	25	UP-5 CALIBRATION STATUS
EA	0	J2-24	23	UP-5 CALIBRATION STATUS
EA	1	J2-22	21	UP-5 CALIBRATION STATUS
EA	2	J2-20	19	UP-5 CALIBRATION STATUS
EA	3	J2-18	17	UP-5 CALIBRATION STATUS
E9	0	J2-16	15	UP-3 CALIBRATOR CONTROL
E9	1	J2-14	13	UP-3 CALIBRATOR CONTROL
E9	2	J2-12	11	UP-3 CALIBRATOR CONTROL
E9	3	J2-10	09	UP-3 CALIBRATOR CONTROL
E9	4	J2-08	07	UP-3 CALIBRATOR CONTROL
E9	5	J2-06	05	UP-3 CALIBRATOR CONTROL
E9	6	J2-04	03	UP-3 CALIBRATOR CONTROL
E9	7	J2-02	01	UP-3 CALIBRATOR CONTROL

Note the odd connector pins are all tied to microprocessor common ground.
All even number wires will connect to the microprocessor common ground.

TABLE 4.23 80/20-4 MICROPROCESSOR FIVE WIRE/CABLE ASSIGNMENTS FOR CONNECTOR J2

DRS TELEMETRY
80/05 WIRE/CABLE

MICROPROCESSOR SIX
(UP-6 CONNECTOR J1)

PORT	BIT	PIN#	WIRE#	PERIPHERAL DEVICE
01	0	J1-48	47	SELECT TAPE TRANSPORT 0
01	1	J1-46	45	SELECT TAPE TRANSPORT 1
01	2	J1-44	43	SELECT DENSITY 0
01	3	J1-42	41	SELECT DENSITY 1
01	4	J1-40	39	PARITY
01	5	J1-38	37	READ
01	6	J1-36	35	WRITE
01	7	J1-34	33	EOF WRITE
		J1-32	31	NOT USED
		J1-30	29	NOT USED
03	5	J1-28	27	NOT USED
03	4	J1-26	25	WRITE CLOCK BUFFER ENABLE
03	0	J1-24	23	NOT USED
03	1	J1-22	21	NOT USED
03	2	J1-20	19	WRITE CLOCK
03	3	J1-18	17	NOT USED
02	0	J1-16	15	BACK SPACE 1 BLOCK
02	1	J1-14	13	BACK SPACE 1 FILE
02	2	J1-12	11	ERASE
02	3	J1-10	09	RESET
02	4	J1-08	07	SEARCH FORWARD 1 BLOCK
02	5	J1-06	05	DEVICE ENABLE
02	6	J1-04	03	OFF LINE COMMAND
02	7	J1-02	01	CONTROL COMMAND

This 80/05 microprocessor controls the magnetic-tape formatter.

Note the odd connector pins are all tied to microprocessor common ground.
All even number wires will connect to the microprooessor common ground.

TABLE 4.24 80/05 MICROPROCESSOR SIX WIRE/CABLE ASSIGNMENTS FOR CONNECTOR J1

DRS TELEMETRY
SBC 116 WIRE/CABLE

MEMORY SBC 116
(116 CONNECTOR J1)

PORT	BIT	PIN#	WIRE#	PERIPHERAL DEVICE
F4	0	J1-48	47	BIT 1 TSWITCH FRONT PANEL
F4	1	J1-46	45	BIT 2 TSWITCH FRONT PANEL
F4	2	J1-44	43	BIT 4 TSWITCH FRONT PANEL
F4	3	J1-42	41	BIT 8 TSWITCH FRONT PANEL
F4	4	J1-40	39	BIT 1 BSWITCH FORNT PANEL
F4	5	J1-38	37	BIT 2 BSWITCH FRONT PANEL
F4	6	J1-36	35	BIT 4 BSWITCH FRONT PANEL
F4	7	J1-34	33	BIT 8 BSWITCH FRONT PANEL
F6	7	J1-32	31	GO/NO LIGHT
F6	6	J1-30	29	GO LIGHT
F6	5	J1-28	27	ALARM LIGHT
F6	4	J1-26	25	ALARM
F6	0	J1-24	23	CAL ACTIVATE SWITCH
F6	1	J1-22	21	ALARM RESET SWITCH
F6	2	J1-20	19	MASTER KEY SWITCH
F6	3	J1-18	17	SPARE
F5	0	J1-16	15	BIT 1 CSWITCH FRONT PANEL
F5	1	J1-14	13	BIT 2 CSWITCH FRONT PANEL
F5	2	J1-12	11	BIT 4 CSWITCH FRONT PANEL
F5	3	J1-10	09	BIT 8 CSWITCH FRONT PANEL
F5	4	J1-08	07	BIT 1 DSWITCH FRONT PANEL
F5	5	J1-06	05	BIT 2 DSWITCH FRONT PANEL
F5	6	J1-04	03	BIT 4 DSWITCH FRONT PANEL
F5	7	J1-02	01	BIT 8 DSWITCH FRONT PANEL

FRONT PANEL is a USGS designed unit.

Note the odd connector pins are all tied to microprocessor common ground.
All even number wires will connect to the microprocessor common ground.

TABLE 4.25 SBC 116 MEMORY WIRE/CABLE ASSIGNMENTS FOR CONNECTOR J1

DRS TELEMETRY
SBC 116 WIRE/CABLE

MEMORY SBC 116
(116 CONNECTOR J2)

PORT	BIT	PIN#	WIRE#	PERIPHERAL DEVICE
F8	0	J2-48	47	BIT 1 FSWITCH FRONT PANEL
F8	1	J2-46	45	BIT 2 FSWITCH FRONT PANEL
F8	2	J2-44	43	BIT 4 FSWITCH FRONT PANEL
F8	3	J2-42	41	BIT 8 FSWITCH FRONT PANEL
F8	4	J2-40	39	BIT 1 SP STEP SWITCH
F8	5	J2-38	37	BIT 2 SP STEP SWITCH
F8	6	J2-36	35	BIT 4 SP STEP SWITCH
F8	7	J2-34	33	BIT 8 SP STEP SWITCH
FA	7	J2-32	31	BIT 8 SP DAILY SWITCH
FA	6	J2-30	29	BIT 4 SP DAILY SWITCH
FA	5	J2-28	27	BIT 2 SP DAILY SWITCH
FA	4	J2-26	25	BIT 1 SP DAILY SWITCH
FA	0	J2-24	23	BIT 1 LP STEP SWITCH
FA	1	J2-22	21	BIT 2 LP STEP SWITCH
FA	2	J2-20	19	BIT 4 LP STEP SWITCH
FA	3	J2-18	17	BIT 8 LP STEP SWITCH
F9	0	J2-16	15	BIT 1 LP DAILY SWITCH
F9	1	J2-14	13	BIT 2 LP DAILY SWITCH
F9	2	J2-12	11	BIT 4 LP DAILY SWITCH
F9	3	J2-10	09	BIT 8 LP DAILY SWITCH
F9	4	J2-08	07	BIT 1 IP PHOTO SWITCH
F9	5	J2-06	05	BIT 2 IP PHOTO SWITCH
F9	6	J2-04	03	BIT 4 IP PHOTO SWITCH
F9	7	J2-02	01	BIT 8 IP PHOTO SWITCH

FRONT PANEL is a USGS designed unit.

Note the odd connector pins are all tied to microprocessor common ground.
All even number wires will connect to the microprocessor common ground.

TABLE 4.26 SBC 116 MEMORY WIRE/CABLE ASSIGNMENTS FOR CONNECTOR J2

DRS TELEMETRY
80/20-4 WIRE/CABLE

MICROPROCESSORS ONE,TWO,THREE, AND FOUR
UP1 AND UP4 ARE DATA TRANSMITTERS
UP2 AND UP3 ARE DATA RECEIVERS
(RS232C CONNECTOR J3)

PORT	PIN#	WIRE#	MOD-PIN#	PERIPHERAL DEVICE
RS232C	J3- 1	2		NOT USED
RS232C	J3- 2	1	1	MODEM PROTECTIVE GROUND, ALL
RS232C	J3- 3	4	15	MODEM XMTR CLOCK, UP1&4
RS232C	J3- 4	3	3	MODEM RECEIVED DATA, UP2&3
RS232C	J3- 5	6		NOT USED
RS323C	J3- 6	5	2	MODEM TRANSMITTER DATA, UP1&4
RS232C	J3- 7	8	17	MODEM RECEIVER CLOCK, UP2&3
RS232C	J3- 8	7	5	MODEM CLEAR TO SEND, UP1&4
RS232C	J3- 9	10		NOT USED
RS232C	J3-10-NC*	9	4	MODEM REQUEST TO SEND, UP1&4*
RS232C	J3-11	12		NOT USED
RS232C	J3-12	11	20	MODEM DATA TERM RDY, UP1&4
RS232C	J3-13	14	6	MODEM DATA SET READY, ALL
RS232C	J3-14	13	7	MODEM SIGNAL GROUND, ALL
RS232C	J3-15	16		NOT USED
RS232C	J3-16	15	8	MODEM DATA CARR DET, UP2&3
RS232C	J3-17	18		NOT USED
RS232C	J3-18	17		NOT USED
RS232C	J3-19	20		NOT USED
RS232C	J3-20	19		NOT USED
RS232C	J3-21	22		NOT USED
RS232C	J3-22	21		NOT USED
RS232C	J3-23	24		NOT USED
RS232C	J3-24	23		NOT USED
RS232C	J3-25	26		NOT USED
RS232C	J3-26	25		NOT USED

*Note Do not connect wire to J3 pin 10. Jumper modem pin 4 to modem pin 9, +12 volts test.

TABLE 4.27 80/20-4 WIRE/CABLE ASSIGNMENTS
MICROPROCESSOR'S ONE, TWO, THREE, AND FOUR
RS232C CONNECTOR J3

DRS TELEMETRY
2400 BAUD MODEMS

UDS-201B

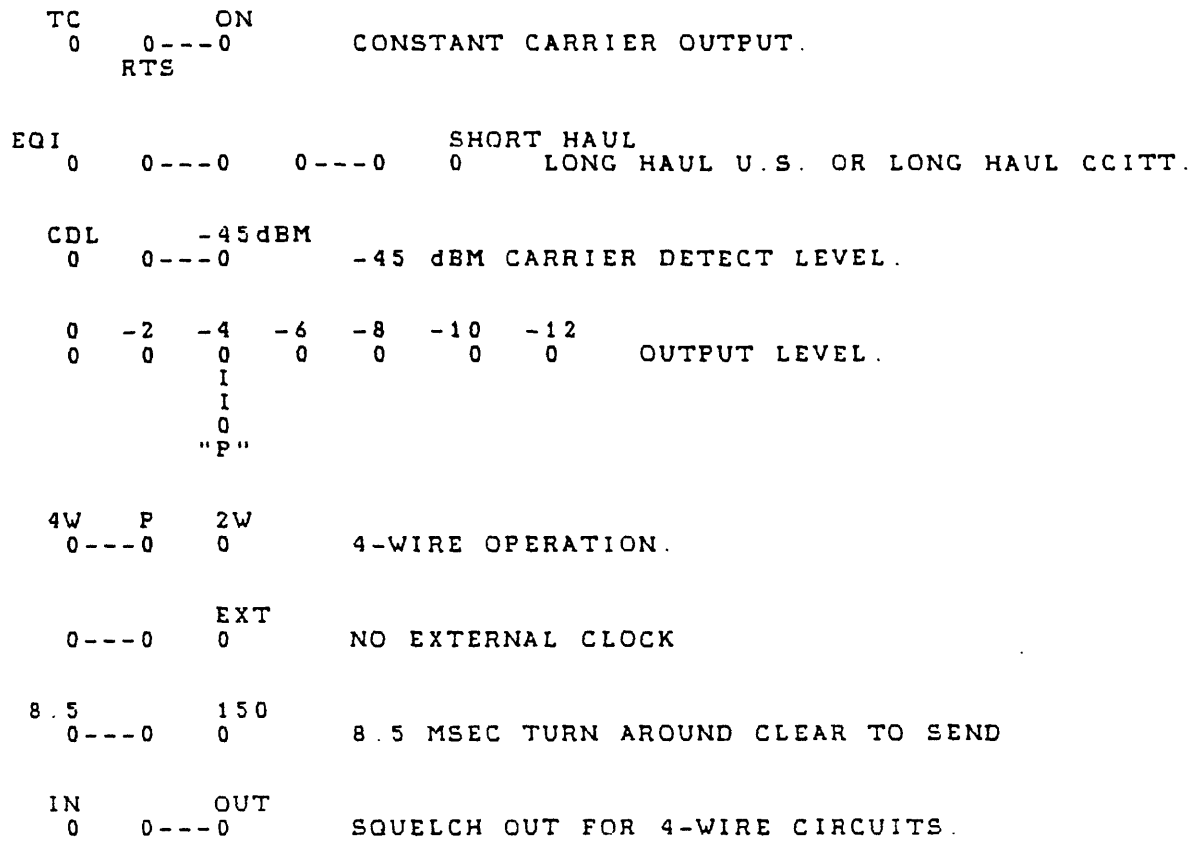
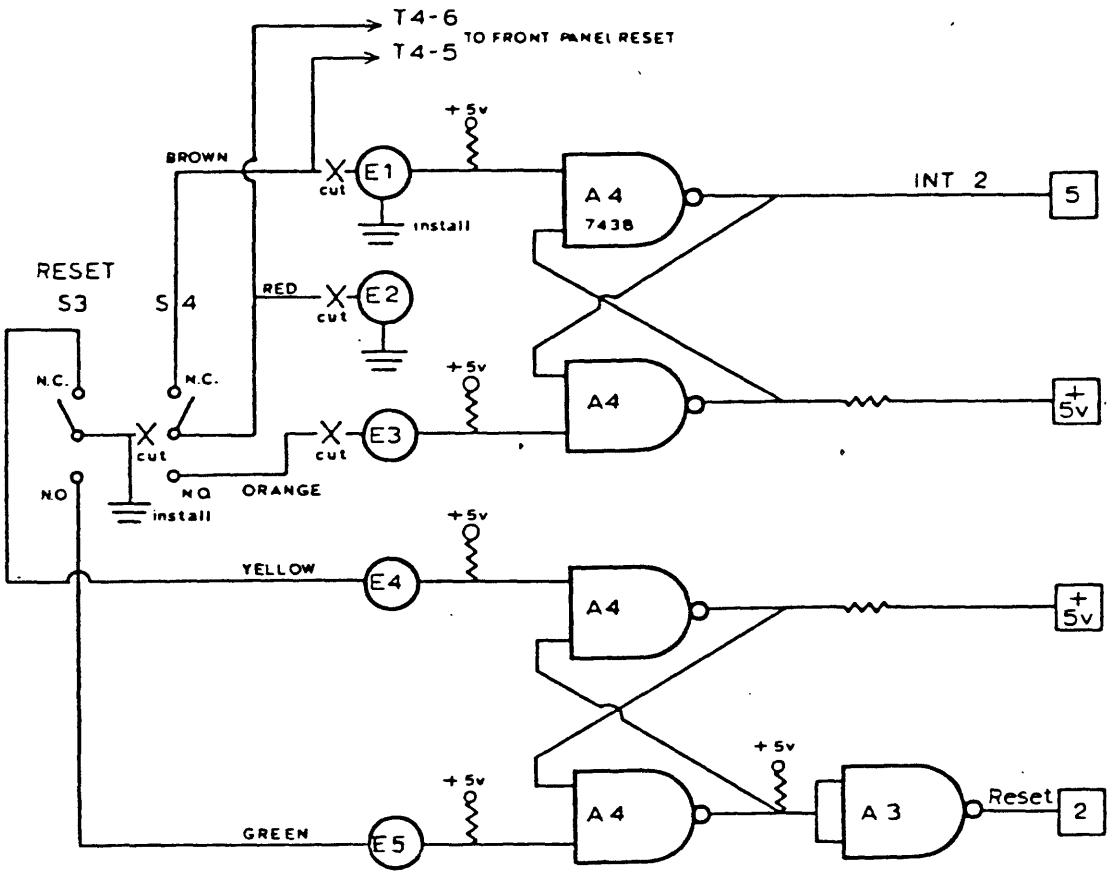


TABLE 4.28 2400 BAUD DIGITAL MODEM
JUMPER/STRAP ASSIGNMENTS



STEPS :

1. Cut brown wire from S4 at E1, connect to T4-5.
2. Cut red wire from S4 at E2, connect to T4-6.
3. Cut orange wire from S4 at E3, insulate cut end.
4. Cut red wire common between S3 and S4
5. Install ground at S3 common.
6 Install ground at E1.

FIGURE 4.1 SBC 655 FRONT PANEL SWITCH MODIFICATION

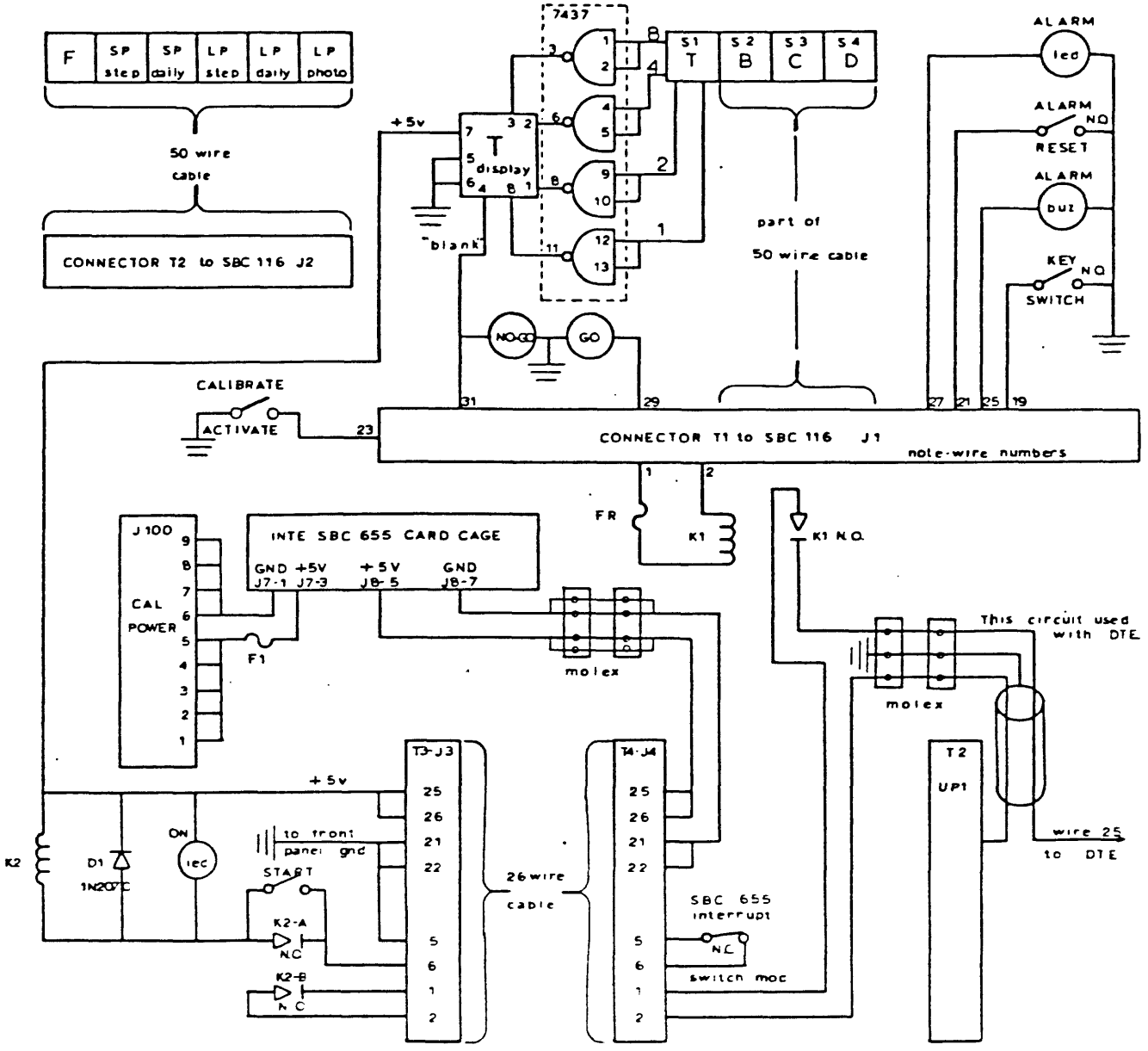


FIGURE 4.2 SBC 655 CHASSIS AND SYSTEM FRONT PANEL SCHEMATIC

5. DWWSSN DRS TELEMETERED SYSTEM INFORMATION

The DWWSSN DRS Telemetry System uses the SBC 116 memory board as the main multi-user random access memory (RAM) storage for temporary storage of information and seismic data. Microprocessor's One, Two, and Six of the central system, write to and read information from this 16-kilobyte RAM. Each microprocessor also has some RAM memory located within its own processor board for sole use. Some discussion as to individual microprocessor RAM locations are given in section 3.

Figure 5.1 presents the major names/labels and memory locations for the SBC 116 memory. These locations or "MAILBOXES" are helpful in determining system operation and status during system checkout or trouble shooting. These "MAILBOX" locations are the primary means of information/data exchange between microprocessors. The "MAILBOX" scheme allows one microprocessor to leave data or command instructions for another microprocessor, without waiting for the other microprocessor to respond. Because of the short 50-millisecond time frame for complete system execution, one microprocessor cannot wait for another to complete a task. Some tasks, such as writing data records to the magnetic tape system requires many 50-millisecond time frames without any interruptions. The "MAILBOX" scheme also eliminates the queuing problems during big events, especially with pre-event data records being written during SP and IP event detection modes of operation.

A microcircuit emulator or tester can be connected to Microprocessor One's 8080 CPU socket and all memory locations for Microprocessor One and the SBC 116 Memory can be reviewed. Table 5.1 and table 5.2 presents these memory locations and

functional names. The entire DWWSSN DRS Telemetry System status and operation can be monitored by the above method. One word of caution is given, using microprocessor emulators or testers will cause millisecond errors in header times. These errors occur because emulators and testers must stop system processing for brief millisecond time periods to do their house-keeping tasks. Normally these time delays are not noticed, but with a system such as the DWWSSN DRS, millisecond errors can be detected. The DWWSSN DRS will operate with these testers and all programmed tasks will be accomplished, but the system will not operate in real time without header time errors. Normally during check-out, magnetic tape recordings are not kept. The final system check-out is preformed with all test equipment disconnected from the system. The final checkout is verified by reading the magnetic tape on the portable DRS Verify-Playback System or suitable computer facility.

Microprocessor emulators and testers can be used with all the system microprocessors for specific microprocessor check-out. The PROGRAM LISTING, for each microprocessor, are given in appendix A. Each microprocessor's EPROM listing are given in appendix B. These EPROM listings provide a means of checking EPROMS for possible malfunctions. A trained microprocessor technician can follow the program listing as machine language code with the EPROM listings. Appendix C provides LINK MAP FILE's for labels and EPROM addresses assigned to each label. Each label in the program listing is assigned an EPROM address and the LINK MAP FILE provides rapid access to program areas of the EPROM listing. The LINK MAP FILE also provides other information, such as the program length.

Appendix D contains the special system operational instructions provided with each DWWSSN DRS System.

DRS TELEMETRY
MEMORY ASSIGNMENTS

SBC 116 RAM MEMORY

RAM LOCATIONS	FUNCTION
C000-C013	HEADER SP RECORD #1, BYTES 1-20
C014-C7CF	DATA SP RECORD #1, BYTES 21-2000
C7D0-C7E3	HEADER SP RECORD #2, BYTES 1-20
C7E4-CF9F	DATA SP RECORD #2, BYTES 21-2000
CFA0-CFB3	HEADER SP RECORD #3, BYTES 1-20
CFB4-D76F	DATA SP RECORD #3, BYTES 21-2000
D770-D783	HEADER IP RECORD #1, BYTES 1-20
D784-DF3F	DATA IP RECORD #1, BYTES 21-2000
DF40-DF53	HEADER IP RECORD #2, BYTES 1-20
DF54-E70F	DATA IP RECORD #2, BYTES 21-2000
E710-E723	HEADER IP RECORD #3, BYTES 1-20
E724-EEDF	DATA IP RECORD #3, BYTES 21-2000
EEE0-EEF3	HEADER LP RECORD #1, BYTES 1-20
EEF4-F6AF	DATA LP RECORD #1, BYTES 21-2000
F6B0-F6C3	HEADER LP RECORD #2, BYTES 1-20
F6C4-FE7F	DATA LP RECORD #2, BYTES 21-2000
FE86-FE87	LP RECORD POINTER DATA
FE88-FE89	SP RECORD POINTER DATA #1
FE8A-FE8B	SP RECORD POINTER DATA #2
FE8C-FE8D	SP RECORD POINTER DATA #3
FE8E-FE8F	IP RECORD POINTER DATA #1
FE90-FE91	IP RECORD POINTER DATA #2
FE92-FE93	IP RECORD POINTER DATA #3
FE94	80/05 FLAG
FE95	REPEAT SWITCH #D
FE96	ALARM RESET
FE98-FE99	80/05 EPROM END
FF00	ADC CODE
FF01	ADC REC 1
FF02	ADC REC 2
FF03	ADC REC 3
FF04	ADC REC 4
FF05	ADC REC 5
FF06	ADC REC 6
FF07	ADC REC 7
FF08	ADC REC 8

Note the RAM locations are given in hexidecimal numbers. The bytes are given as decimal numbers.

TABLE 5.1 SBC 116 RAM MEMORY ASSIGNMENTS

DRS TELEMETRY

MEMORY ASSIGNMENTS

MICROPROCESSOR ONE RAM MEMORY

RAM LOCATIONS	FUNCTION
FLAGS	
3F70	IP ED EVENT-ON FLAG
3728	SP ED EVENT-ON FLAG
3834	SP RECORD FLAG
3838	IP RECORD FLAG
383C	LP RECORD FLAG
3808	SP 2ND EVENT-ON FLAG
3814	IP 2ND EVENT-ON FLAG
3819	IP FLAG
COUNTERS	
3802	IP COUNT
3804	IP COUNT
POINTERS	
3832	SP DATA POINTER
3836	IP DATA POINTER
383A	LP DATA POINTER
DATA/INFORMATION	
3810	DIGISWITCH #1 SP ED PARAMETERS
3811	DIGISWITCH #2 IP ED PARAMETERS
3812	DIGISWITCH #3 SYSTEM CONFIGURATION
3820	TIME BYTE 1
3821	TIME BYTE 2
3822	TIME BYTE 3
3823	TIME BYTE 4
3824	TIME BYTE 5
3825	TIME BYTE 6
3826	SP RECORD BYTE 10 MAILBOX
3827	IP RECORD BYTE 10 MAILBOX
3828	LP RECORD BYTE 10 MAILBOX
3829	CAL CODE RECEIVED
382A	ADC CODE RECEIVED
382B	PAST ADC CODE TRANSMITTED
382C	TEL STATUS
382D	TIMEOUT/RESTART
382E	BYTE 17 SP FORMAT ERROR
382F	BYTE 17 IP FORMAT ERROR
3830	AMP/SAT
3862	NWORD FOR ADC CODE
3863	TWORD
3864	CALWORD
3865	TRANSWORD 1 (ADC CODE)
3866	TRANSWORD 1 (TWORD OR CAL WORD)
3870	ADC CODE
3871	ADC CODE PAST
3900	ADC 1
3901	ADC 2
3902	ADC 3
3903	ADC 4
3904	ADC 5
3905	ADC 6
3906	ADC 7
3907	ADC 8

Note the RAM locations are given in hexidecimal numbers. The bytes are given as decimal numbers.

TABLE 5.2 MICROPROCESSOR ONE RAM MEMORY ASSIGNMENTS

6. DWWSSN DRS TELEMETERED SYSTEM DIGITAL TO ANALOG UNIT

The DWWSSN DRS Telemetry System uses a USGS designed multichannel digital-to-analog multiplexer system for converting the digital data into individual analog seismic channel signals. This unit provides continuous analog channels for each SP, IP, and LP channel being received at the DWWSSN DRS Central System. Individual BNC channel connectors provide output capability for the user to display all channels on analog recorders or to futher transmit the data with analog frequency division multiplexed (FDM) telemetry. The seismic data from Jamestown, California is telemetered from the Berkeley facility to the USGS Menlo Park facility using FDM telemetry.

Figure 6.1 shows the front panel of the Digital to Analog Multiplexer System. The "CHANNEL SELECT SWITCH" allows the operator to monitor any one of the available analog channels on a special BNC connector. One helicorder is provided as part of the central system and uses this switched analog output for analog monitoring of a operator selected seismic channel.

This Digital to Analog Multiplexer has only the "POWER OFF-ON SWITCH" and the "CHANNEL SELECT SWITCH" for operator control. This system is automatic and under control of Microprocessor One.

The system schematic is shown in figure 6.2.

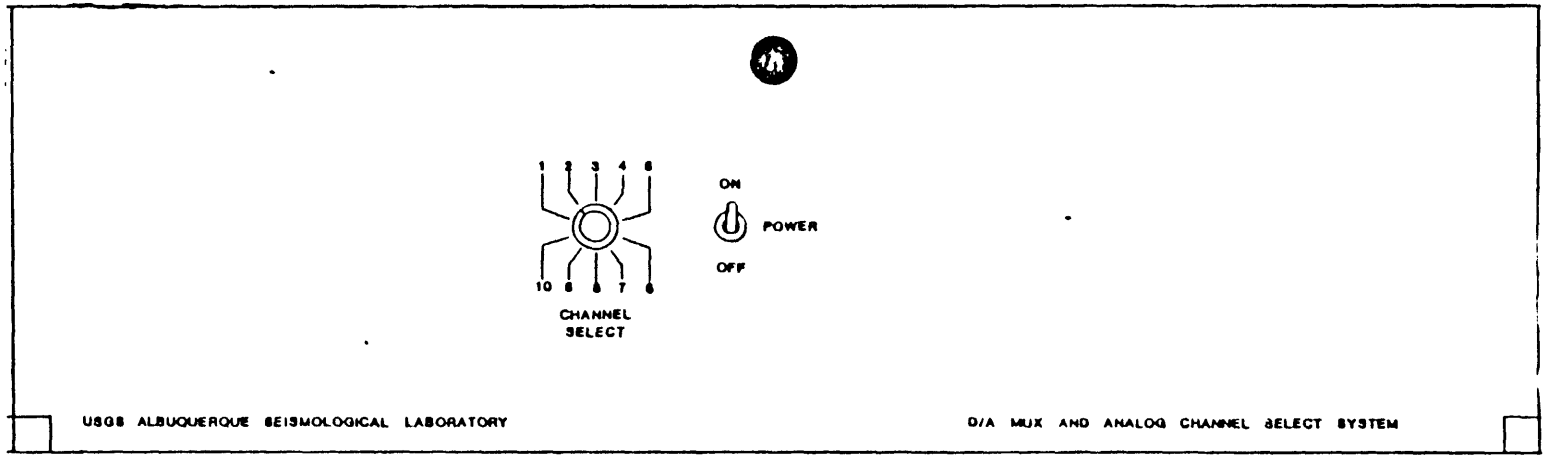


FIGURE 6.1 DIGITAL TO ANALOG MULTIPLEXER UNIT FRONT PANEL

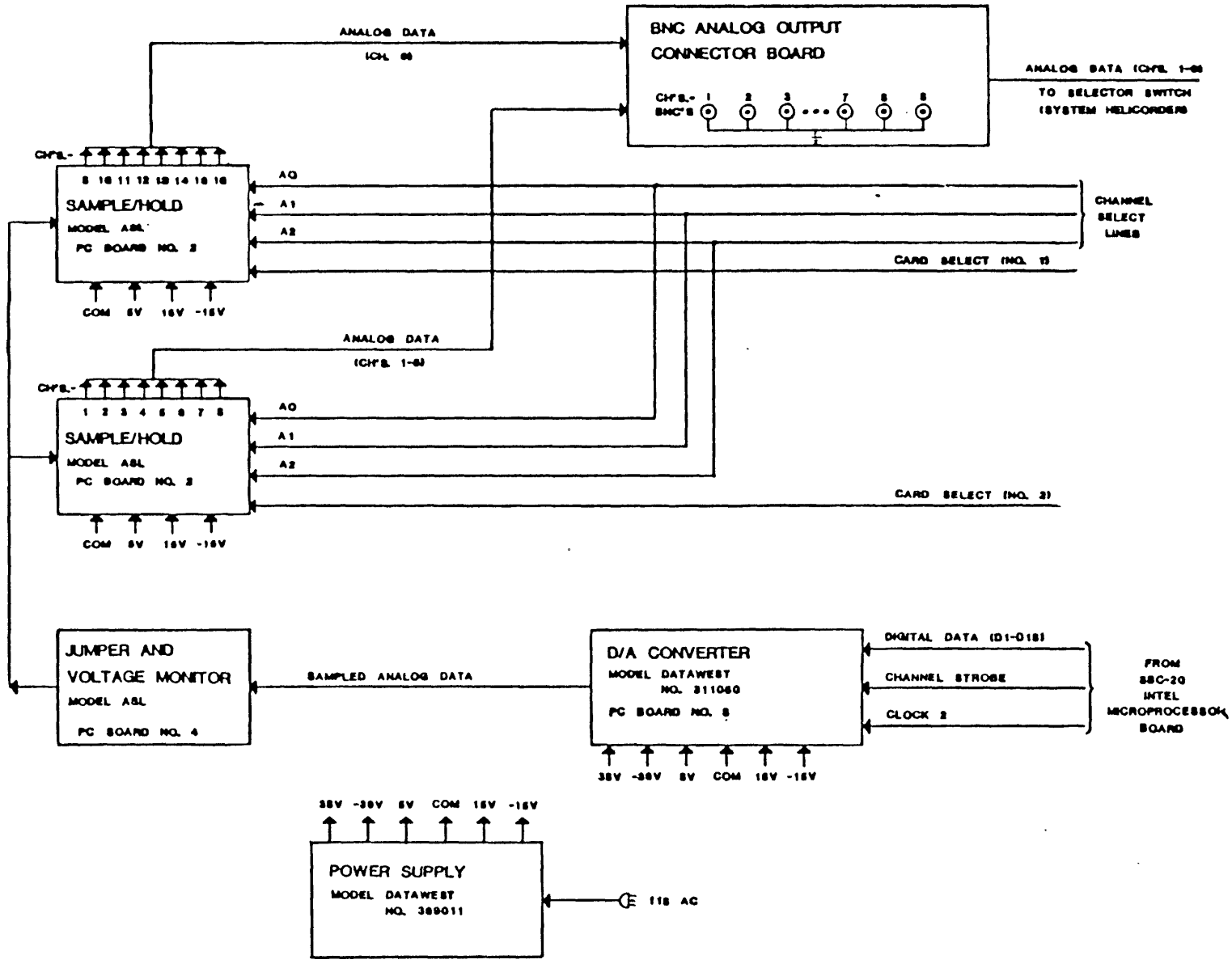


FIGURE 6.2 DIGITAL TO ANALOG MULTIPLEXER SCHEMATIC

APPENDIX A.1

8080 PROGRAM LISTING
MICROPROCESSOR ONE

```
PUBLIC  CLOCK
PUBLIC  RETURN
PUBLIC  EDRET
PUBLIC  RESED
EXTRN   ED
EXTRN   SRSTRT
                                ;JUNE 30, 1982
                                ;THIS IS THE MICROPROCESSOR ONE UP1 PROGRAM FOR
                                ;THE DRS TELEMETRY SYSTEM, ASYNCHRONOUS VERSION.

EVENTA EQU 2000H
EVENTB EQU 200CH

        NOP
        DI
        JMP     SPINIT
        NOP             ;SAVE SPACE FOR HARD CALL.
        NOP             ;SAVE SPACE FOR HARD CALL.
EDRET:  JMP     EVNTR   ;THIS IS A SPECIAL CALL RETURN ADDRESS FOR
        NOP             ;LIBRARY PROGRAM (PROM LOCATED ON 116 BOARD)
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP             ;THIS AREA RESERVED FOR VECTORED INTERRUPTS.
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
```

```
        JMP     CLOCK   ;THIS WILL KEEP THE SYSTEM RUNNING.
SPINIT: LXI     SP,39E0H;SET STACK POINTER 39E0.
        LXI     H,2FFFH ;ZERO 80/20 RAM.
ZERO:   INX     H
        MVI     A,00H
        MOV     M,A
        MOV     A,H
        CPI     3FH
        JNZ     ZERO
        MOV     A,L
        CPI     0FFH
        JNZ     ZERO
        LXI     H,0BFFFH;ZERO 116 MEMORY.
ZER1:   INX     H
        MVI     A,00H
        MOV     M,A
        MOV     A,H
        CPI     0FFH
        JNZ     ZER1
        MOV     A,L
        CPI     0FFH
        JNZ     ZER1
INIT:   MVI     A,80H   ;CONFIGURES DAMUX PORTS , MODE 0.
        OUT     0E7H    ;E4=OUTPUT, E5=OUTPUT, E6=OUTPUT.
        MVI     A,92H   ;CONFIGURES DTE PORTS.
        OUT     0EBH    ;E8=OUTPUT, E9=INPUT,EA=OUTPUT.
        MVI     A,07H   ;INITIALIZE PORT E4 (DAMUX).
        OUT     0E4H
        MVI     A,93H   ;CONFIGURES SWITCH PORTS (116) MODE 0.
        OUT     0F7H    ;F4=INPUT, F5=INPUT, F6 LO=INPUT, F6 HI=OUTPUT.
        MVI     A,9BH   ;CONFIGURES SWITCH PORTS (116) MODE 0.
        OUT     0FBH    ;F8, F9, FA=INPUT.
        MVI     A,0FFH  ;SET DTE DATA STROBE LINE TO ZERO.
        OUT     0EAH
        MVI     A,00H   ;SET ADC CODE PAST = 0.
        STA     3871H
        STA     38FDH   ;SET ADC ERROR = 0.
        STA     38FEH
        STA     0FE94H  ;SET 80/05 FLAG = 0.
        MVI     A,01H
        STA     3862H   ;SET SEQUENCE NUMBER N = 01.
        LXI     H,0F6B0H;SET LP POINTER TO SECOND LP RECORD.
        SHLD    383AH
        LXI     H,0C7D0H;SET SP POINTER TO SECOND SP RECORD.
        SHLD    3832H
        LXI     H,0DF40H;SET IP POINTER TO SECOND IP RECORD.
        SHLD    3836H
WAITST: IN      0F6H    ;WAIT HERE FOR KEY SWITCH TO BR CLOSED.
        ANI     0FH
        CPI     0BH
        JNZ     WAITST
        JMP     L0EDC
RETURN: MVI     A,93H   ;INSURES CONFIGURATION OF PORT F6.
```

```
        OUT     0F7H
        IN      0F6H    ;READ CAL ACTIVATE SWITCH.
        ANI     0FH
        CPI     0EH
        JNZ     RESCAL
        CALL    CALDE
        JMP     TELST
RESCAL: MVI     A,00H   ;RESET CALDE MEMORY TO ZERO.
        STA     3864H
TELST:  IN      0F4H    ;READ T SWITCH
        ANI     0FH     ;MASK T SWITCH DATA.
        STA     3863H   ;STORE T WORD FOR TRANSMISSION.
        LXI     H,382CH ;COMPARE T WORD RECIVED WITH T WORD?
        SUB     M
        JNZ     NOGO
GO:     LDA     0FE96H  ;T COMPARE GOOD, TEST FOR ALARM.
        ANA     A
        JZ      ONAG
        MVI     A,0B0H  ;OUTPUT NO-ALARM AND GO ENABLE.
        OUT     0F6H
        JMP     OFLAG
ONAG:   MVI     A,80H   ;OUTPUT ALARM AND GO ENABLE.
        OUT     0F6H
        JMP     OFLAG
NOGO:   LDA     0FE96H  ;T COMPARE NO-GOOD, TEST FOR ALARM.
        ANA     A
        JNZ     ONANG
        MVI     A,40H   ;OUTPUT ALARM AND NO-GO ENABLE.
        OUT     0F6H
        JMP     OFLAG
ONANG:  MVI     A,70H   ;OUTPUT NO-ALARM AND NO-GO ENABLE.
        OUT     0F6H
OFLAG:  MVI     A,0FFH  ;OUTPUT 80/05 FLAG.
        STA     0FE94H
KEYSC:  IN      0F6H    ;IS KEY SWITCH CLOSED?
        ANI     0FH
        CPI     0BH
        JNZ     CLOCK
LOEDC:  IN      0F4H    ;****THIS ARE RESERVED FOR ED CONSTANTS
        RAR
        RAR
        RAR
        RAR
        ANI     0FH
        STA     3810H   ;READ AND STORE "B" SWITCH, SP EVENT DETECT PARAM.
        IN      0F5H
        CMA
        MOV     B,A
        ANI     0FH
        STA     3811H   ;READ AND STORE "C" SWITCH, IP EVENT DETECT PARAM.
        MOV     A,B
        RAR
        RAR
```

```
        RAR
        RAR
        ANI     0FH
        STA     3812H   ;READ AND STORE "D" SWITCH, SYSTEM CONFIGURATION.
        MVI     A,00H
        STA     3814H   ;SET IP 2ND EVENT FLAG = 0.
        STA     3870H   ;SET IP EVENT FLAG = 0.
        STA     3803H   ;SET SP 2ND EVENT FLAG = 0.
        STA     3F28H   ;SET SP EVENT FLAG = 0.
        STA     3801    ;SET SP' EVENT DETECT FLAG = 0.
        STA     3834H   ;SET SP RECORD FLAG = 0.
        STA     3838H   ;SET IP RECORD FLAG = 0.
        MVI     A,0FFH
        STA     3806H   ;SET FIRST TIME EVENT DETECT = FF.
        LXI     H,3A00H ;SET SP AND IP EVENT DET.  RAM AREA = 00'S.
        LXI     D,0000H ;SP AREA IS 3A00 TO 3C2F.
RIAGA:  MOV     M,D     ;IP AREA IS 3C40 TO 3EFF.
        INX     H
        MVI     A,3FH   ;IS END = 3F00?
        CMP     H
        JNZ     RIAGA
        LXI     H,3F70H ;IP RAM MEMORY ZERO.
        LXI     D,0000H
IPAGA:  MOV     M,D
        INX     H
        MVI     A,9FH     ;IS END = 379F?
        CMP     L
        JNZ     IPAGA
        MVI     A,80H   ;THIS IS SOFTWARE RESET FOR SERIAL I/O
        OUT     0EDH    ;AS PER JOHN DIZEL.
        MVI     A,00H
        OUT     0EDH
        MVI     A,40H
        OUT     0EDH
        JMP     SRSTRT
RESED:  JMP     EVENTB  ;JUMP TO SP ED INIT AND RETURN TO NEXT LINE "EVNTR
EVNTR:  NOP
CLOCK:  IN      0E9H    ;WAIT FOR THE 50 MSEC CLOCK PULSE.
        ANI     01H
        JZ      CLOCK
DEBNC:  IN      0E9H    ;THIS IS FOR DEBOUNCE.
        ANI     01H
        JZ      DEBNC
        IN      0E9H
        ANI     01H
        JZ      DEBNC
SPTC:   LHLD    3832H   ;CHECK SP POINTER TO SEE IF END OF RECORD.
        MOV     A,H
        CPI     0D7H    ;END OF RECORD #3 ? IF NOT CHECK RECORD #1.
        JNZ     SPR1CH
        MOV     A,L     ;IS LSBYTE = END OF RECORD #3 ?
        CPI     70H     ;(D76F + 1) OR GREATER.
        JC      NUMB
```

```
        LXI     H,0D770H;RESET SP RECORD POINTER TO END + 1 OF SP
        SHLD    3832H   ;RECORD #3.
        CALL    SPTIME
        JMP     NUMB
SPR1CH: LHLD    3832H   ;END OF RECORD #1 ?, IF NOT CHECK RECORD #2.
        MOV     A,H
        CPI     0C7H    ;C7CFH + 1 = C7D0H
        JNZ     SPR2CH  ;(C7CF)
        MOV     A,L
        CPI     0D0H
        JNZ     NUMB
        CALL    SPTIME
        JMP     NUMB
SPR2CH: LHLD    3832H   ;END OF RECORD #2?   (CF9F)
        CPI     0CFH
        JNZ     NUMB
        MOV     A,L     ;CF9FH + 1 = CFA0H
        CPI     0A0H
        JNZ     NUMB
        CALL    SPTIME
NUMB:   LDA     3862H   ;GET "N" FOR SEQUENCE NUMBER.
        CPI     01D
        JZ      SEN10
        CPI     02D
        JZ      SEN11
        CPI     03D
        JZ      SEN12
        CPI     04D
        JZ      SEN11
        CPI     05D
        JZ      SEN13
        CPI     06D
        JZ      SEN11
        CPI     07D
        JZ      SEN12
        CPI     08D
        JZ      SEN11
        CPI     09D
        JZ      SEN13
        CPI     10D
        JZ      SEN11
        CPI     11D
        JZ      SEN12
        CPI     12D
        JZ      SEN11
        CPI     13D
        JZ      SEN13
        CPI     14D
        JZ      SEN11
        CPI     15D
        JZ      SEN12
        CPI     16D
        JZ      SEN11
```

```
        CPI     17D
        JZ      SEN13
        CPI     18D
        JZ      SEN11
        CPI     19D
        JZ      SEN12
        MVI     A,00H   ;SET "N" - 00.
        STA     3862H
        JMP     SEN11
SEN13:  MVI     A,13H   ;SET ADC CODE IN TRANSWORD 1 SLOT.
        STA     3865H   ;SP AND TEL STAT ADC CODE.
        LDA     3863H   ;SET TWORD IN TRANSWORD 2 SLOT.
        STA     3866H
        JMP     TRANS
SEN12:  MVI     A,12H   ;SET ADC CODE IN TRANSWORD 1 SLOT.
        STA     3865H   ;SP AND CAL/AMP ADC CODE.
        LDA     3864H   ;SET CAL WORD IN TRANSWORD 2 SLOT.
        STA     3866H
        JMP     TRANS
SEN11:  LHLD    3836H   ;LOAD IP POINTER AND CHECK IF END  OF RECORD #3+1
        MOV     A,H     ;(EEDF + 1)
        CPI     0EEH
        JNZ     IPR1CH
        MOV     A,L
        CPI     0E0H    ;THIS INSURES IP RECORD CANNOT EXCEED LIMITS
        JC      SEND11  ;OF IP RECORD #3 (EEDF +1) OR GREATER.
        LXI     H,0EEE0H;RESET IP POINTER TO END + 1 OF RECORD #3.
        SHLD    3836H
        CALL    IPTIME
        JMP     SEND11
IPR1CH: LHLD    3836H   ;IS IP RECORD AT THE END OF RECORD #1 (DF3F + 1)
        MOV     A,H
        CPI     0DFH
        JNZ     IPR2CH
        MOV     A,L
        CPI     40H
        JNZ     SEND11
        CALL    IPTIME
        JMP     SEND11
IPR2CH: LHLD    3836H   ;IS IP RECORD POINTER AT THE END OF RECORD #2+1
        MOV     A,H     ;(E70F + 1)
        CPI     0E7H
        JNZ     SEND11
        MOV     A,L
        CPI     10H
        JNZ     SEND11
        CALL    IPTIME
SEND11: MVI     A,11H   ;SET ADC CODE IN TRANSWORD 1 SLOT.
        STA     3865H   ;SP AND IP ADC CODE.
        MVI     A,00H   ;SET TRANSWORD 2 = 00.
        STA     3866H
        JMP     TRANS
SEN10:  LHLD    383AH   ;LOAD LP POINTER AND CHECK IF END OF RECORD  #2+1
```

```
        MOV     A,H         ;(FE7F + 1)
        CPI     0FEH
        JNZ     LPR1CH
        MOV     A,L
        CPI     80H
        JC      SEND10
        CALL    LPTIM1
        JMP     SEND10
LPR1CH: MOV     A,H
        CPI     0F6H        ;IS LP POINTER EQUAL TO END OF RECORD #1+1
        JNZ     SEND10      ;(F6AF + 1)
        MOV     A,L
        CPI     0B0H
        JNZ     SEND10
        CALL    LPTIM2
SEND10: MVI     A,10H       ;SET ADC CODE IN TRANSWORD 1 SLOT.
        STA     3865H       ;SP AND LP ADC CODE.
        MVI     A,00H       ;SET TRANSWORD 2 = 00.
        STA     3866H
TRANS:  MVI     A,00H       ;THIS IS SYSTEM SOFTWARE RESET
        OUT     0EDH        ;AS PER INTEL BOOK.
        OUT     0EDH
        OUT     0EDH
        MVI     A,40H
        OUT     0EDH
        MVI     A,1CH       ;SET TRANSMIT MODE INSTRUCTION,2 SYNC & PARITY.
        OUT     0EDH
        MVI     A,0AAH      ;OUTPUT SYNC WORD "AA"
        OUT     0EDH
        MVI     A,0AAH      ;OUTPUT SYNC WORD "AA"
        OUT     0EDH
        MVI     A,33H       ;SET OUTPUT COMMAND WORD.
        OUT     0EDH
TXRE0:  IN      0EDH
        ANI     01H
        JZ      TXRE0
        MVI     A,0AAH      ;OUTPUT SYNC WORD ONE.
        OUT     0ECH
TXRE1:  IN      0EDH
        ANI     01H
        JZ      TXRE1
        MVI     A,0AAH      ;OUTPUT SYNC WORD TWO.
        OUT     0ECH
TXREA:  IN      0EDH        ;IS TX READY FROM STATUS
        ANI     01H
        JZ      TXREA
        LDA     3865H       ;OUTPUT TRANSWORD 1.  (ADC CODE).
        OUT     0ECH
TXREB:  IN      0EDH
        ANI     01H
        JZ      TXREB
        LDA     3866H       ;OUTPUT TRANSWORD 2.   (EITHER CAL, TELSTAT, OR 0).
        OUT     0ECH
```

```
TXREC:  IN      0EDH    ;OUTPUT TRANSWORD 3.  (DELAY DUMMY WORD = 3.75 MS).
        ANI     01H
        JZ      TXREC
        MVI     A,00H
        OUT     0ECH
TXRED:  IN      0EDH    ;OUTPUT TRANSWORD 4.  (DELAY DUMMY WORD = 3.75 MS).
        ANI     01H
        JZ      TXRED
        MVI     A,0FFH
        OUT     0ECH
ENDIT:  IN      0EDH    ;WAIT FOR LAST DATA BYTE TO BE TRANSMITTED.
        ANI     01H
        JZ      ENDIT
        MVI     A,00H   ;INSERT DUMMY WORD FOR SERIAL I/O.
        OUT     0ECH
ENDX:   IN      0EDH    ;WAIT FOR END.
        ANI     01H
        JZ      ENDX
        MVI     A,40H   ;RESET SERIAL I/O.
        OUT     0EDH
        LDA     3862H   ;INCREMENT "N".
        INR     A
        STA     3862H
DATMO:  LXI     H,0FF00H;GET TEMP ADC DATA FROM 116 AND STORE IN UP1.
        MOV     A,M
        STA     38FFH
        STA     3870H   ;ALSO STORE REC ADC CODE IN MAILBOX.
        INX     H
        MOV     A,M
        STA     3900H
        INX     H
        MOV     A,M
        STA     3901H
        INX     H
        MOV     A,M
        STA     3902H
        INX     H
        MOV     A,M
        STA     3903H
        INX     H
        MOV     A,M
        STA     3904H
        INX     H
        MOV     A,M
        STA     3905H
        INX     H
        MOV     A,M
        STA     3906H
        INX     H
        MOV     A,M
        STA     3907H
OUTDA:  LDA     38FFH   ;LOAD ADC CODE RECEIVED.  DISPLAY AS PER THIS CODE
        CPI     10H
```

```
        JZ      DISA    ;CODE WAS 10.
        CPI     11H
        JZ      DISB    ;CODE WAS 11.
        CPI     12H
        JZ      DISC    ;CODE WAS 12.
        CPI     13H
        JZ      DISD    ;CODE WAS 13.
        LDA     382AH   ;"ERROR" INCREMENT ADC CODE ERROR TYPE 1,
        INR     A       ;BYTE 15 OF RECORDS.
        STA     382AH
        JMP     CODCK
DISA:   CALL    SPDIS   ;DISPLAY SP DATA AND LP DATA.
        CALL    LPDIS
        JMP     CODCK
DISB:   CALL    SPDIS   ;DISPLAY SP DATA AND IP DATA.
        CALL    IPDIS
        JMP     CODCK
DISC:   CALL    SPDIS   ;DISPLAY SP DATA AND PUT CAL/AMP STATUS IN HEADERS
        LDA     3902H   ;AMP LEVEL FOR NO-SAT IS HIGH = 1.
        CMA             ;AMPSAT RECORDED IN SYSTEM NO-SAT = LOW =0.
        STA     3830H   ;AMP/SAT STATUS MAILBOX.
        LDA     3903H
        STA     3829H   ;STORE CALCODE STATUS AT BYTE 14 MAILBOX.
        JMP     CODCK
DISD:   CALL    SPDIS   ;DISPLAY SP DATA AND CHECK TELEMETRY STATUS.
        LDA     3902H   ;STORE TEL STATUS.
        STA     382CH
CODCK:  LXI     H,3870H ;IS REC ADC CODE = ADC CODE PAST?
        LDA     3871H   ;ADC CODE PAST = 3871.
        SUB     M
        JZ      STODA
        LDA     382BH   ;INCREMENT ADC CODE ERROR TYPE 2,
        INR     A       ;BYTE 16 OF RECORDS.
        STA     382BH
STODA:  LDA     3871H   ;IS ADC PAST CODE = 10?
        CPI     10H
        JNZ     CO11
        CALL    LPSTO   ;CALL LP DATA STORAGE AND FORMAT SR.
        JMP     CSPS
CO11:   LDA     3871H   ;IS ADC PAST CODE = 11?
        CPI     11H
        JNZ     CSPS
        CALL    IPSTO   ;CALL IP DATA STORAGE AND FORMAT SR.
CSPS:   CALL    SPSTO   ;CALL SP DATA STORAGE AND FORMAT SR.
        LDA     3865H   ;MOVE ADC CODE TO ADC CODE PAST.
        STA     3871H
POITES: LDA     383BH   ;LOAD LP POINTER MSBYTE.
        CPI     0FEH    ;TEST FOR POINTER BEYOND FE80 ADDRESS.
        JNZ     CALCON
        LDA     383AH   ;LOAD LP POINTER LSBYTE.
        CPI     80H
        JC      CALCON
        LXI     H,0FE80H;THIS INSURES LP POINTER DOES NOT GET MUCH
```

```
        SHLD    393AH   ;END OF LP DATA STORE AREA.
CALCON: JMP     ED      ;GO TO SWITCH CONFIGURATION PORTION.
SPDIS:  LDA     3900H   ;DISPLAY SP DATA (THIS VERSION ONLY SPV).
        RAL             ;LEAVE SIGN BIT SAME COMP DATA.
        CMA
        RAR
        OUT     0E5H    ;LOAD MSBYTE THEN LSBYTE TO DA.
        LDA     3901H
        CMA
        OUT     0E6H
        MVI     A,87H   ;STROBE DATA INTO DA.
        OUT     0E4H
        MVI     A,47H
        OUT     0E4H
        MVI     A,07H   ;SELECT CHANNEL NUMBER.
        OUT     0E4H
        MVI     A,0FH   ;SELECT CARD NUMBER.
        OUT     0E4H
        MVI     A,07H   ;INITIALIZE PORT E4.
        RET
IPDIS:  LDA     3902H   ;IP DISPLAY
        RAL             ;LEAVE SIGN BIT SAME COMP.  DATA.
        CMA
        RAR
        OUT     0E5H    ;OUTPUT MS BYTE FIRST THEN LSBYTE TO DA.
        LDA     3903H   ;THIS IS FIRST CHANNEL.
        CMA
        OUT     0E6H
        MVI     A,87H   ;STROBE DATA INTO DA.
        OUT     0E4H
        MVI     A,47H
        OUT     0E4H
        MVI     A,04H   ;SELECT CHANNEL.
        OUT     0E4H
        MVI     A,0CH   ;SELECT CARD.
        OUT     0E4H
        LDA     3904H   ;THIS IS SECOND CHANNEL.
        RAL             ;LEAVE SIGN BIT SAME COMP.  DATA .
        CMA
        RAR
        OUT     0E5H
        LDA     3905H
        CMA
        OUT     0E6H
        MVI     A,87H   ;STROBE DATA INTO DA.
        OUT     0E4H
        MVI     A,47H
        OUT     0E4H
        MVI     A,03H   ;SELECT CHANNEL.
        OUT     0E4H
        MVI     A,0BH   ;SELECT CARD.
        OUT     0E4H
        LDA     3906H   ;THIS IS THIRD CHANNEL.
```

```
        RAL             ;LEAVE SIGN BIT SAME COMP.  DATA.
        CMA
        RAR
        OUT     0E5H
        LDA     3907H
        CMA
        OUT     0E6H
        MVI     A,87H   ;STROBE DATA INTO DA.
        OUT     0E4H
        MVI     A,47H
        OUT     0E4H
        MVI     A,02H   ;SELECT CHANNEL.
        OUT     0E4H
        MVI     A,1AH   ;SELECT CARD.
        OUT     0E4H
        MVI     A,07H   ;INITIALIZE PORT E4.
        OUT     0E4H
        RET
LPDIS:  LDA     3902H   ;LP DISPLAY
        RAL             ;LEAVE SIGN BIT SAME COMP.  DATA.
        CMA
        RAR
        OUT     0E5H    ;OUTPUT MS BYTE FIRST THEN LSBYTE TO DA.
        LDA     3903H   ;THIS IS FIRST CHANNEL.
        CMA
        OUT     0E6H
        MVI     A,87H   ;STROBE DATA INTO DA.
        OUT     0E4H
        MVI     A,47H
        OUT     0E4H
        MVI     A,01H   ;SELECT CHANNEL.
        OUT     0E4H
        MVI     A,09H   ;SELECT CARD.
        OUT     0E4H
        LDA     3904H   ;THIS IS SECOND CHANNEL.
        RAL             ;LEAVE SIGN BIT SAME COMP.  DATA.
        CMA
        RAR
        OUT     0E5H
        LDA     3905H
        CMA
        OUT     0E6H
        MVI     A,87H   ;STROBE DATA INTO DA.
        OUT     0E4H
        MVI     A,47H
        OUT     0E4H
        MVI     A,00H   ;SELECT CHANNEL.
        OUT     0E4H
        MVI     A,08H   ;SELECT CARD.
        OUT     0E4H
        LDA     3906H   ;THIS IS THIRD CHANNEL.
        RAL             ;LEAVE SIGN BIT SAME COMP.  DATA.
        CMA
```

```
        RAR
        OUT     0E5H
        LDA     3907H
        CMA
        OUT     0E6H
        MVI     A,87H   ;STROBE DATA INTO DA.
        OUT     0E4H
        MVI     A,47H
        OUT     0E4H
        MVI     A,07H   ;SELECT CHANNEL.
        OUT     0E4H
        MVI     A,17H   ;SELECT CARD.
        OUT     0E4H
        MVI     A,07H   ;INITIALIZE PORT E4.
        OUT     0E4H
        RET
SPSTO:  LHLD    3832H   ;SET REG H,L WITH SP DATA POINTER.
        LDA     3900H   ;GET SP MS BYTE AND STORE.
        MOV     M,A
        INX     H       ;ADVANCE SP POINTER
        LDA     3901H   ;GET SP LSBYTE AND STORE.
        MOV     M,A
        INX     H       ;ADVANCE SP POINTER AND RESTORE TO 3832.
        SHLD    3832H
        RET
IPSTO:  LHLD    3836H   ;SET REG H,L WITH IP DATA POINTER.
        LDA     3902H   ;GET IP #1 MS BYTE AND STORE
        MOV     M,A
        INX     H       ;ADVANCE IP POINTER.
        LDA     3903H   ;GET IP #1 LS BYTE AND STORE.
        MOV     M,A
        INX     H
        LDA     3904H   ;GET IP #2 AND STORE.
        MOV     M,A
        INX     H
        LDA     3905H
        MOV     M,A
        INX     H
        LDA     3906H   ;GET IP #3 AND STORE.
        MOV     M,A
        INX     H
        LDA     3907H
        MOV     M,A
        INX     H       ;ADVANCE IP POINTER AND RESTORE TO 3836.
        SHLD    3836H
        RET
LPSTO:  LHLD    383AH   ;SET REG H,L WITH IP POINTER.
        LDA     3902H   ;GET LP #1 DATA AND STORE.
        MOV     M,A
        INX     H
        LDA     3903H
        MOV     M,A
        INX     H
```

```
        LDA     3904H   ;GET LP #2 AND STORE.
        MOV     M,A
        INX     H
        LDA     3905H
        MOV     M,A
        INX     H
        LDA     3906H   ;GET LP #3 AND STORE.
        MOV     M,A
        INX     H
        LDA     3907H
        MOV     M,A
        INX     H       ;ADVANCE LP POINTER AND RESTORE TO 383A.
        SHLD    383AH
        RET
                        ;THIS IS THE CALIBRATION DECODE PORTION OF THE
                        ;DRS TELEMETRY PROGRAM, UP1.
CALDE:  IN      0F8H    ;READ CALIBRATION FUNCTION SWITCH.
        ANI     0FH     ;DATA LOWER PART OF PORT.
        MOV     B,A
FSO:    MOV     A,B
        CPI     00H     ;IS F SWITCH = 0?
        JZ      ABORT
        CPI     01H     ;IS F SWITCH = 1?
        JZ      LPSTP
        CPI     02H     ;IS F SWITCH = 2?
        JZ      SPSTP
        CPI     03H     ;IS F SWITCH = 3?
        JZ      LPSIN
        CPI     04H     ;IS F SWITCH = 4?
        JZ      SPSIN
        CPI     05H     ;IS F SWITCH = 5?
        JZ      LPRES
        CPI     06H     ;IS F SWITCH = 6?
        JZ      SPRES
        CPI     07H     ;IS F SWITCH = 7?
        JZ      IPRES
        CPI     08H     ;IS F SWITCH = 8?
        JZ      IPPHO
        CPI     09H     ;IS F SWITCH = 9?
        JZ      ABORT
        CPI     0AH     ;IS F SWITCH = 10?
        JZ      ABORT
        CPI     0BH     ;IS F SWITCH = 11?
        JZ      TEST1
        CPI     0CH     ;IS F SWITCH = 12?
        JZ      TEST2
        CPI     0DH     ;IS F SWITCH = 13?
        JZ      TEST3
        CPI     0EH     ;IS F SWITCH = 14?
        JZ      TEST4
ABORT:  MVI     A,0E0H  ;SET CAL 3864 TO E0.
        STA     3864H
        RET
```

```
LPSTP:  IN      0FAH    ;READ LP STEP SWITCH.
        CMA
        ANI     0FH
        CPI     00H     ;IS SWITCH = 0?
        JZ      ABORT
        CPI     01H     ;IS SWITCH = 1?
        JZ      C25
        CPI     02H     ;IS SWITCH = 2?
        JZ      C24
        CPI     03H     ;IS SWITCH = 3?
        JZ      C23
        CPI     04H     ;IS SWITCH = 4?
        JZ      C22
        CPI     05H     ;IS SWITCH = 5?
        JZ      C21
C20:    MVI     A,20H   ;SWITCH IS 6 OR GREATER SO OUTPUT LEVEL 6.
        STA     3864H
        RET
C21:    MVI     A,21H   ;OUTPUT LEVEL 5.
        STA     3864H
        RET
C22:    MVI     A,22H   ;OUTPUT LEVEL 4.
        STA     3864H
        RET
C23:    MVI     A,23H   ;OUTPUT LEVEL 3.
        STA     3864H
        RET
C24:    MVI     A,24H   ;OUTPUT LEVEL 2.
        STA     3864H
        RET
C25:    MVI     A,25H   ;OUTPUT LEVEL 1.
        STA     3864H
        RET
SPSTP:  IN      0F8H    ;READ SP STEP SWITCH.
        RAR
        RAR
        RAR
        RAR
        ANI     0FH
        CPI     00H     ;IS SWITCH = 0?
        JZ      ABORT
        CPI     01H     ;IS SWITCH = 1.
        JZ      C83
        CPI     02H     ;IS SWITCH = 2.
        JZ      C82
        CPI     03H     ;IS SWITCH = 3.
        JZ      C81
C80:    MVI     A,80H   ;OUTPUT LEVEL 4.
        STA     3864H
        RET
C81:    MVI     A,81H   ;OUTPUT LEVEL 3.
        STA     3864H
        RET
```

```
C82:    MVI     A,82H   ;OUTPUT LEVEL 2.
        STA     3864H
        RET
C83:    MVI     A,83H   ;OUTPUT LEVEL 1.
        STA     3864H
        RET
SPSIN:  IN      0FAH    ;READ SP DAILY SINE SWITCH
        CMA
        RAR             ;DATA IS HI PART OF PORT.
        RAR
        RAR
        RAR
        ANI     0FH
        CPI     00H     ;IS SWITCH = 0?
        JZ      ABORT
        CPI     01H     ;IS SWITCH = 1?
        JZ      C88
        CPI     02H     ;IS SWITCH = 2?
        JZ      C87
        CPI     03H     ;IS SWITCH = 3?
        JZ      C86
        CPI     04H     ;IS SWITCH = 4?
        JZ      C85
C84:    MVI     A,84H   ;OUTPUT LEVEL 5.
        STA     3864H
        RET
C85:    MVI     A,85H   ;OUTPUT LEVEL 4.
        STA     3864H
        RET
C86:    MVI     A,86H   ;OUTPUT LEVEL 3.
        STA     3864H
        RET
C87:    MVI     A,87H   ;OUTPUT LEVEL 2.
        STA     3864H
        RET
C88:    MVI     A,88H   ;OUTPUT LEVEL 1.
        STA     3864H
        RET
LPSIN:  IN      0F9H    ;READ LP DAILY SINE SWITCH.
        CMA
        ANI     0FH     ;LOWER PART OF PORT.
        CPI     00H     ;IS SWITCH = 0?
        JZ      ABORT
        CPI     01H     ;IS SWITCH = 1?
        JZ      C26
        CPI     02H     ;IS SWITCH = 2?
        JZ      C27
        CPI     03H     ;IS SWITCH = 3?
        JZ      C28
        CPI     04H     ;IS SWITCH = 4?
        JZ      C29
C2A:    MVI     A,2AH   ;OUTPUT LEVEL 5.
        STA     3864H
```

```
        RET
C29:    MVI     A,29H   ;OUTPUT LEVEL 4.
        STA     3864H
        RET
C28:    MVI     A,28H   ;OUTPUT LEVEL 3
        STA     3864H
        RET
C27:    MVI     A,27H   ;OUTPUT LEVEL 2.
        STA     3864H
        RET
C26:    MVI     A,26H   ;OUTPUT LEVEL 1.
        STA     3864H
        RET
IPRES:  MVI     A,40H   ;OUTPUT IP SINE RESPONSE CODE.
        STA     3864H
        RET
SPRES:  MVI     A,89H   ;OUTPUT SP SINE RESPONSE CODE.
        STA     3864H
        RET
LPRES:  MVI     A,4BH   ;OUTPUT LP SINE RESPONSE CODE.
        STA     3864H
        RET
IPPHO:  IN      0F9H    ;READ IP PHOTO SWITCH.
        CMA
        RAR             ;HI PART OF PORT.
        RAR
        RAR
        RAR
        ANI     0FH
        CPI     00H     ;IS SWITCH = 0?
        JZ      ABORT
        CPI     01H     ;IS SWITCH = 1?
        JZ      C2B
        CPI     02H     ;IS SWITCH = 2?
        JZ      C2C
        CPI     03H     ;IS SWITCH = 3?
        JZ      C2D
        CPI     04H     ;IS SWITCH = 4?
        JZ      C2E
C2F:    MVI     A,2FH   ;OUTPUT LEVEL 5.
        STA     3864H
        RET
C2E:    MVI     A,2EH   ;OUTPUT LEVEL 4.
        STA     3864H
        RET
C2D:    MVI     A,2DH   ;OUTPUT LEVEL 3.
        STA     3864H
        RET
C2C:    MVI     A,2CH   ;OUTPUT LEVEL 2.
        STA     3864H
        RET
C2B:    MVI     A,2BH   ;OUTPUT LEVEL 1.
        STA     3864H
```

```
        RET
TEST1:  MVI     A,0E1H  ;OUTPUT 128 POINT TEST CODE.
        STA     3864H
        RET
TEST2:  MVI     A,0E2H  ;OUTPUT 64 POINT TEST CODE.
        STA     3864H
        RET
TEST3:  MVI     A,0E3H  ;OUTPUT TEST 3 CODE.
        STA     3864H
        RET
TEST4:  MVI     A,0E4H  ;OUTPUT TEST 4 CODE.
        STA     3864H
        RET
                        ;THIS IS THE TIME PROGRAM SEGMENT FOR THE
                        ;WWSSN DRS MICROPROCESSOR PROGRAM UP1
                        ;USING SYSTRON DONNER DIGITAL CLOCK MOD. 8110.
STIME:  MVI     A,01H   ;LOAD  M/SEC ONES AND TENS STROBE.
        CMA
        OUT     0EAH
        NOP
        NOP
        IN      0E8H    ;INPUT M/SEC ONES AND TENS.
        CMA
        MOV     B,A     ;TEMP.  STORE IN REG B.
        MVI     A,02H   ;LOAD SECONDS ONES AND M/SEC HUNDREDS.
        CMA
        OUT     0EAH
        NOP
        NOP
        IN      0E8H    ;INPUT SECONDS UNITS AND M/SEC HUNDREDS
        CMA
        MOV     C,A
        MOV     A,B
        RRC
        RRC
        RRC
        RRC
        ANI     0FH
        MOV     E,A
        MOV     A,C
        RRC
        RRC
        RRC
        RRC
        MOV     D,A
        ANI     0F0H
        ORA     E
        STA     3825H
        MVI     A,04H   ;LOAD TENS SEC.  AND ONES MIN.
        CMA
        OUT     0EAH
        NOP
        NOP
```

```
IN      0E8H    ;INPUT TENS SEC.  AND ONES MIN.
CMA
RRC
RRC
RRC
RRC
MOV     B,A     ;TEMP.  STORE IN REG. B
ANI     0F0H
MOV     C,A
MOV     A,D
ANI     0FH
ORA     C
STA     3824H
MVI     A,08H     ;LOAD HOURS ONES AND MIN TENS
CMA
OUT     0EAH
NOP
NOP
IN      0E8H       ;INPUT HOURS ONES AND MIN.  TENS
CMA
RRC
RRC
RRC
RRC
MOV     D,A
ANI     0F0H
MOV     C,A
MOV     A,B
ANI     0FH
ORA     C
STA     3823H
MVI     A,10H     ;LOAD DAYS ONES AND HOURS TENS STROBE
CMA
OUT     0EAH
NOP
NOP
IN      0E8H    ;INPUT DAYS ONES AND HOURS TENS
CMA
RRC
RRC
RRC
RRC
MOV     B,A
ANI     0F0H
MOV     C,A
MOV     A,D
ANI     0FH
ORA     C
STA     3822H
MVI     A,20H   ;LOAD DAYS HUNDREDS AND DAYS TENS STROBE
CMA
OUT     0EAH
NOP
```

```
        NOP
        IN      0E8H    ;INPUT DAYS HUNDREDS AND DAYS TENS
        CMA
        RRC
        RRC
        RRC
        RRC
        MOV     C,A
        ANI     0F0H
        MOV     D,A
        MOV     A,B
        ANI     0FH
        ORA     D
        STA     3821H
        MOV     A,C
        ANI     0FH
        MOV     C,A
        IN      0E9H
        ANI     0F0H
        ORA     C
        STA     3820H
        MVI     A,0FFH  ;RESET SYSTRON DONNER TIME PORT.
        OUT     0EAH
        RET
SPTIME: LHLD    3832H   ;LOAD SP POINTER INTO REG'S H&L.
        LDA     3808H   ;IS SP 2ND EVENT FLAG=0?
        ANA     A
        JZ      SPEVNT
SPAGAI: LHLD    3832H   ;IS SP POINTER AT THE END + 1 OF SP
        MOV     A,L     ;RECORD #3?
        CPI     70H     ;IF SO JUMP TO STAR1.
        JZ      STAR1
        MOV     A,L     ;IS SP POINTER AT THE END + 1 OF SP
        CPI     0A0H    ;RECORD #2?
        JZ      STAR2   ;IF SO JUMP TO STAR2
        MOV     A,L     ;IS SP POINTER AT THE END + 1 OF SP
        CPI     0D0H    ;RECORD #1?
        JZ      STAR3   ;IF SO JUMP TO STAR3.
        LDA     382EH   ;INCREMENT SP FORMAT ERROR.
        INR     A
        STA     382EH
        RET
STAR3:  LXI     H,0C7D0H;SET SP RECORD POINTER DATA #2 EQUAL TO
        SHLD    0FE8AH  ;END+ 1 OF RECORD #1.
        JMP     SPE0
STAR1:  LXI     H,0D770H;SET SP RECORD POINTER DATA #2 EQUAL TO
        SHLD    0FE8AH  ;END; 1 OF RECORD #3.
        JMP     SPE0
STAR2:  LXI     H,0CFA0H;SET SP RECORD POINTER DATA #2 EQUAL TO
        SHLD    0FE8AH  ;END+ 1 RECORD #2.
SPE0:   LDA     03F28H  ;IS SP EVENT =0?
        ANA     A       ;IF NOT JUMP TO MOVE SP POINTER.
        JNZ     MSPP
```

```
        MVI     A,00H    ;SET SP 2ND EVENT = 0.
        STA     3808H
        JMP     MSPP
SPEVNT: LDA     3F28H    ;IS SP EVENT = 0?
        ANA     A        ;IF SO JUMP TO  MOVE SP POINTER.
        JZ      MSPP
        MVI     A,0FFH   ;SET SP 2ND EVENT = 1.
        STA     3808H
        MOV     A,L      ;IS SP POINTER AT END+1 OF SP RECORD #3? (70).
        CPI     70H      ;IF SO JUMP TO MOON1.
        JZ      MOON1
        MOV     A,L      ;IS SP POINTER AT END+1 OF SP RECORD #2? (A0).
        CPI     0A0H     ;IF SO JUMP TO MOON2.
        JZ      MOON2
MOON3:  LDA     0CFA9H   ;SET BIT #4, BYTE #10 FOR ONE PRE EVENT RECORD,
        ORI     10H      ;SP RECORD #3.
        STA     0CFA9H
        LXI     H,0D770H;SET SP RECORD POINTER DATA #1 (1ST RECORD TO
        SHLD    0FE88H   ;BE WRITTEN) EQUAL TO END+1 OF RECORD #3.
        JMP     SPAGAI
MOON1:  LDA     0C7D9H   ;SET BIT #4, BYTE #10, SP RECORD #2.
        ORI     10H
        STA     0C7D9H
        LXI     H,0CFA0H;SET SP RECORD POINTER DATA #1 (1ST RECORD TO BE
        SHLD    0FE88H   ;WRITTEN) EQUAL TO END+1 OF RECORD #2.
        JMP     SPAGAI
MOON2:  LDA     0C009H   ;SET BIT #4, Byte #10, SP RECORD #1.
        ORI     10H
        STA     0C009H
        LXI     H,0C7D0H;SET SP RECORD POINTER DATA #1 (1ST RECORD TO BE
        SHLD    0FE88H   ;WRITTEN) EQUAL TO END+1 OF RECORD #1.
        JMP     SPAGAI
MSPP:   LHLD    3832H    ;IS SP MsBYTE POINTER = END RECORD #3?
        MOV     A,H      ;IF SO JUMP TO SET BYTE #1.
        CPI     0D7H
        JNZ     SETBY1
        MOV     A,L
        CPI     70H
        JNZ     SETBY1
        LXI     H,0C000H;RESET SP POINTER FROM END RECORD #3 TO BEGINNING
        SHLD    3832H    ;OF RECORD #1.
SETBY1: MVI     A,64H    ;SET RECORD BYTE #1 TO STATION ID.
        MOV     M,A
        INX     H
SETBY2: MVI     A,20H    ;SET RECORD BYTE #2 TO RECORD SAMPLE RATE.
        MOV     M,A
        INX     H
        SHLD    3832H    ;RESTORE H,L TO SP POINTER LOCATION.
        CALL    STIME     ;CALL TIME SUBROUTINE.
SETBY3: LHLD    3832H    ;SET RECORD BYTE #3 TO 1'S YEARS AND
        LDA     3820H    ;100'S DAYS.
        MOV     M,A
        INX     H
```

```
SETBY4: LDA     3821H   ;SET RECORD BYTE #4 TO 10'S DAYS AND
        MOV     M,A     ;1'S DAYS.
        INX     H
SETBY5: LDA     3822H   ;SET RECORD BYTE #5 TO 10'S HOURS AND
        MOV     M,A     ;1'S HOURS.
        INX     H
SETBY6: LDA     3823H   ;SET RECORD BYTE #6 TO 10'S MIN AND
        MOV     M,A     ;1'S MIN.
        INX     H
SETBY7: LDA     3824H   ;SET RECORD BYTE #7 TO 10'S SEC AND
        MOV     M,A     ;1'S SEC.
        INX     H
SETBY8: LDA     3825H   ;SET RECORD BYTE #8 TO 100'S MSEC AND
        MOV     M,A     ;10'S MSEC.
        INX     H
SETBY9: MVI     A,01H   ;SET RECORD BYTE #9 TO NUMBER OF CHANNELS.
        MOV     M,A
        INX     H
SETBYA: LDA     3826H   ;WRITE SP MAILBOX INTO BYTE 10.
        MOV     M,A
        MVI     A,00H   ;CLEAR SP BYTE #10 MAILBOX =00.
        STA     3826H
        INX     H
SETBYB: LDA     3810H   ;SET RECORD BYTE #11 TO DIGISWITCH #B.
        MOV     M,A
        INX     H
SETBYC: LDA     3811H   ;SET RECORD BYTE #12 TO DIGISWITCH #C.
        MOV     M,A
        INX     H
SETBYD: LDA     3812H   ;SET RECORD BYTE #13 TO DIGISWITCH #D.
        MOV     M,A
        INX     H
SETBYE: LDA     3829H   ;SET RECORD BYTE #14 TO CALCODE.
        MOV     M,A
        INX     H
SETBYF: LDA     382AH   ;SET RECORD BYTE #15 TO ADC ERROR TYPE 1,
        MOV     M,A     ;REC ADC CODE NOT EQUAL TO 10,11,12,OR 13.
        INX     H
SETBYG: LDA     382BH   ;SET RECORD BYTE #16 TO ADC ERROR TYPE 2,
        MOV     M,A     ;ADC PAST CODE NOT EQUAL TO REC ADC CODE.
        INX     H
SETBYH: LDA     382EH   ;SET RECORD BYTE #17 TO SP FORMAT ERROR.
        MOV     M,A
        INX     H
SETBYX: MVI     A,00H   ;SET RECORD BYTES 18 TO 20 = 00.
        MOV     M,A     ;BYTE 18 = 00.
        INX     H
        MOV     M,A     ;BYTE 19 = 00.
        INX     H
        MOV     M,A     ;BYTE 20 = 00.
        INX     H
        SHLD    3832H   ;RESTORE H,L TO SP POINTER LOOKING AT BYTE # 21.
        RET
```

```
IPTIME: LHLD    3836H   ;LOAD IP POINTER INTO REG'S H&L.
        LDA     3814H   ;IS IP 2ND EVENT FLAG=0?
        ANA     A
        JZ      IPEVNT
IPAGAI: LHLD    3836H   ;IS IP POINTER AT THE END + 1 OF IP
        MOV     A,L     ;RECORD #3?
        CPI     0E0H    ;IF SO JUMP TO WSTAR1.
        JZ      WSTAR1
        MOV     A,L     ;IS IP POINTER AT THE END + 1 OF IP
        CPI     10H     ;RECORD #2?
        JZ      WSTAR2  ;IF SO JUMP TO WSTAR2
        MOV     A,L     ;IS IP POINTER AT THE END +1 OF IP
        CPI     40H     ;RECORD #1?
        JZ      WSTAR3
        LDA     382FH   ;INCREMENT IP FORMAT ERROR.
        INR     A
        STA     382FH
        RET
WSTAR3: LXI     H,0DF40H;SET IP RECORD POINTER DATA #2 EQUAL TO
        SHLD    0FE90H  ;END+ 1 OF RECORD #1.
        JMP     IPE0
WSTAR1: LXI     H,0EEE0H;SET IP RECORD POINTER DATA #2 EQUAL TO
        SHLD    0FE90H  ;END; 1 OF RECORD #3.
        JMP     IPE0
WSTAR2: LXI     H,0E710H;SET IP RECORD POINTER DATA #2 EQUAL TO
        SHLD    0FE90H  ;END+ 1 RECORD #2.
IPE0:   LDA     03F70H  ;IS IP EVENT =0?
        ANA     A       ;IF NOT JUMP TO MOVE IP POINTER.
        JNZ     MIPP
        MVI     A,00H   ;SET IP 2ND EVENT = 0.
        STA     3814H
        JMP     MIPP
IPEVNT: LDA     3F70H   ;IS IP EVENT = 0?
        ANA     A       ;IF SO JUMP TO  MOVE IP POINTER.
        JZ      MIPP
        MVI     A,0FFH  ;SET IP 2ND EVENT = 1.
        STA     3814H
        MOV     A,L     ;IS IP POINTER AT END+1 OF IP RECORD #3? (E0).
        CPI     0E0H    ;IF SO JUMP TO IMOON1.
        JZ      IMOON1
        MOV     A,L     ;IS IP POINTER AT END+1 OF IP RECORD #2? (10).
        CPI     10H     ;IF SO JUMP TO IMOON2.
        JZ      IMOON2
IMOON3: LDA     0E719H  ;SET BIT #4, BYTE #10 FOR ONE PRE-EVENT RECORD,
        ORI     10H     ;IP RECORD #3. RD.
        STA     0E719H
        LXI     H,0EEE0H;SET IP RECORD POINTER DATA #1 (1ST RECORD TO
        SHLD    0FE8EH  ;BE WRITTEN) EQUAL TO END+1 OF RECORD #3.
        JMP     IPAGAI
IMOON1: LDA     0DF49H  ;SET BIT #4, BYTE #10, IP RECORD #2 TO 1.
        ORI     10H
        STA     0DF49H
        LXI     H,0E710H;SET IP RECORD POINTER DATA #1 (1ST RECORD TO BE
```

```
        SHLD    0FE8EH  ;WRITTEN) EQUAL TO END+1 OF RECORD #2.
        JMP     IPAGAI
IMOON2: LDA     0D779H  ;SET BIT #4, BYTE #10, IP RECORD #1 TO 1.
        ORI     10H
        STA     0D779H
        LXI     H,0DF40H;SET IP RECORD POINTER DATA #1 (1ST RECORD TO BE
        SHLD    0FE8EH  ;WRITTEN) EQUAL TO END+1 OF RECORD #1.
        JMP     IPAGAI
MIPP:   LHLD    3836H   ;IS IP MSBYTE POINTER = END RECORD #3?
        MOV     A,H     ;IF SO JUMP TO SET BYTE #1.
        CPI     0EEH
        JNZ     ISETB1
        MOV     A,L
        CPI     0E0H
        JNZ     ISETB1
        LXI     H,0D770H;RESET IP POINTER FROM END RECORD #3 TO BEGINNING
        SHLD    3836H   ;OF RECORD #1.
ISETB1: MVI     A,64H   ;SET RECORD BYTE #1 TO STATION ID.
        MOV     M,A
        INX     H
ISETB2: MVI     A,10H   ;SET RECORD BYTE #2 TO RECORD SAMPLE RATE.
        MOV     M,A
        INX     H
        SHLD    3836H   ;RESTORE H,L TO IP POINTER LOCATION.
        CALL    STIME    ;CALL TIME SUBROUTINE.
ISETB3: LHLD    3836H   ;SET RECORD BYTE #3 TO 1'S YEARS AND
        LDA     3820H   ;100'S DAYS.
        MOV     M,A
        INX     H
ISETB4: LDA     3821H   ;SET RECORD BYTE #4 TO 10'S DAYS AND
        MOV     M,A     ;1'S DAYS.
        INX     H
ISETB5: LDA     3822H   ;SET RECORD BYTE #5 TO 10'S HOURS AND
        MOV     M,A     ;1'S HOURS.
        INX     H
ISETB6: LDA     3823H   ;SET RECORD BYTE #6 TO 10'S MIN AND
        MOV     M,A     ;1'S MIN.
        INX     H
ISETB7: LDA     3824H   ;SET RECORD BYTE #7 TO 10'S SEC AND
        MOV     M,A     ;1'S SEC.
        INX     H
ISETB8: LDA     3825H   ;SET RECORD BYTE #8 TO 100'S MSEC AND
        MOV     M,A     ;10'S MSEC.
        INX     H
ISETB9: MVI     A,03H   ;SET RECORD BYTE #9 TO NUMBER OF CHANNELS.
        MOV     M,A
        INX     H
ISETBA: LDA     3827H   ;LOAD IP MAILBOX INTO BYTE 10.
        MOV     M,A
        MVI     A,00H   ;CLEAR SP BYTE #10 MAILBOX =00.
        STA     3827H
        INX     H
ISETBB: LDA     3810H   ;SET RECORD BYTE #11 TO DIGISWITCH #B.
```

```
          MOV     M,A
          INX     H
ISETBC:   LDA     3811H    ;SET RECORD BYTE #12 TO DIGISWITCH #C.
          MOV     M,A
          INX     H
ISETBD:   LDA     3812H    ;SET RECORD BYTE #13 TO DIGISWITCH #D.
          MOV     M,A
          INX     H
ISETBE:   LDA     3829H    ;SET RECORD BYTE #14 TO CAL CODE.
          MOV     M,A
          INX     H
ISETBF:   LDA     382AH    ;SET RECORD BYTE #15 TO ADC ERROR TYPE 1,
          MOV     M,A      ;REC ADC CODE NOT EQUAL TO 10,11,12,OR 13.
          INX     H
ISETBG:   LDA     382BH    ;SET RECORD BYTE #16 TO ADC ERROR TYPE 2,
          MOV     M,A      ;ADC PAST CODE NOT EQUAL TO REC ADC CODE.
          INX     H
ISETBH:   LDA     382FH    ;SET RECORD BYTE #17 TO IP FORMAT ERROR.
          MOV     M,A
          INX     H
ISETBX:   MVI     A,00H    ;SET RECORD BYTES 18 TO 20 = 00.
          MOV     M,A      ;BYTE 18 = 00.
          INX     H
          MOV     M,A      ;BYTE 19 = 00.
          INX     H
          MOV     M,A      ;BYTE 20 = 00.
          INX     H
          SHLD    3836H    ;RESTORE H,L TO SP POINTER LOOKING AT BYTE # 21.
          RET
LPTIM2:   LXI     H,0F6B0H;SET LP RECORD POINTER TO START ADDRESS
          SHLD    383AH    ;OF RECORD #2.
          SHLD    0FE86H   ;SET LP RECORD TO BE WRITTEN ON TAPE.
          JMP     TIMELP
LPTIM1:   LXI     H,0FE80H;SET LP RECORD POINTER TO END + 1 OF SECOND RECORD
          SHLD    0FE86H
          LXI     H,0EEE0H;SET LP RECORD POINTER TO START ADDRESS
          SHLD    383AH    ;OF RECORD #1.
TIMELP:   MVI     A,64H    ;SET RECORD BYTE #1 TO STATION ID.
          MOV     M,A
          INX     H
LSETB2:   MVI     A,01     ;SET RECORD BYTE #2 TO RECORD SAMPLE RATE.
          MOV     M,A
          INX     H
          SHLD    383AH    ;RESTORE H,L TO LP POINTER LOCATION.
          CALL    STIME     ;CALL TIME SR.
LSETB3:   LHLD    383AH    ;SET RECORD BYTE #3 TO 1'S YEARS AND
          LDA     3820H    ;100'S DAYS.
          MOV     M,A
          INX     H
LSETB4:   LDA     3821H    ;SET RECORD BYTE #4 TO 10'S DAYS AND
          MOV     M,A      ;1'S DAYS.
          INX     H
LSETB5:   LDA     3822H    ;SET RECORD BYTE #5 TO 10'S HOURS AND
```

```
        MOV     M,A
        INX     H
LSETB6: LDA     3823H   ;SET RECORD BYTE #6 TO 10'S MINUTES AND
        MOV     M,A     ;1'S MINUTES.
        INX     H
LSETB7: LDA     3824H   ;SET RECORD BYTE #7 TO 10'S SEC AND
        MOV     M,A     ;1'S SEC.
        INX     H
LSETB8: LDA     3825H   ;SET RECORD BYTE #8 TO 100'S MSEC AND
        MOV     M,A     ;10'S MSEC.
        INX     H
LSETB9: MVI     A,03H   ;SET RECORD BYTE #9 TO NUMBER OF CHANNELS.
        MOV     M,A
        INX     H
LSETBA: LDA     3828H   ;LOAD LP MAILBOX INTO BYTE 10.
        MOV     M,A
        MVI     A,00H   ;SET RECORD BYTE #10 MAILBOX = 0.
        STA     3828H   ;SET LP RECORD BYTE #10 = 0.
        INX     H
LSETBB: LDA     3810H   ;SET RECORD BYTE #11 TO DIGISWITCH #B.
        MOV     M,A
        INX     H
LSETBC: LDA     3811H   ;SET RECORD BYTE #12 TO DIGISWITCH #C.
        MOV     M,A
        INX     H
LSETBD: LDA     3812H   ;SET RECORD BYTE #13 TO DIGISWITCH #D.
        MOV     M,A
        INX     H
LSETBE: LDA     3829H   ;SET RECORD BYTE #14 TO CAL CODE.
        MOV     M,A
        INX     H
LSETBF: LDA     382AH   ;SET RECORD BYTE TO ADC ERROR TYPE 1,
        MOV     M,A     ;REC ADC CODE NOT EQUAL TO 10,11,12,OR 13.
        INX     H
LSETBG: LDA     382BH   ;SET RECORD BYTE TO ADC ERROR TYPE 2,
        MOV     M,A     ;ADC PAST CODE NOT EQUAL TO REC ADC CODE.
        INX     H
LSETBX: MVI     A,00H   ;SET RECORD BYTE #17 TO 20 = 0.
        MOV     M,A     ;BYTE 17 = 00.
        INX     H
        MOV     M,A     ;BYTE 18 = 00.
        INX     H
        MOV     M,A     ;BYTE 19 = 00.
        INX     H
        MOV     M,A     ;BYTE 20 = 00.
        INX     H
        SHLD    383AH   ;RESTORE H,L TO LP POINTER LOOKING AT BYTE #21.
        RET
        END
```

APPENDIX A.2

8080 PROGRAM LISTING
MICROPROCESSOR TWO

```
        ;THIS IS WWSSN DRS TELEMETRY MICROPROCESSOR TWO PROGRAM.
        ;MICROPROCESSOR FOUR IS THE REMOTE TRANSMITT UNIT.
START:  NOP             ;UP2 PROGRAM START.
UPTHR:  DI              ;DISABLE INTERRUPTS.
        NOP             ;THIS AREA IS RESERVED FOR VECTORED INTERRUPTS.
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
AGAIN:  DI              ;DISABLE INTERRUPTS.
```

```
        LXI     SP,3F00H;SET STACK POINTER ADDRESS.
        LXI     H,38FFH ;SET MEMORY POINTER.
        MVI     A,80H   ;THIS IS SOFTWARE RESET FOR SERIAL I/O.
        OUT     0EDH
        MVI     A,00H
        OUT     0EDH
        MVI     A,40H
        OUT     0EDH
        MVI     A,1CH   ;OUTPUT RECEIVE MODE INSTRUCTION, 2 SYNC & PARITY.
        OUT     0EDH
        MVI     A,0AAH  ;DEFINE FIRST SYNC WORD.
        OUT     0EDH
        MVI     A,0AAH  ;DEFINE SECOND SYNC WORD.
        OUT     0EDH    .
        MVI     A,86H   ;OUTPUT REC COMMAND WORD.
        OUT     0EDH
        IN      0ECH    ;READ DATA TO CLEAR INPUT READ REGISTER.
SYND1:  IN      0EDH    ;CHECK SYNC DET.
        ANI     40H
        JZ      SYND1
RXRE1:  IN      0EDH    ;CHECK FOR FIRST WORD.
        ANI     02H
        JZ      RXRE1
        IN      0ECH    ;INPUT FIRST WORD.
        MOV     M,A
        INX     H       ;INCREMENT MEMORY POINTER.
RXRE2:  IN      0EDH    ;CHECK FOR SECOND WORD.
        ANI     02H
        JZ      RXRE2
        IN      0ECH    ;INPUT SECOND WORD.
        MOV     M,A     ;STORE IN 80/20 RAM MEMORY.
        INX     H       ;INCREMENT MEMORY POINTER.
RXRE3:  IN      0EDH    ;CHECK FOR THIRD WORD.
        ANI     02H
        JZ      RXRE3
        IN      0ECH    ;INPUT THIRD WORD.
        MOV     M,A     ;STORE IN 80/20 RAM MEMORY.
        INX     H       ;INCREMENT MEMORY POINTER.
RXRE4:  IN      0EDH    ;CHECK FOR FOURTH WORD.
        ANI     02H
        JZ      RXRE4
        IN      0ECH    ;INPUT FOURTH WORD.
        MOV     M,A     ;STORE IN 80/20 RAM MEMORY.
        INX     H       ;INCREMENT MEMORY POINTER.
RXRE5:  IN      0EDH    ;CHECK FOR FIFTH WORD.
        ANI     02H
        JZ      RXRE5
        IN      0ECH    ;INPUT FIFTH WORD.
        MOV     M,A     ;STORE IN 80/20 RAM MEMORY.
        INX     H       ;INCREMENT MEMORY POINTER.
RXRE6:  IN      0EDH    ;CHECK FOR SIXTH WORD.
        ANI     02H
        JZ      RXRE6
```

```
        IN      0ECH    ;INPUT SIXTH WORD.
        MOV     M,A     ;STORE IN 80/20 RAM MEMORY.
        INX     H       ;INCREMENT MEMORY POINTER.
RXRE7:  IN      0EDH    ;CHECK FOR SEVENTH WORD.
        ANI     02H
        JZ      RXRE7
        IN      0ECH    ;INPUT SEVENTH WORD.
        MOV     M,A     ;STORE IN 80/20 RAM MEMORY.
        INX     H       ;INCREMENT MEMORY POINTER.
RXRE8:  IN      0EDH    ;CHECK FOR EIGHTH WORD.
        ANI     02H
        JZ      RXRE8
        IN      0ECH    ;INPUT EIGHTH WORD.
        MOV     M,A     ;STORE IN 80/20 RAM MEMORY.
        INX     H       ;INCREMENT MEMORY POINTER.
RXRE9:  IN      0EDH    ;CHECK FOR NINTH WORD.
        ANI     02H
        JZ      RXRE9
        IN      0ECH    ;INPUT NINTH WORD.
        MOV     M,A     ;STORE IN 80/20 RAM MEMORY.
        LXI     D,0FF00H;LOAD 116 MEMORY ADDRESS.
        LXI     H,38FFH ;LOAD UP2 MEMORY ADDRESS.
MOVE1:  MOV     A,M     ;LOAD FIRST UP2 WORD FOR TRANSFER.
        XCHG
        MOV     M,A     ;LOAD WORD IN 116 MEMORY.
        INX     H       ;INCREMENT 116 MEMORY POINTER.
        XCHG
        INX     H       ;INCREMENT UP2 MEMORY POINTER.
MOVE2:  MOV     A,M     ;LOAD SECOND UP2 WORD FOR TRANSFER.
        XCHG
        MOV     M,A     ;LOAD WORD IN 116 MEMORY.
        INX     H       ;INCREMENT 116 MEMORY POINTER.
        XCHG
        INX     H       ;INCREMENT UP2 MEMORY POINTER.
MOVE3:  MOV     A,M     ;LOAD THIRD- UP2 WORD FOR TRANSFER.
        XCHG
        MOV     M,A     ;LOAD WORD IN 116 MEMORY.
        INX     H       ;INCREMENT 116 MEMORY POINTER.
        XCHG
        INX     H       ;INCREMENT UP2 MEMORY POINTER.
MOVE4:  MOV     A,M     ;LOAD FOURTH UP2 WORD FOR TRANSFER.
        XCHG
        MOV     M,A     ;LOAD WORD IN 116 MEMORY.
        INX     H       ;INCREMENT 116 MEMORY POINTER.
        XCHG
        INX     H       ;INCREMENT UP2 MEMORY POINTER.
MOVE5:  MOV     A,M     ;LOAD FIFTH UP2 WORD FOR TRANSFER.
        XCHG
        MOV     M,A     ;LOAD WORD IN 116 MEMORY.
        INX     H       ;INCREMENT 116 MEMORY POINTER.
        XCHG
        INX     H       ;INCREMENT UP2 MEMORY POINTER.
MOVE6:  MOV     A,M     ;LOAD SIXTH UP2 WORD FOR TRANSFER.
```

```
        XCHG
        MOV     M,A         ;LOAD WORD IN 116 MEMORY.
        INX     H           ;INCREMENT 116 MEMORY POINTER.
        XCHG
        INX     H           ;INCREMENT UP2 MEMORY POINTER.
MOVE7:  MOV     A,M         ;LOAD SEVENTH UP2 WORD FOR TRANSFER.
        XCHG
        MOV     M,A         ;LOAD WORD IN 116 MEMORY.
        INX     H           ;INCREMENT 116 MEMORY POINTER.
        XCHG
        INX     H           ;INCREMENT UP2 MEMORY POINTER.
MOVE8:  MOV     A,M         ;LOAD EIGHTH UP2 WORD FOR TRANSFER.
        XCHG
        MOV     M,A         ;LOAD WORD IN 116 MEMORY.
        INX     H           ;INCREMENT 116 MEMORY POINTER.
        XCHG
        INX     H           ;INCREMENT UP2 MEMORY POINTER.
MOVE9:  MOV     A,M         ;LOAD NINTH UP2 WORD FOR TRANSFER.
        XCHG
        MOV     M,A
        JMP     AGAIN
        END
```

APPENDIX A.3

8080 PROGRAM LISTING
MICROPROCESSOR THREE

```
        ;MAY 26,1982
        ;ASYNCHRONOUS VERSION 1.0
        ;THIS IS WWSSN DRS TELEMETRY MICROPROCESSOR THREE PROGRAM.
        ;
        ;MICROPROCESSOR THREE IS THE REMOTE RECEIVE UNIT.
        ;MICROPROCESSOR FOUR IS THE REMOTE TRANSMIT UNIT.
START:  NOP                 ;UP3 PROGRAM START.
        NOP                 ;THIS AREA IS RESERVED FOR VECTORED INTERRUPTS.
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        LXI     SP,3F00H;SET STACK POINTER ADDRESS.
        MVI     A,89H   ;PROGRAM PORTS (J2) E8 AND E9 OUTPUT, EA INPUT.
        OUT     0EBH
UPTHR:  DI              ;DISABLE INTERRUPTS
        MVI     A,80H   ;THIS IS SOFTWARE RESET FOR SERIAL I/O.
        OUT     0EDH
        MVI     A,00H
        OUT     0EDH
        MVI     A,40H
        OUT     0EDH
```

```
        MVI     A,1CH   ;OUTPUT RECEIVE MODE INSTRUCTION.
        OUT     0EDH
        MVI     A,0AAH  ;DEFINE SYNC WORD.
        OUT     0EDH
        MVI     A,0AAH  ;DEFINE SYNC WORD,
        OUT     0EDH
        MVI     A,86H   ;OUTPUT REC COMMAND WORD.
        OUT     0EDH
        IN      0ECH    ;READ DATA TO CLEAR INPUT READ REGISTER.
SYND1:  IN      0EDH    ;CHECK SYNC DET.
        ANI     40H
        JZ      SYND1
RXRE1:  IN      0EDH    ;CHECK FOR FIRST WORD.
        ANI     02H
        JZ      RXRE1
        IN      0ECH    ;INPUT FIRST WORD.
        OUT     0E8H    ;OUTPUT DATA 1 TO UP4 PORT.
        MOV     B,A
        STA     3800H   ;STORE FIRST WORD.
RXRE2:  IN      0EDH    ;CHECK FOR SECOND WORD.
        ANI     02H
        JZ      RXRE2
        IN      0ECH    ;INPUT SECOND WORD.
        MOV     C,A
        STA     3801H   ;STORE SECOND WORD.
        MOV     A,B     ;DATA 1 TEST.
        CPI     12H     ;IS DATA 1 = 12 CODE?
        JZ      DATA2
        CPI     13H     ;IS DATA 1 = 13 CODE?
        JNZ     ENDIT
        MOV     A,C     ;MOVE DATA 2 TO UP4 PORT (ADC).
        OUT     0E8H
        JMP     ENDIT
DATA2:  MOV     A,C     ;OUTPUT DATA 2 TO UP5 (CALIBRATOR).
        OUT     0E9H
ENDIT:  JMP     UPTHR
        END
```

APPENDIX A.4

8080 PROGRAM LISTING
MICROPROCESSOR FOUR

```
        ;MAY 26,1982
        ;ASYNCHRONOUS VERSION 1.0
        ;THIS IS WWSSN DRS TELEMETRY MICROPROCESSOR FOUR PROGRAM.
        ;
        ;MICROPROCESSOR FOUR IS THE REMOTE TRANSMIT UNIT.
        ;MICROPROCESSOR THREE IS THE REMOTE RECEIVE UNIT.
START:  NOP                 ;UP4 PROGRAM START.
        DI                  ;DISABLE INTERRUPTS.
        NOP                 ;THIS AREA IS RESERVED FOR VECTORED INTERRUPTS.
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        DI                  ;DISABLE INTERRUPTS.
        LXI     SP,3F00H;SET STACK POINTER ADDRESS.
        MVI     A,92H   ;SET PORTS E4 AND E5 AS INPUT, E6 AS OUTPUT.
        OUT     0E7H
        MVI     A,9BH   ;SET PORTS E8,E9,AND EA AS INPUT.
        OUT     0EBH
        MVI     A,00H   ;SET START (RAM) = 00.
        STA     3800H
        LXI     H,38FFH ;SET RAM 38FF-39FF = 00.
MEMZ:   MVI     A,00H
        MOV     M,A
        INX     H
        MOV     A,L
```

```
        CPI     OFFH
        JNZ     MEMZ
        MVI     A,80H   ;SOFTWARE RESET SERIAL I/O.
        OUT     OEDH
        MVI     A,00H
        OUT     OEDH
        MVI     A,40H
        OUT     OEDH
RECST:  IN      OE8H    ;INPUT REMOTE PORT,
        MOV     B,A
        ANI     10H     ;IS DATA 1 = 0001 XXXX?
        JZ      LASTA
        LDA     3800H
        CMP     B       ;IS DATA 1 THE SAME AS LAST DATA 1?
        JZ      LASTB
        MOV     A,B     ;STORE NEW DATA 1 AS LAST DATA 1.
        STA     3800H
        MOV     A,B     ;IS DATA 1 = 10 CODE?
        CPI     10H
        JNZ     DATA1
        STA     38FFH   ;STORE ADC CODE FOR TRANSMISSION.
        CALL    SPSR
        CALL    LPSR
        JMP     OUTPUT
DATA1:  MOV     A,B     ;IS DATA 1 = 11 CODE?
        CPI     11H
        JNZ     DATA2
        STA     38FFH   ;STORE ADC CODE FOR TRANSMISSION.
        CALL    SPSR
        CALL    IPSR
        JMP     OUTPUT
DATA2:  MOV     A,B     ;IS DATA 1 = 12 CODE?
        CPI     12H
        JNZ     DATA3
        STA     38FFH   ;STORE ADC CODE FOR TRANSMISSION.
        CALL    SPSR
        IN      OE9H    ;READ AMP SAT STATUS, STORE IN TRANSMIT STORE.
        STA     3902H
        IN      OEAH    ;READ CALCODE IN PROGRESS.
        STA     3903H
        JMP     OUTPUT
DATA3:  MOV     A,B     ;IS DATA 1 = 13 CODE?
        CPI     13H
        JNZ     LASTC
        STA     38FFH   ;STORE ADC CODE FOR TRANSMISSION.
        CALL    SPSR
OUTPUT: LXI     H,38FFH ;SET H,L WITH OUTPUT MEMORY ADDRESS.
        MVI     A,1CH   ;SET TRANSMIT MODE INSTRUCTION, 2 SYNC & PARITY.
        OUT     OEDH
        MVI     A,0AAH  ;OUTPUT SYNC WORD "AA".
        OUT     OEDH
        MVI     A,0AAH  ;OUTPUT SYNC WORD "AA".
        OUT     OEDH
```

```
        MVI     A,33H   ;SET OUTPUT COMMAND WORD.
        OUT     0EDH
TXRE0:  IN      0EDH    ;IS TX READY?
        ANI     01H
        JZ      TXRE0
        MVI     A,0AAH  ;OUTPUT COMMAND SYNC WORD.
        OUT     0ECH
TXRE1:  IN      0EDH    ;IS TX READY?
        ANI     01H
        JZ      TXRE1
        MVI     A,0AAH  ;OUTPUT SYNC WORD TWO.
        OUT     0ECH
TXREA:  IN      0EDH    ;IS TX READY?
        ANI     01H
        JZ      TXREA
        MOV     A,M     ;OUTPUT FIRST DATA BYTE.
        OUT     0ECH
        INX     H       ;INCREMENT MEMORY POINTER.
TXREB:  IN      0EDH    ;IS TX READY?
        ANI     01H
        JZ      TXREB
        MOV     A,M     ;OUTPUT SECOND DATA BYTE.
        OUT     0ECH
        INX     H
TXREC:  IN      0EDH    ;IS TX READY?
        ANI     01H
        JZ      TXREC
        MOV     A,M     ;OUTPUT THIRD DATA BYTE.
        OUT     0ECH
        INX     H       ;INCREMENT MEMORY POINTER.
TXRED:  LDA     38FFH   ;IS DATA 1 EQUAL TO 13 CODE?
        CPI     13H     ;IF NOT JUMP TO TXRED1.
        JNZ     TXRED1
        IN      0E8H    ;WAS 13 CODE SO INPUT T-WORD,
        STA     3902H   ;FOR RETRANSMISSION.
TXRED1: IN      0EDH    ;IS TX READY?
        ANI     01H
        JZ      TXRED1
        MOV     A,M     ;OUTPUT FOURTH DATA BYTE.
        OUT     0ECH
        INX     H       ;INCREMENT MEMORY POINTER.
TXREE:  IN      0EDH    ;IS TX READY?
        ANI     01H
        JZ      TXREE
        MOV     A,M     ;OUTPUT FIFTH DATA BYTE.
        OUT     0ECH
        INX     H       ;INCREMENT MEMORY POINTER.
TXREF:  IN      0EDH    ;IS TX READY?
        ANI     01H
        JZ      TXREF
        MOV     A,M     ;OUTPUT SIXTH DATA BYTE.
        OUT     0ECH
        INX     H       ;INCREMENT MEMORY POINTER.
```

```
TXREG:  IN      0EDH    ;IS TX READY?
        ANI     01H
        JZ      TXREG
        MOV     A,M     ;OUTPUT SEVENTH DATA BYTE.
        OUT     0ECH
        INX     H       ;INCREMENT MEMORY POINTER?
TXREH:  IN      0EDH    ;IS TX READY?
        ANI     01H
        JZ      TXREH
        MOV     A,M     ;OUTPUT EIGHT DATA BYTE.
        OUT     0ECH
        INX     H
TXREI:  IN      0EDH    ;IS TX READY?
        ANI.    01H
        JZ      TXREI
        MOV     A,M     ;OUTPUT NINTH DATA BYTE.
        OUT     0ECH
ENDIT:  IN      0EDH    ;WAIT FOR LAST (EIGHT) DATA BYTE TO BE TRANSMITTED
        ANI     01H
        JZ      ENDIT
        MVI     A,00H   ;OUTPUT DUMMY WORD.
        OUT     0ECH    ;THIS ALLOWS THE LAST (EIGHT) DATA BYTE TO BE
ENDY:   IN      0EDH    ;COMPLETED IN TRANSMISSION.
        ANI     01H
        JZ      ENDY
        MVI     A,40H   ;RESET SERIAL I/O.
        OUT     0EDH
        LXI     H,38FFH ;RESET RAM ADC & CODE AREA (38FF-3907)
ZERO:   MVI     A,00H
        MOV     M,A
        INX     H
        MOV     A,L
        CPI     08H
        JNZ     ZERO
        JMP     RECST   ;RETURN TO START.
SPSR:   MVI     A,0FFH  ;ESTABLISH SP-1 MUX ADDRESS.
        OUT     0E6H    ;ADDRESS 00=FF DUE TO INVERSION.
        CALL    STROB   ;STROBE ADC.
        NOP             ;DELAY 5-6 USEC.
        NOP
        NOP
        IN      0E5H    ;INPUT SP-1 MS BYTE.
        STA     3900H   ;STORE AT ADC1 MS BYTE.
        IN      0E4H    ;INPUT SP-1 LS BYTE.
        CMA             ;COMPLIMENT DUE TO PORT TYPE.
        STA     3901H   ;STORE AT ADC1 LS BYTE.
        RET             ;THIS SELECTS ONLY 1 SP CHANNEL REMOVE FOR ALL.
        MVI     A,0FEH  ;ESTABLISH SP-2 MUX ADDRESS.
        OUT     0E6H
        CALL    STROB   ;STROBE ADC.
        NOP             ;DELAY 5-6 USEC.
        NOP
        NOP
```

```
        IN      0E5H    ;INPUT SP-2 MS BYTE.
        STA     3902H   ;STORE AT ADC2 MS BYTE.
        IN      0E4H    ;INPUT SP-2 LS BYTE.
        CMA             ;COMPLIMENT DUE TO PORT TYPE.
        STA     3903H   ;STORE AT ADC2 LS BYTE.
        MVI     A,0FDH  ;ESTABLISH SP-3 MUX ADDRESS.
        OUT     0E6H
        CALL    STROB   ;STROBE ADC.
        NOP             ;DELAY 5-6 USEC.
        NOP
        NOP
        IN      0E5H    ;INPUT SP-3 MS BYTE.
        STA     3904H   ;STORE AT ADC3 MS BYTE.
        IN      0E4H    ;INPUT SP-3 LS BYTE.
        CMA             ;COMPLIMENT DUE TO PORT TYPE.
        STA     3905H   ;STORE AT ADC3 LS BYTE.
        RET
IPSR:   MVI     A,0FCH  ;ESTABLISH IP-1 MUX ADDRESS.
        OUT     0E6H    ;ADDRESS 03=FC DUE TO INVERSION.
        CALL    STROB   ;STROBE ADC.
        NOP             ;DELAY 5-6 USEC.
        NOP
        NOP
        IN      0E5H    ;INPUT IP-1 MS BYTE.
        STA     3902H   ;STORE AT ADC2 MS BYTE.
        IN      0E4H    ;INPUT IP-1 LS BYTE.
        CMA             ;COMPLIMENT DUE TO PORT TYPE.
        STA     3903H   ;STORE AT ADC2 LS BYTE.
        MVI     A,0FBH  ;ESTABLISH IP-2 MUX ADDRESS.
        OUT     0E6H
        CALL    STROB   ;STROBE ADC.
        NOP             ;DELAY 5-6 USEC.
        NOP
        NOP
        IN      0E5H    ;INPUT IP-2 MS BYTE.
        STA     3904H   ;STORE AT ADC3 MS BYTE.
        IN      0E4H    ;INPUT IP-2 LS BYTE.
        CMA             ;COMPLIMENT DUE TO PORT TYPE.
        STA     3905H   ;STORE AT ADC3 LS BYTE.
        MVI     A,0FAH  ;ESTABLISH IP-3 MUX ADDRESS.
        OUT     0E6H
        CALL    STROB   ;STROBE ADC.
        NOP             ;DELAY 5-6 USEC.
        NOP
        NOP
        IN      0E5H    ;INPUT IP-3 MS BYTE.
        STA     3906H   ;STORE AT ADC4 MS BYTE.
        IN      0E4H    ;INPUT IP-3 LS BYTE.
        CMA             ;COMPLIMENT DUE TO PORT TYPE.
        STA     3907H   ;STORE AT ADC4 LS BYTE.
        RET
LPSR:   MVI     A,0F9H  ;ESTABLISH LP-1 MUX ADDRESS.
        OUT     0E6H    ;ADDRESS 00=FF DUE TO INVERSION.
```

```
        CALL    STROB   ;STROBE ADC.
        NOP             ;DELAY 5-6 USEC.
        NOP
        NOP
        IN      0E5H    ;INPUT LP-1 MS BYTE.
        STA     3902H   ;STORE AT ADC2 MS BYTE.
        IN      0E4H    ;INPUT LP-1 LS BYTE.
        CMA             ;COMPLIMENT DUE TO PORT TYPE.
        STA     3903H   ;STORE AT ADC2 LS BYTE.
        MVI     A,0F8H  ;ESTABLISH LP-2 MUX ADDRESS.
        OUT     0E6H
        CALL    STROB   ;STROBE ADC.
        NOP             ;DELAY 5-6 USEC.
        NOP
        NOP
        IN      0E5H    ;INPUT LP-2 MS BYTE.
        STA     3904H   ;STORE AT ADC3 MS BYTE.
        IN      0E4H    ;INPUT LP-2 LS BYTE.
        CMA             ;COMPLIMENT DUE TO PORT TYPE.
        STA     3905H   ;STORE AT ADC3 LS BYTE.
        MVI     A,0F7H  ;ESTABLISH LP-3 MUX ADDRESS.
        OUT     0E6H
        CALL    STROB   ;STROBE ADC.
        NOP             ;DELAY 5-6 USEC.
        NOP
        NOP
        IN      0E5H    ;INPUT LP-3 MS BYTE.
        STA     3906H   ;STORE AT ADC4 MS BYTE.
        IN      0E4H    ;INPUT LP-3 LS BYTE.
        CMA             ;COMPLIMENT DUE TO PORT TYPE.
        STA     3907H   ;STORE AT ADC4 LS BYTE.
        RET
STROB:  MVI     A,08H   ;BIT 0 RESET AND INVERTED = 1.
        OUT     0E7H
        MVI     A,09H   ;BIT 0 RESET AND INVERTED = 0.
        OUT     0E7H
        RET
LASTA:  JMP     RECST
LASTB:  JMP     RECST
LASTC:  JMP     RECST
        END
```

APPENDIX A.5

8080 PROGRAM LISTING
MICROPROCESSOR SIX

```
PUBLIC  INITRC
                        ;JANUARY 30, 1982
                        ;THIS PROGRAM IS THE 80/05 TAPE-WRITE PROGRAM
                        ;FOR THE DRS TELEMETRY SYSTEM.  IT WILL WORK
                        ;ON THE DRS SYTEMS IF THE "SWITCH" LOCATIONS
                        ;ARE CHANGED.


INITRC: NOP
        DI              ;DISABLE INTERRUPTS
        LXI     SP,3FE0H;LOAD STACK POINTER WITH STACK LOCATION
        MVI     A,07H   ;PROGRAM THE THREE PORTS VIA THE
        OUT     00H     ;CONTROL PORT 00
        CALL    RESET1
        CALL    DEL1MS
        LXI     H,0000H ;ZERO OUT RECORD AND FLAG COUNTERS
        SHLD    3E00H   ;SET RECORD COUNTER FLAG = 00
        SHLD    3E02H   ;SET MSB RECORD COUNTER #1 = 00
START1: CALL    SWOPN   ;WAIT FOR THE KEY SWITCH TO CLOSE.
DELAYF: CALL    DEL1MS
        CALL    SWCL    ;WAIT FOR THE KEY SWITCH TO OPEN
        CALL    DL1SEC
        CALL    RESET1
        CALL    RPNTRS
        CALL    CK8005
ZERO2:  MVI     A,0FFH  ;TURN OFF ALARM
        STA     0FE96H
        LXI     H,0000H ;ZERO OUT RECORD AND FLAG COUNTERS
        SHLD    3E00H
        SHLD    3E02H
RECYCL: IN      0F6H    ;CHECK ALARM RESET BUTTON IF IT
        ANI     0FH     ;IS PUSHED IN, RESET THE COUNTER AND
                        ;TURN OFF THE ALARM
        CPI     0DH
        JNZ     CHCKSL
        MVI     A,00H
        STA     3E01H   ;SET RECORD 100 COUNT = 00.
        MVI     A,0FFH
        STA     0FE96H  ;TURN ALARM OFF.
CHCKSL: IN      0F6H    ;IS  MASTER SWITCH ACTIVATED?
        ANI     0FH
        CPI     0BH
        JNZ     CHCKWR
        JMP     DELAYF
RPNTRS: LXI     H,0000H ;SET LP RECORD DATA POINTER = 00
        SHLD    0FE86H
        SHLD    0FE88H  ;SET SP RECORD DATA POINTER#1 =00
        SHLD    0FE8AH  ;SET SP RECORD DATA POINTER#2 =00
        SHLD    0FE8CH  ;     "     "       "      "   #3 =00
        SHLD    0FE8EH  ;    WB     "       "      "   #1 =00
        SHLD    0FE90H  ;     "     "       "      "   #2 =00
        SHLD    0FE92H  ;     "     "       "      "   #3 =00
```

```
        MVI     A,00H    ;SET 8005 FLAG = --
        STA     0FE94H
        RET
CK8005: LDA     0FE94H   ;CHECK 80/05 FLAG IF = 1 RETURN, IF
                         ; = 0 CONTINUE TO CHECK
        RAR
        JNC     CK8005
        RET
CHCKWR: LHLD    0FE86H   ;CHECK THE ADDRESS OF THE LONG PERIOD
                         ;RECORD POINTER.  IF IT IS = 0 JUMP TO SHORT
                         ;PERIOD CHECKS.
        XCHG
        LXI     H,0000H ;ZERO LP MAILBOX.
        SHLD    0FE86H
LP1T:   MOV     A,D
        CPI     0F6H     ;TEST FOR MSBYTE LP RECORD #1.
        JNZ     LP2T
        MOV     A,E
        CPI     0B0H     ;TEST FOR LSBYTE LP RECORD #1
        JNZ     LP2T
        LXI     H,0EEE0H;WRITE LP RECORD #1.
        CALL    PLSRST
        JMP     SP1
LP2T:   MOV     A,D
        CPI     0FEH     ;TEST FOR MSBYTE LP RECORD #2.
        JNZ     SP1
        MOV     A,E
        CPI     80H      ;TEST FOR LSBYTE LP RECORD #2.
        JNZ     SP1
        LXI     H,0F6B0H;WRITE LP RECORD #2.
        CALL    PLSRST
        JMP     SP2
SP1:    LHLD    0FE88H   ;CHECK THE ADDRESS OF SP #1 RECORD POINTER.
                         ;IF = 0 JUMP TO SP #2 CHECKS.
        XCHG
        LXI     H,0000H ;ZERO SP #1 MAILBOX.
        SHLD    0FE88H
        MOV     A,D
        CPI     0C7H     ;TEST FOR MSBYTE SP RECORD #1.
        JNZ     SP12
        MOV     A,E
        CPI     0D0H     ;TEST FOR LSBYTE SP RECORD #1.
        JNZ     SP12
        LXI     H,0C000H;WRITE SP RECORD #1.
        CALL    PLSRST
        JMP     SP2
SP12:   MOV     A,D      ;PERFORM THE SAME CHECK ON SP RECORD
                         ;POINTER #2 AS WITH SP RECORD POINTER #1
        CPI     0CFH     ;TEST FOR MSBYTE SP RECORD #2.
        JNZ     SP13
        MOV     A,E
        CPI     0A0H     ;TEST FOR LSBYTE SP RECORD #2.
        JNZ     SP13
```

```
        LXI     H,0C7D0H;WRITE SP RECORD #2.
        CALL    PLSRST
        JMP     SP2
SP13:   MOV     A,D     ;PERFORM SAME CHECK ON SP RECORD POINTER  #3
                        ;AS WITH SP RECORD POINTER #1
        CPI     0D7H    ;TEST FOR MSBYTE SP RECORD #3.
        JNZ     SP2
        MOV     A,E
        CPI     70H     ;TEST FOR LSBYTE SP RECORD #3.
        JNZ     SP2
        LXI     H,0CFA0H;WRITE SP RECORD #3.
        CALL    PLSRST
SP2:    LHLD    0FE8AH  ;LOAD SP MAILBOX #2.
        XCHG
        LXI     H,0000H
        SHLD    0FE8AH  ;ZERO SP MAILBOX #2.
        MOV     A,D
        CPI     0C7H    ;TEST FOR MSBYTE SP RECORD #1
        JNZ     SP22
        MOV     A,E     ;TEST FOR LSBYTE SP RECORD #1
        CPI     0D0H
        JNZ     SP22
        LXI     H,0C000H;WRITE SP RECORD #1.
        CALL    PLSRST
        JMP     IP1
SP22:   MOV     A,D     ;TEST FOR MSBYTE SP RECORD #2.
        CPI     0CFH
        JNZ     SP23
        MOV     A,E     ;TEST FOR LSBYTE SP RECORD #2.
        CPI     0A0H
        JNZ     SP23
        LXI     H,0C7D0H;WRITE SP RECORD #2.
        CALL    PLSRST
        JMP     IP1
SP23:   MOV     A,D     ;TEST FOR MSBYTE SP RECORD #3.
        CPI     0D7H
        JNZ     IP1
        MOV     A,E     ;TEST FOR LSBYTE SP RECORD #3.
        CPI     70H
        JNZ     IP1
        LXI     H,0CFA0H;WRITE SP RECORD #3.
        CALL    PLSRST
IP1:    LHLD    0FE8EH  ;CHECK THE ADDRESS OF THE WB RECORD POINTER #1.
                        ;IF IT IS = 0, JUMP TO WB #2 CHECK.
        XCHG
        LXI     H,0000H ;ZERO IP MAILBOX #1.
        SHLD    0FE8EH
        MOV     A,D     ;TEST MSBYTE IP RECORD #1.
        CPI     0DFH
        JNZ     IP12
        MOV     A,E     ;TEST LSBYTE IP RECORD #1.
        CPI     40H
        JNZ     IP12
```

```
        LXI     H,0D770H;WRITE IP RECORD #1.
        CALL    PLSRST
        JMP     IP2
IP12:   MOV     A,D     ;PERFORM SAME CHECK ON IP RECORD #2
        CPI     0E7H    ;TEST MSBYTE IP RECORD #2.
        JNZ     IP13
        MOV     A,E     ;TEST LSBYTE IP RECORD #2.
        CPI     10H
        JNZ     IP13
        LXI     H,0DF40H;WRITE IP RECORD #2.
        CALL    PLSRST
        JMP     IP2
IP13:   MOV     A,D     ;TEST MSBYTE IP RECORD #3.
        CPI     0EEH
        JNZ     IP2
        MOV     A,E     ;TEST LSBYTE IP RECORD #3.
        CPI     0E0H
        JNZ     IP2
        LXI     H,0E710H;WRITE IP RECORD #3.
        CALL    PLSRST
IP2:    LHLD    0FE90H  ;LOAD IP MAILBOX #2.
        XCHG
        LXI     H,0000H ;ZERO IP MAILBOX #2.
        SHLD    0FE90H
        MOV     A,D     ;TEST FOR MSBYTE IP RECORD #1.
        CPI     0DFH
        JNZ     IP22
        MOV     A,E     ;TEST FOR LSBYTE IP RECORD #1.
        CPI     40H
        JNZ     IP22
        LXI     H,0D770H;WRITE IP RECORD #1.
        CALL    PLSRST
        JMP     END
IP22:   MOV     A,D     ;TEST FOR MSBYTE IP RECORD #2.
        CPI     0E7H
        JNZ     IP23
        MOV     A,E     ;TEST FOR LSBYTE IP RECORD #2.
        CPI     10H
        JNZ     IP23
        LXI     H,0DF40H;WRITE IP RECORD #2.
        CALL    PLSRST
        JMP     END
IP23:   MOV     A,D     ;TEST FOR MSBYTE IP RECORD #3.
        CPI     0EEH
        JNZ     END
        MOV     A,E     ;TEST FOR LSBYTE IP RECORD #3.
        CPI     0E0H
        JNZ     END
        LXI     H,0E710H;WRITE IP RECORD #3.
        CALL    PLSRST
END:    NOP
RETURN: CALL    DEL1MS
        CALL    RESET1
```

```
        JMP     ISDSWF
PLSRST: MVI     A,20H   ;PROVIDE RESET PULSE TO THE TAPE FORMATER
                        ;20 = 04 (WITH DATA LINE 0-7 REVERSED)
                        ;0000 0100 = 04H IS EQUAL TO 1600 BPI
                        ;0010 0000 = 20H
        OUT     01H
        MVI     A,20H   ;DEVICE ENABLE
        OUT     02H
        MVI     A,28H   ;DEVICE ENABLE & RESET
        OUT     02H
        MVI     A,20H   ;DEVICE ENABLE
        OUT     02H
        MVI     A,00H   ;ENABLE TRISTATE BUFFER
        OUT     03H
        MVI     D,02H   ; *  SET UP WRITE PULSE DATA INFO IN REG D.
                        ;(THIS WILL ENABLE THE PROCESSOR TO DETERMINE
                        ;WHEN A WRITE PULSE HAS BEEN RECEIVED)
        MVI     B,32H
        MVI     C,32H   ;LOAD REG C,B WITH BLOCK LENGTH INFO (THIS
                        ;WILL ENABLE THE PROGRAM TO COUNT THE CORRECT
                        ;LENGTH OF THE BLOCK
        MVI     E,00H   ;LOAD REG E WITH THE INITIAL SAMPLE WAIT COUNT
        MVI     A,22H   ;(44->22 DUE TO DATA LINE 0 - 7 REVERSAL
                        ;STROBE CONVERT LINE WITH WRITE 1BLOCK
                        ;INFORMATION.
        OUT     01H
        MVI     A,00H   ;STORE 00 IN DELAY COUNTER
        STA     3E05H
        MVI     A,0A0H  ;SET SET RECORDER FORMATTER WITH
                        ;(CONTROLCOMMAND + DEVICE ENABLE)
        OUT     02H
        MVI     A,20H   ;SET RECORDER FORMATTER WITH(DEVICE ENABLE)
        OUT     02
        MOV     A,M     ;MOVE DATA TO TRANSFER PORT
        INX     H       ;INCREMENT DATA POINTER
        OUT     01H
IN1:    IN      00H
        ANA     D
        JZ      END1
        INR     E       ;INCREMENT REG E IF NOT 00 JUMP TO IN1
        JNZ     IN1
        LDA     3E05H   ;INCREMENT DELAY COUNTER
        INR     A
        STA     3E05H
        JNZ     IN1     ;IF DELAY COUNTER NOT = 00 JUMP TO IN1
        JMP     RESDEL
END1:   MOV     A,M
        OUT     01H
HERE1S: MOV     E,D
SHOT1:  IN      00H     ;RESET COUNTER (KIKOUT) INPUT WRITE PULSE DATA
        ANA     D       ;UNTIL PULSE HAS BEEN RECEIVED OR TIME HAS EXPIRED
        JZ      END1SH  ;WHEN THE PULSE HAS BEEN RECEIVED INCREMENT
                        ;THE 256 COUNTER .  WHEN THE COUNT IS REACHED
```

```
                                ;MOVE TO 2nd SHOT HERE
          INR       E
          JNZ       SHOT1
          JMP       RESDEL
END1SH:   INX       H
          MOV       A,M
          OUT       01H
          INR       C
          JNZ       HERE1S
HERE2S:   MOV       E,D       ;REFER TO 1stSHOT HERE(HERE1S)FOR DETAILS
SHOT2:    IN        00H
          ANA       D
          JZ        END2SH
          INR       E
          JNZ       SHOT2
          JMP       RESDEL
END2SH:   INX       H
          MOV       A,M
          OUT       01H
          INR       C
          JNZ       HERE2S
HERE3S:   MOV       E,D       ;REFER TO 1stSHOT HERE FOR DETAILS
SHOT3:    IN        00H
          ANA       D
          JZ        END3SH
          INR       E
          JNZ       SHOT3
          JMP       RESDEL
END3SH:   INX       H
          MOV       A,M
          OUT       01H
          INR       C
          JNZ       HERE3S
HERE4S:   MOV       E,D
SHOT4:    IN        00H
          ANA       D
          JZ        END4SH
          INR       E
          JNZ       SHOT4
          JMP       RESDEL
END4SH:   INX       H
          MOV       A,M
          OUT       01H
          INR       C
          JNZ       HERE4S
HERE5S:   MOV       E,D
SHOT5:    IN        00H
          ANA       D
          JZ        END5SH
          INR       E
          JNZ       SHOT5
          JMP       RESDEL
END5SH:   INX       H
```

```
          MOV     A,M
          OUT     01H
          INR     C
          JNZ     HERE5S
HERE6S:   MOV     E,D
SHOT6:    IN      00H
          ANA     D
          JZ      END6SH
          INR     E
          JNZ     SHOT6
          JMP     RESDEL
END6SH:   INX     H
          MOV     A,M
          OUT     01H
          INR     C
          JNZ     HERE6S
HERE7S:   MOV     E,D
SHOT7:    IN      00H
          ANA     D
          JZ      END7SH
          INR     E
          JNZ     SHOT7
          JMP     RESDEL
END7SH:   INX     H
          MOV     A,M
          OUT     01H
          INR     C
          JNZ     HERE7S
HERE8S:   MOV     E,D
SHOT8:    IN      00H
          ANA     D
          JZ      END8SH
          INR     E
          JNZ     SHOT8
          JMP     RESDEL
END8SH:   INX     H
          MOV     A,M
          OUT     01H
          INR     C
          JNZ     HERE8S
HERE9S:   MOV     E,D
SHOT9:    IN      00H
          ANA     D
          JZ      END9SH
          INR     E
          JNZ     SHOT9
          JMP     RESDEL
END9SH:   MVI     A,0FFH  ;TURN TRI-STATE MIRRORING DEVICE OFF
          OUT     03H
          MVI     A,20H   ;LOAD RESET INFO ON PORT 1
          OUT     01H     ;0C HEX = 20 DATA LINES 0 -7 INVERTED
          MVI     A,00H   ;DELAY TO ALLOW TIME FOR TAPE TO STOP
          MVI     B,00H
```

```
        MVI     C,0FDH
DELNOW: INR     A
        JNZ     DELNOW
        INR     B
        JNZ     DELNOW
        INR     C
        JNZ     DELNOW
        MVI     A,00H   ;ENABLE TRI-STATE MIRRORING DEVICES
        OUT     03H
        CALL    DL1SEC
        LDA     3E00H   ;DETERMINE WHICH COUNTER TO USE
                        ;GOOD BLOCK 100 BLOCK
        ANA     A
        JNZ     INCCN2
        LDA     3E02H   ;INCREMENT 6000 COUNTER
        INR     A
        STA     3E02H
        JNZ     CNR1RT
        LDA     3E03H
        INR     A
        STA     3E03H
        CPI     18H
        JNZ     CNR1RT
        MVI     A,00H
        OUT     0F6H
        MVI     A,0FFH
        STA     3E00H
CNR1RT: RET
INCCN2: LDA     3E01H   ;INCREMENT 100 COUNTER
        INR     A
        STA     3E01H
        CPI     64H
        JNZ     CNR2RT
        MVI     A,00H
        OUT     0F6H
        MVI     A,00H
        STA     3E01H
CNR2RT: RET
DL1SEC: MVI     A,00H
        MVI     B,00H
        MVI     C,0FDH
INCA:   INR     A
        JNZ     INCA
        INR     B
        JNZ     INCA
        INR     C
        JNZ     INCA
        RET
RESET1: MVI     A,0FFH  ;DISABLE TRI-STATE MIRRORING AND RESET TAPE FORMAT
        OUT     03H
        MVI     A,20H   ;0C = 20 DUE TO 0 -7 LINE REVERSAL
        OUT     01H
        MVI     A,20H
```

```
        OUT     02
        MVI     A,28H
        OUT     02
        MVI     A,20H
        OUT     02H
        RET
DEL1MS: MVI     A,00H
MS1:    INR     A
        JNZ     MS1
        RET
RESDEL: MVI     A,00H       ;TURN ALARM ON
        STA     0FE96H
        CALL    RESET1      ;RESET FORMATTER
        CALL    DL1SEC      ;DELAY 1 SEC
        MVI     A,0FFH      ;TURN ALARM OFF
        STA     0FE96H
ISDSWF: IN      0F6H        ;IS MASTER KEY SWITCH CLOSED? IF NOT JUMP.
        ANI     0FH
        CPI     0BH
        JNZ     RECYCLE
        IN      0F5H        ;IS DSWITCH = 14 (E)? IF NOT JUMP,
        CMA                 ;DATA IS INVERTED, SO COMPLIMENT.
        ANI     0F0H        ;IF SO WRITE EOT.   MASK OUT C SWITCH.
        CPI     0E0H
        JNZ     RECYCLE
        MVI     A,21H       ;D SWITCH WAS 14.
        OUT     01H         ;WRITE AN EOF ON THE TAPE.
        MVI     A,20H       ;STROBE CONTROL COMMAND AND DEVICE ENABLE
                            ;LINES TO ENTER EOF COMMAND
        OUT     02H
        MVI     A,0A0H
        OUT     02H
        MVI     A,20H
        OUT     02H
        JMP     RECYCLE
SWOPN:  IN      0F6H        ;READ MASTER KEY, IS SWITCH OPEN? STAY HERE
        ANI     0FH
        CPI     0FH         ;UNTIL IT IS OPENED.
        JNZ     SWOPN
        RET
SWCL:   IN      0F6H        ;READ MASTER KEY, IS SWITCH CLOSED? STAY HERE
        ANI     0FH
        CPI     0BH         ;UNTILL IT IS CLOSED.
        JZ      SWCL
        RET
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
```

```
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
LXI     H,0AA77H;IF 80/05 PROGRAM EVER GOES WILD THIS SECTION
                ;WILL FLAG MEMORY THAT THE PROGRAM GOT HERE
                ;AND IT SHOULD RETURN TO THE START OF PROGRAM
SHLD    0FE98H
JMP     ZER02
END
```

APPENDIX B.1

2716 EPROM LISTING
MICROPROCESSOR ONE

```
STARPLEX PROM Programmer utility  Version 1.0

PROM type 2716   PAGE NUMBER: 0001

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F        0123456789ABCD
0000    00 F3 C3 2F 00 00 00 C3 64 01 00 00 00 00 00 00      |   /     d
0010    00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00      |
0020    00 00 00 00 00 00 00 00 00 00 00 00 C3 65 01 31      |                e
0030    E0 39 21 FF 2F 23 3E 00 77 7C FE 3F C2 35 00 7D      | 9! /#> wl ? 5
0040    FE FF C2 35 00 21 FF BF 23 3E 00 77 7C FE FF C2      |   5 !  #> wl
0050    48 00 7D FE FF C2 48 00 3E 80 D3 E7 3E 92 D3 EB      |H }    H >    >
0060    3E 07 D3 E4 3E 93 D3 F7 3E 9B D3 FB 3E FF D3 EA      |>   >   >   >
0070    3E 00 32 71 38 32 FD 38 32 FE 38 32 94 FE 3E 01      |> 2q82 82 82
0080    32 62 38 21 B0 F6 22 3A 38 21 D0 C7 22 32 38 21      |2b8!  ":8!  "2
0090    40 DF 22 36 38 DB F6 E6 0F FE 0B C2 95 00 C3 FC      |@ "68
00A0    00 3E 93 D3 F7 DB F6 E6 0F FE 0E C2 B4 00 CD 42      | >
00B0    05 C3 B9 00 3E 00 32 64 38 DB F4 E6 0F 32 63 38      |    > 2d8    2
00C0    21 2C 38 96 C2 DC 00 3A 96 FE A7 CA D5 00 3E B0      |!,8    :
00D0    D3 F6 C3 EE 00 3E 80 D3 F6 C3 EE 00 3A 96 FE A7      |     >       :
00E0    C2 EA 00 3E 40 D3 F6 C3 EE 00 3E 70 D3 F6 3E FF      |   >@      >p
00F0    32 94 FE DB F6 E6 0F FE 0B C2 65 01 DB F4 1F 1F      |2          e

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F        0123456789ABCD
0100    1F 1F E6 0F 32 10 38 DB F5 2F 47 E6 0F 32 11 38      |    2 8  /G  2
0110    78 1F 1F 1F 1F E6 0F 32 12 38 3E 00 32 14 38 32      |x       2 8> 2
0120    70 38 32 03 38 32 28 3F 32 D9 0E 32 34 38 32 38      |p82 82(?2  248
0130    38 3E FF 32 06 38 21 00 3A 11 00 00 72 23 3E 3F      |8> 2 8! :    r#
0140    BC C2 3C 01 21 70 3F 11 00 00 72 23 3E 9F BD C2      |  < !p?    r#>
0150    4A 01 3E 80 D3 ED 3E 00 D3 ED 3E 40 D3 ED C3 D8      |J >   >   >@
0160    0B C3 0C 20 00 DB E9 E6 01 CA 65 01 DB E9 E6 01      |               e
0170    CA 6C 01 DB E9 E6 01 CA 6C 01 2A 32 38 7C FE D7      | 1       1 *28|
0180    C2 95 01 7D FE 70 DA BB 01 21 70 D7 22 32 38 CD      |   } p   !p "2
0190    99 07 C3 BB 01 2A 32 38 7C FE C7 C2 AA 01 7D FE      |      *28|
01A0    D0 C2 BB 01 CD 99 07 C3 BB 01 2A 32 38 FE CF C2      |               *28
01B0    BB 01 7D FE A0 C2 BB 01 CD 99 07 3A 62 38 FE 01      |  }          :b8
01C0    CA 90 02 FE 02 CA 41 02 FE 03 CA 33 02 FE 04 CA      |       A     3
01D0    41 02 FE 05 CA 25 02 FE 06 CA 41 02 FE 07 CA 33      |A    %    A
01E0    02 FE 08 CA 41 02 FE 09 CA 25 02 FE 0A CA 41 02      |    A    %
```

```
01F0    FE 0B CA 33 02 FE 0C CA 41 02 FE 0D CA 25 02 FE      |   3    A    %

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F       0123456789ABCD
0200    0E CA 41 02 FE 0F CA 33 02 FE 10 CA 41 02 FE 11      |  A    3    A
0210    CA 25 02 FE 12 CA 41 02 FE 13 CA 33 02 3E 00 32      | %    A    3 >
0220    62 38 C3 41 02 3E 13 32 65 38 3A 63 38 32 66 38      |b8 A > 2e8: c82
0230    C3 BE 02 3E 12 32 65 38 3A 64 38 32 66 38 C3 BE      |   > 2e8: d82f8
0240    02 2A 36 38 7C FE EE C2 5C 02 7D FE E0 DA 83 02      | *68|   \ }
0250    21 E0 EE 22 36 38 CD B3 08 C3 83 02 2A 36 38 7C      |!  "68      *6
0260    FE DF C2 71 02 7D FE 40 C2 83 02 CD B3 08 C3 83      |   q } @
0270    02 2A 36 38 7C FE E7 C2 83 02 7D FE 10 C2 83 02      | *68|     }
0280    CD B3 08 3E 11 32 65 38 3E 00 32 66 38 C3 BE 02      |   > 2e8> 2f8
0290    2A 3A 38 7C FE FE C2 A5 02 7D FE 80 DA B4 02 CD      |*:8|      }
02A0    D9 09 C3 B4 02 7C FE F6 C2 B4 02 7D FE B0 C2 B4      |      |     }
02B0    02 CD CD 09 3E 10 32 65 38 3E 00 32 66 38 3E 00      |    > 2e8> 2f8
02C0    D3 ED D3 ED D3 ED 3E 40 D3 ED 3E 1C D3 ED 3E AA      |       >@  >
02D0    D3 ED 3E AA D3 ED 3E 33 D3 ED DB ED E6 01 CA DA      |  >    >3
02E0    02 3E AA D3 EC DB ED E6 01 CA E5 02 3E AA D3 EC      | >           >
02F0    DB ED E6 01 CA F0 02 3A 65 38 D3 EC DB ED E6 01      |        :e8

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F       0123456789ABCD
0300    CA FC 02 3A 66 38 D3 EC DB ED E6 01 CA 08 03 3E      |   :f8
0310    00 D3 EC DB ED E6 01 CA 13 03 3E FF D3 EC DB ED      |          >
0320    E6 01 CA 1E 03 3E 00 D3 EC DB ED E6 01 CA 29 03      |     >
0330    3E 40 D3 ED 3A 62 38 3C 32 62 38 21 00 FF 7E 32      |>@  :b8<2b8!
0340    FF 38 32 70 38 23 7E 32 00 39 23 7E 32 01 39 23      | 82p8#~2 9#~2
0350    7E 32 02 39 23 7E 32 03 39 23 7E 32 04 39 23 7E      |~2 9#~2 9#~2 9
0360    32 05 39 23 7E 32 06 39 23 7E 32 07 39 3A FF 38      |2 9#~2 9#~2 9:
0370    FE 10 CA 3E 03 FE 11 CA 97 03 FE 12 CA A0 03 FE      |
0380    13 CA B3 03 3A 2A 38 3C 32 2A 38 C3 BC 03 CD 08      |     :*8<2*8
0390    04 CD 88 04 C3 BC 03 CD 08 04 CD 29 04 C3 BC 03      |           )
03A0    CD 08 04 3A 02 39 2F 32 30 38 3A 03 39 32 29 38      |   : 9/208: 92
03B0    C3 BC 03 CD 08 04 3A 02 39 32 2C 38 21 70 38 3A      |      : 92,8!p
03C0    71 38 96 CA CD 03 3A 2B 38 3C 32 2B 38 3A 71 38      |q8     :+8<2+8:
03D0    FE 10 C2 DB 03 CD 1D 05 C3 E6 03 3A 71 38 FE 11      |           :q8
03E0    C2 E6 03 CD F8 04 CD E7 04 3A 65 38 32 71 38 3A      |         :e82q
```

```
03F0    3B 38 FE FE C2 05 04 3A 3A 38 FE 80 DA 05 04 21      ;8      ::8

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F       0123456789ABCD
0400    80 FE 22 3A 39 C3 4E 0A 3A 00 39 17 2F 1F D3 E5      "  :9 N  :  9 /
0410    3A 01 39 2F D3 E6 3E 87 D3 E4 3E 47 D3 E4 3E 07      : 9/  >    >G
0420    D3 E4 3E 0F D3 E4 3E 07 C9 3A 02 39 17 2F 1F D3      >    >  :  9 /
0430    E5 3A 03 39 2F D3 E6 3E 87 D3 E4 3E 47 D3 E4 3E      : 9/  >    >G
0440    04 D3 E4 3E 0C D3 E4 3A 04 39 17 2F 1F D3 E5 3A      >    :  9 /
0450    05 39 2F D3 E6 3E 87 D3 E4 3E 47 D3 E4 3E 03 D3      9/  >    >G  >
0460    E4 3E 0B D3 E4 3A 06 39 17 2F 1F D3 E5 3A 07 39      >    :  9 /    :
0470    2F D3 E6 3E 87 D3 E4 3E 47 D3 E4 3E 02 D3 E4 3E     /  >    >G  >
0480    1A D3 E4 3E 07 D3 E4 C9 3A 02 39 17 2F 1F D3 E5      >      :  9 /
0490    3A 03 39 2F D3 E6 3E 87 D3 E4 3E 47 D3 E4 3E 01      : 9/  >    >G
04A0    D3 E4 3E 09 D3 E4 3A 04 39 17 2F 1F D3 E5 3A 05      >    :  9 /
04B0    39 2F D3 E6 3E 87 D3 E4 3E 47 D3 E4 3E 00 D3 E4     9/  >    >G  >
04C0    3E 08 D3 E4 3A 06 39 17 2F 1F D3 E5 3A 07 39 2F     >    :  9 /    :
04D0    D3 E6 3E 87 D3 E4 3E 47 D3 E4 3E 07 D3 E4 3E 17      >    >G  >
04E0    D3 E4 3E 07 D3 E4 C9 2A 32 38 3A 00 39 77 23 3A      >     *28:  9w
04F0    01 39 77 23 22 32 38 C9 2A 36 38 3A 02 39 77 23     9w#"28 *68:  9

ADDR    0, 1  2  3  4  5  6  7  8  9  A  B  C  D  E  F       0123456789ABCD
0500    3A 03 39 77 23 3A 04 39 77 23 3A 05 39 77 23 3A      : 9w#:  9w#:  9w
0510    06 39 77 23 3A 07 39 77 23 22 36 38 C9 2A 3A 38     9w#:  9w#"68 *
0520    3A 02 39 77 23 3A 03 39 77 23 3A 04 39 77 23 3A      : 9w#:  9w#:  9w
0530    05 39 77 23 3A 06 39 77 23 3A 07 39 77 23 22 3A     9w#:  9w#:  9w#
0540    38 C9 DB F8 E6 0F 47 78 FE 00 CA 93 05 FE 01 CA     8       Gx
0550    99 05 FE 02 CA E0 05 FE 03 CA 54 06 FE 04 CA 14                T
0560    06 FE 05 CA 9C 06 FE 06 CA 96 06 FE 07 CA 90 06
0570    FE 08 CA A2 06 FE 09 CA 93 05 FE 0A CA 93 05 FE
0580    0B CA E2 06 FE 0C CA E8 06 FE 0D CA EE 06 FE 0E
0590    CA F4 06 3E E0 32 64 38 C9 DB FA 2F E6 0F FE 00        > 2d8    /
05A0    CA 93 05 FE 01 CA DA 05 FE 02 CA D4 05 FE 03 CA
05B0    CE 05 FE 04 CA C8 05 FE 05 CA C2 05 3E 20 32 64                 >
05C0    38 C9 3E 21 32 64 38 C9 3E 22 32 64 38 C9 3E 23     8 >!2d8 >"2d8
05D0    32 64 38 C9 3E 24 32 64 38 C9 3E 25 32 64 38 C9     2d8 >$2d8 >%2
05E0    DB F8 1F 1F 1F 1F E6 0F FE 00 CA 93 05 FE 01 CA
```

```
05F0    0E 06 FE 02 CA 08 06 FE 03 CA 02 06 3E 80 32 64      |              >

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F       0123456789ABCD
0600    38 C9 3E 81 32 64 38 C9 3E 82 32 64 38 C9 3E 83      |8 > 2d8 > 2d8
0610    32 64 38 C9 DB FA 2F 1F 1F 1F 1F E6 0F FE 00 CA      |2d8   /
0620    93 05 FE 01 CA 4E 06 FE 02 CA 48 06 FE 03 CA 42      |      N     H
0630    06 FE 04 CA 3C 06 3E 84 32 64 38 C9 3E 85 32 64      |     < > 2d8 >
0640    38 C9 3E 86 32 64 38 C9 3E 87 32 64 38 C9 3E 88      |8 > 2d8 > 2d8
0650    32 64 38 C9 DB F9 2F E6 0F FE 00 CA 93 05 FE 01      |2d8   /
0660    CA 8A 06 FE 02 CA 84 06 FE 03 CA 7E 06 FE 04 CA      |              ~
0670    78 06 3E 2A 32 64 38 C9 3E 29 32 64 38 C9 3E 28      |x >*2d8 >)2d8
0680    32 64 38 C9 3E 27 32 64 38 C9 3E 26 32 64 38 C9      |2d8 >'2d8 >&2d
0690    3E 40 32 64 38 C9 3E 89 32 64 38 C9 3E 4B 32 64      |>@2d8 > 2d8 >K
06A0    38 C9 DB F9 2F 1F 1F 1F 1F E6 0F FE 00 CA 93 05      |8   /
06B0    FE 01 CA DC 06 FE 02 CA D6 06 FE 03 CA D0 06 FE      |
06C0    04 CA CA 06 3E 2F 32 64 38 C9 3E 2E 32 64 38 C9      |    >/2d8 >.2d
06D0    3E 2D 32 64 38 C9 3E 2C 32 64 38 C9 3E 2B 32 64      |>-2d8 >,2d8 >+
06E0    38 C9 3E E1 32 64 38 C9 3E E2 32 64 38 C9 3E E3      |8 > 2d8 > 2d8
06F0    32 64 38 C9 3E E4 32 64 38 C9 3E 01 2F D3 EA 00      |2d8 > 2d8 > /

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F       0123456789ABCD
0700    00 DB E8 2F 47 3E 02 2F D3 EA 00 00 DB E8 2F 4F      |   /G> /
0710    78 0F 0F 0F 0F E6 0F 5F 79 0F 0F 0F 0F 57 E6 F0      |x      ÷y     W
0720    B3 32 25 38 3E 04 2F D3 EA 00 00 DB E8 2F 0F 0F      | 2%8> /       /
0730    0F 0F 47 E6 F0 4F 7A E6 0F B1 32 24 38 3E 08 2F      |  G  Oz   2$8>
0740    D3 EA 00 00 DB E8 2F 0F 0F 0F 0F 57 E6 F0 4F 78      |      /    W
0750    E6 0F B1 32 23 38 3E 10 2F D3 EA 00 00 DB E8 2F      |   2#8> /
0760    0F 0F 0F 0F 47 E6 F0 4F 7A E6 0F B1 32 22 38 3E      |    G  Oz   2"
0770    20 2F D3 EA 00 00 DB E8 2F 0F 0F 0F 0F 4F E6 F0      | /       /    O
0780    57 78 E6 0F B2 32 21 38 79 E6 0F 4F DB E9 E6 F0      |Wx   2!8y  O
0790    B1 32 20 38 3E FF D3 EA C9 2A 32 38 3A 08 38 A7      | 2 8>     *28:
07A0    CA E7 07 2A 32 38 7D FE 70 CA C9 07 7D FE A0 CA      |   *28> p   >
07B0    D2 07 7D FE D0 CA C0 07 3A 2E 38 3C 32 2E 38 C9      |  }      :.8<2.
07C0    21 D0 C7 22 8A FE C3 D8 07 21 70 D7 22 8A FE C3      |!   "      !p "
07D0    D8 07 21 A0 CF 22 8A FE 3A 28 3F A7 C2 32 08 3E      |  !   "   :(?  2
07E0    00 32 08 38 C3 32 08 3A 28 3F A7 CA 32 08 3E FF      | 2 8 2 :(?  2
07F0    32 08 38 7D FE 70 CA 10 08 7D FE A0 CA 21 08 3A      |2 8> p   >    !
```

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STARPLEX PROM Programmer utility  Version 1.0

PROM type 2716   PAGE NUMBER: 0001
```

800 PLUS

```
ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F          0123456789ABCD
0000    A9 CF F6 10 32 A9 CF 21 70 D7 22 88 FE C3 A3 07    |     2  !p "
0010    3A D9 C7 F6 10 32 D9 C7 21 A0 CF 22 88 FE C3 A3    |:     2  !  "
0020    07 3A 09 C0 F6 10 32 09 C0 21 D0 C7 22 88 FE C3    | :     2  !  "
0030    A3 07 2A 32 38 7C FE D7 C2 47 08 7D FE 70 C2 47    |  *281    G } p
0040    08 21 00 C0 22 32 38 3E 64 77 23 3E 20 77 23 22    | !  "28>dw#> w
0050    32 38 CD FA 06 2A 32 38 3A 20 38 77 23 3A 21 38    |28   *28: 8w#:
0060    77 23 3A 22 38 77 23 3A 23 38 77 23 3A 24 38 77    |w#: "8w#: #8w#: $
0070    23 3A 25 38 77 23 3E 01 77 23 3A 26 38 77 3E 00    |#: %8w#> w#: &8w
0080    32 26 38 23 3A 10 38 77 23 3A 11 38 77 23 3A 12    |2&8#: 8w#: 8w#
0090    38 77 23 3A 29 38 77 23 3A 2A 38 77 23 3A 2B 38    |8w#: )8w#: *8w#:
00A0    77 23 3A 2E 38 77 23 3E 00 77 23 77 23 77 23 22    |w#: .8w#> w#w#w
00B0    32 38 C9 2A 36 38 3A 14 38 A7 CA 01 09 2A 36 38    |28 *68: 8     *
00C0    7D FE E0 CA E3 08 7D FE 10 CA EC 08 7D FE 40 CA    |}      }      }
00D0    DA 08 3A 2F 38 3C 32 2F 38 C9 21 40 DF 22 90 FE    |  :/8<2/8 !@ "
00E0    C3 F2 08 21 E0 EE 22 90 FE C3 F2 08 21 10 E7 22    |   !  "      !
00F0    90 FE 3A 70 3F A7 C2 4C 09 3E 00 32 14 38 C3 4C    |  :p?  L > 2 8
```

800 PLUS

```
ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F          0123456789ABCD
0100    09 3A 70 3F A7 CA 4C 09 3E FF 32 14 38 7D FE E0    | :p?  L > 2 8}
0110    CA 2A 09 7D FE 10 CA 3B 09 3A 19 E7 F6 10 32 19    | * }    ;  :
0120    E7 21 E0 EE 22 8E FE C3 BD 08 3A 49 DF F6 10 32    |  !  "      :I
0130    49 DF 21 10 E7 22 8E FE C3 BD 08 3A 79 D7 F6 10    |I !  "      :y
0140    32 79 D7 21 40 DF 22 8E FE C3 BD 08 2A 36 38 7C    |2y !@ "      *6
0150    FE EE C2 61 09 7D FE E0 C2 61 09 21 70 D7 22 36    |   a }   a !p
0160    38 3E 64 77 23 3E 10 77 23 22 36 38 CD FA 06 2A    |8>dw#> w#"68
0170    36 38 3A 20 38 77 23 3A 21 38 77 23 3A 22 38 77    |68: 8w#: !8w#: "
0180    23 3A 23 38 77 23 3A 24 38 77 23 3A 25 38 77 23    |#: #8w#: $8w#: %
0190    3E 03 77 23 3A 27 38 77 3E 00 32 27 38 23 3A 10    |> w#: '8w> 2'8#
01A0    38 77 23 3A 11 38 77 23 3A 12 38 77 23 3A 29 38    |8w#: 8w#: 8w#:
01B0    77 23 3A 2A 38 77 23 3A 2B 38 77 23 3A 2F 38 77    |w#: *8w#: +8w#: /
01C0    23 3E 00 77 23 77 23 77 23 22 36 38 C9 21 B0 F6    |#> w#w#w#"68 !
01D0    22 3A 38 22 86 FE C3 E5 09 21 80 FE 22 86 FE 21    |": 8"      !  "
01E0    E0 EE 22 3A 38 3E 64 77 23 3E 01 77 23 22 3A 38    |  ": 8>dw#> w#'
```

```
01F0  CD FA 06 2A 3A 38 3A 20 38 77 23 3A 21 38 77 23   |   *:8. 8w#:!8
```

800 PLUS

```
ADDR  0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F    0123456789ABCD
0200  3A 22 38 77 23 3A 23 38 77 23 3A 24 38 77 23 3A  |:"8w#:#8w#:$8w
0210  25 38 77 23 3E 03 77 23 3A 28 38 77 3E 00 32 28  |%8w#> w#:(8w>
0220  38 23 3A 10 38 77 23 3A 11 38 77 23 3A 12 38 77  |8#: 8w#: 8w#:
0230  23 3A 29 38 77 23 3A 2A 38 77 23 3A 2B 38 77 23  |#:)8w#:*8w#:+8
0240  3E 00 77 23 77 23 77 23 77 23 22 3A 38 C9 00 3A  |> w#w#w#w#":8
0250  12 38 FE 00 C2 5F 0A 3E FF 32 19 38 C3 F1 0B 3A  | 8  ← > 2 8
0260  12 38 FE 01 CA BE 0A 3A 12 38 FE 02 CA B3 0A 3A  | 8    : 8
0270  12 38 FE 03 CA A0 0A 3A 12 38 FE 04 C2 E7 0A 3E  | 8    : 8
0280  FF 32 19 38 C3 D4 0A 3A 12 38 FE 05 CA E7 0A 3E  | 2 8  : 8
0290  00 32 28 3F 32 08 38 32 70 3F 32 14 38 C3 F5 0A  | 2(?2 82p?2 8
02A0  3E FF 32 28 3F 32 08 38 3E FF 32 70 3F 32 14 38  |> 2(?2 8> 2p?2
02B0  C3 F5 0A 3E 00 32 28 3F 32 08 38 C3 A8 0A 3E FF  |  > 2(?2 8
02C0  32 28 3F 32 08 38 3E 00 32 70 3F 32 14 38 32 19  |2(?2 8> 2p?2 8
02D0  38 C3 F5 0A 3A 19 38 FE FF C2 F5 0A 3A FF 38 FE  |8  : 8    :
02E0  11 C2 F5 0A C3 3A 0F 3E 00 32 14 38 32 70 38 32  |    : > 2 82p
02F0  19 38 C3 F1 0B 3A FF 38 FE 12 C2 A1 00 3A 29 38  | 8  : 8    :
```

800 PLUS

```
ADDR  0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F    0123456789ABCD
0300  E6 F0 FE 80 CA 13 0B 3A 30 38 E6 0E 47 CA 1D 0B  |      :08  G
0310  C3 23 0B 21 26 38 3E 80 B6 77 C3 07 0B 21 26 38  | # !&8>  w
0320  78 B6 77 11 30 38 2A 32 38 EB 19 D2 3E 0B 21 60  |x w 08*28  >
0330  30 19 D2 47 0B 3A 26 38 32 A9 CF C3 4D 0B 3A 26  |0  G :&82  M
0340  38 32 09 C0 C3 4D 0B 3A 26 38 32 D9 C7 3A 29 38  |82  M :&82
0350  FE 4B CA A6 0B E6 F0 FE 40 C2 63 0B 21 27 38 3E  | K     @ c !
0360  80 B6 77 3A 30 38 E6 0E 47 CA 72 0B 21 27 38 78  |  w:08  G r !
0370  B6 77 11 C0 20 2A 36 38 EB 19 D2 8D 0B 21 F0 18  | w   *68
0380  19 D2 96 0B 3A 27 38 32 19 E7 C3 9C 0B 3A 27 38  |    :'82
0390  32 79 D7 C3 9C 0B 3A 27 38 32 49 DF 3A 03 39 E6  |2y    :'82I :
03A0  F0 FE 20 C2 AD 0B 21 28 38 3E 80 B6 77 3A 02 39  |      !(8>  w
03B0  E6 0E 47 CA BC 0B 21 28 38 78 B6 77 11 50 09 2A  |  G   !(8. w
03C0  3A 38 19 D2 CF 0B 3A 28 38 32 B9 F6 C3 A1 00 3A  |:8    :(82
03D0  28 38 32 E9 EE C3 A1 00 21 1B 3F 11 00 00 72 23  |(82     ! ?
03E0  3E 5F BD C2 DE 0B 3E 00 32 08 38 32 28 3F C3 61  |>+    > 2 82(
```

```
03F0    01 3A 00 39 67 3A 01 39 6F 22 34 3F 21 20 3F 34      | : 9g  9o"4?! 
```

800 PLUS

```
ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F       0123456789ABCD
0400    3A 23 3F 17 D2 15 0C 2A 21 3F 23 22 21 3F 2A 3B      |:#?    *!?#"!?
0410    3F 23 22 3B 3F 21 20 3F 3A 02 3F 96 DA 96 0C 3A      |?#";?! ?: ?    
0420    3F 3F 32 3E 3F 3A 35 3F 17 DA 55 0C 3A 33 3F 17      |??2>?:5?  U :3
0430    DA 4D 0C 21 32 3F 3A 34 3F 96 21 33 3F 3A 35 3F      | M !2?:4? !3?:
0440    9E 17 D2 4D 0C 3E 00 32 3F 3F C3 6D 0C 3E FF 32      |   M > 2?? m >
0450    3F 3F C3 6D 0C 3A 33 3F 17 D2 45 0C 21 32 3F 3A      |?? m :3?  E !2
0460    34 3F 96 21 33 3F 3A 35 3F 9E C3 41 0C 21 3F 3F      |4? !3?:5?  A !
0470    3A 3E 3F BE CA 5F 0E 3A 36 3F 17 DA 8C 0C 2A 32      |:>?  ← :6?
0480    3F 22 38 3F 3E FF 32 36 3F C3 5F 0E 21 20 3F 3A      |?"8?> 26? ← !
0490    05 3F 96 D2 5F 0E 3E 00 32 20 3F 2A 32 3F 44 4D      | ?· ← > 2 ?*2?
04A0    2A 38 3F EB CD F9 0E EB 22 47 3F 2A 32 3F 22 38      |*8?     "G?*2?
04B0    3F 3A 23 3F 17 DA 2F 0D 21 00 3A 3A 24 3F 85 6F      |?:#?  / ! ::$?
04C0    3A 40 3F 96 32 40 3F 3A 41 3F 26 3B 9E 32 41 3F      |:@? 2@?:A?&; 2
04D0    D2 D7 0C 21 42 3F 35 21 01 3F 3A 00 3F 06 01 BE      |   !B?5! ?: ?
04E0    CA F6 0C 0F 4F 78 07 47 79 BE C2 E3 0C 21 00 3C      |    Ox Gy    !
04F0    3A 25 3F 85 6F EB 21 20 3C 3A 25 3F 85 6F 7E EB      |:%? o ! <:%? o
```

800 PLUS

```
ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F       0123456789ABCD
0500    57 5E 21 00 3A 3A 24 3F 85 6F 73 21 00 3B 3A 24      |W^! ::$? os! ;
0510    3F 85 6F 72 21 24 3F 34 3A 00 3F BE C2 21 0D 36      |? or!$?4: ?  !
0520    00 2A 40 3F 19 22 40 3F D2 2F 0D 21 42 3F 34 21      | *@? "@? / !B?
0530    00 3C 3A 25 3F 85 6F C6 20 47 3A 43 3F 96 32 43      | <:%? o  G:C?
0540    3F 68 3A 44 3F 9E 32 44 3F D2 50 0D 21 45 3F 35      |?h:D? 2D? P !E
0550    21 01 3F 46 21 47 3F EB 21 48 3F 7E EB 57 5E 21      |! ?F!G? !H?~ W
0560    00 3C 3A 25 3F 85 6F 73 21 20 3C 3A 25 3F 85 6F      | <:%? os! <:%?
0570    72 21 25 3F 34 3A 01 3F BE C2 7E 0D 36 00 2A 43      |r!%?4: ?  ~ 6 
0580    3F 19 22 43 3F D2 8C 0D 21 45 3F 34 3A 29 3F 1F      |? "C?   !E?4:)
0590    DA B3 0D 2A 00 3F 5C 26 00 16 00 19 EB 2A 2E 3F      |   * ?\&      *
05A0    23 22 2E 3F 7B 95 7A 9C D2 B0 0D 3E FF 32 29 3F      |#".?{ z    > 2
05B0    C3 5F 0E 2A 43 3F 22 1C 3F 3A 45 3F 32 1E 3F 3A      | ← *C?" ?:E?2 
05C0    04 3F 32 1F 3F CD 6E 0E 79 21 40 3F 96 78 21 41      | ?2 ? n y!@? x
05D0    3F 9E 7A 21 42 3F 9E D2 02 0E 3A 23 3F 17 D2 5F      |? z!B?    :#?
05E0    0E 21 3C 3F 3A 07 3F BE D2 48 0E 3E 00 32 21 3F      | !<?: ?  H > 2
```

```
05F0  32 22 3F 32 23 3F 32 3B 3F 32 3C 3F 32 28 3F C3   |2"?2#?2;?2<?2(
```

800 PLUS

```
ADDR  0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F    0123456789ABCD
0600  5F 0E C3 31 0E 2A 40 3F 22 1C 3F 3A 42 3F 32 1E   |←  1 *@?" ?:B?
0610  3F 3A 84 3F 32 1F 3F CD 6E 0E 79 21 43 3F 96 78   |?:  ?2 ? n y!C?
0620  21 44 3F 9E 7A 21 45 3F 9E D2 31 0E 3E FF 32 AE   |!D? z!E?  1 >
0630  3F 3A 23 3F 17 DA 43 0E 3E FF 32 28 3F 32 23 3F   |?:#?  C > 2(?2
0640  C3 48 0E 3E 00 32 3C 3F 21 22 3F 3A 09 3F BE C2   | H > 2<?!"?:  ?
0650  5F 0E 21 10 3F 3E 00 77 23 7D FE 49 C2 55 0E 2A   |← ! ?> w#} I U
0660  32 3F 22 30 3F 2A 34 3F 22 32 3F C3 D4 0A 3E 07   |2?"0?*4?"2?
0670  32 19 3F 3E 00 4F 47 57 32 1B 3F 32 1A 3F A7 3A   |2 ?> OGW2 ?2 ?
0680  1F 3F 1F 32 1F 3F D2 A2 0E 2A 1C 3F 09 44 4D 21   | ? 2 ?   * ? D
0690  1E 3F 7A 8E 57 21 1A 3F 3A 1B 3F 8E 32 1B 3F DA   | ?z W! ?:  ? 2
06A0  F3 0E 3A 19 3F 3D 32 19 3F C2 CF 0E 1E 02 37 3F   |  : ?=2 ?
06B0  3A 1B 3F 1F 32 1B 3F 7A 1F 57 78 1F 47 79 1F 4F   |: ? 2 ?z Wx Gy
06C0  7B 3D 5F C2 AE 0E 3A 1B 3F E6 FF C2 F3 0E C9 37   |{=←   : ?
06D0  3F 3A 1C 3F 17 32 1C 3F 3A 1D 3F 17 32 1D 3F 3A   |?:  ? 2 ?:  ? 2
06E0  1E 3F 17 32 1E 3F 3A 1A 3F 17 32 1A 3F DA F3 0E   | ? 2 ?:  ? 2 ?
06F0  C3 7E 0E 3E FF 57 47 4F C9 7A 17 DA 0D 0F 78 17   | ~ > WGO z
```

800 PLUS

```
ADDR  0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F    0123456789ABCD
0700  D2 26 0F 79 2F 6F 78 2F 67 23 19 EB C9 78 17 DA   | & y/ox/g#    >
0710  1A 0F 69 60 EB 4D 44 C3 03 0F 79 2F 4F 78 2F 47   |  i` MD   y/Ox
0720  7B 2F 5F 7A 2F 57 79 2F 6F 78 2F 67 23 19 EB 7A   |{/←z/Wy/ox/g#
0730  17 D0 7B 2F 5F 7A 2F 57 13 C9 3A 02 39 67 3A 02   |  {/←z/W  : 9g
0740  39 6F 22 78 3F 3A 73 3F 32 72 3F 2A 80 3F 23 22   |9o"x?:s?2r?* ?
0750  80 3F 3A 79 3F 17 DA 82 0F 3A 77 3F 17 DA 7A 0F   | ?:y?    :w?
0760  21 76 3F 3A 78 3F 96 21 77 3F 3A 79 3F 9E 17 D2   |!v?:x? !w?:y?
0770  7A 0F 3E 00 32 73 3F C3 9A 0F 3E FF 32 73 3F C3   |z > 2s?   > 2s
0780  9A 0F 3A 77 3F 17 D2 72 0F 21 76 3F 3A 78 3F 96   |  :w?  r !v?:x
0790  21 77 3F 3A 79 3F 9E C3 6E 0F 3A 71 3F FE 03 D2   |!w?:y?  n :q?
07A0  A9 0F 21 71 3F 34 C3 07 10 21 72 3F 3A 73 3F BE   |  !q?4   !r?:s
07B0  CA 07 10 3A 7A 3F 17 DA C8 0F 2A 76 3F 22 7B 3F   |   :z?    *v?"
07C0  3E FF 32 7A 3F C3 07 10 2A 76 3F 44 4D 2A 7B 3F   |> 2z?   *v?DM*
07D0  EB CD F9 0E EB 22 7D 3F 2A 76 3F 22 7B 3F 21 60   |     "}?*v?"{?
07E0  3F 3A 7D 3F 96 23 3A 7E 3F 9E D2 16 10 21 62 3F   |?:}? #:~?
07F0  3A 80 3F 96 23 3A 81 3F 9E DA 07 10 3E 00 32 70   |: ? #: ?    >
```

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STARPLEX PROM Programmer utility  Version 1.0

PROM type 2716   PAGE NUMBER: 0001
```

1000 PLUS

```
ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F        0123456789ABCD
0000    3F 32 80 3F 32 81 3F 2A 76 3F 22 74 3F 2A 78 3F       |?2 ?2 ?*v?"t?*
0010    22 76 3F C3 A1 00 3E FF 32 70 3F 32 18 38 3E 00       |"v?    > 2p?2 8
0020    32 80 3F 32 81 3F C3 07 10 FF FF FF FF FF FF FF       |2 ?2 ?
0030    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
0040    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
0050    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
0060    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
0070    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
0080    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
0090    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
00A0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
00B0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
00C0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
00D0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
00E0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
00F0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
```

1000 PLUS

```
ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F        0123456789ABCD
0100    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
0110    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
0120    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
0130    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
0140    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
0150    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
0160    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
0170    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
0180    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
0190    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
01A0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
01B0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
01C0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
01D0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
01E0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
01F0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF       |
```

APPENDIX B.2

2708 EPROM LISTING
MICROPROCESSOR TWO

```
STARPLEX PROM Programmer utility  Version 1.0

PROM type 2708   PAGE NUMBER: 0001

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F        0123456789ABCDE
0000    00 F3 00 00 00 00 00 00 00 00 00 00 00 00 00 00      |
0010    00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00      |
0020    00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00      |
0030    00 00 F3 31 00 3F 21 FF 38 3E 80 D3 ED 3E 00 D3     |    1 ?! 8>    >
0040    ED 3E 40 D3 ED 3E 1C D3 ED 3E AA D3 ED 3E AA D3     | >@  >    >    >
0050    ED 3E 86 D3 ED DB EC DB ED E6 40 CA 57 00 DB ED     | >          @ W
0060    E6 02 CA 5E 00 DB EC 77 23 DB ED E6 02 CA 69 00     |    ^    w#       i
0070    DB EC 77 23 DB ED E6 02 CA 74 00 DB EC 77 23 DB     |   w#       t    w#
0080    ED E6 02 CA 7F 00 DB EC 77 23 DB ED E6 02 CA 8A     |           w#
0090    00 DB EC 77 23 DB ED E6 02 CA 95 00 DB EC 77 23     |    w#              t
00A0    DB ED E6 02 CA A0 00 DB EC 77 23 DB ED E6 02 CA     |             w#
00B0    AB 00 DB EC 77 23 DB ED E6 02 CA B6 00 DB EC 77     |     w#
00C0    11 00 FF 21 FF 38 7E EB 77 23 EB 23 7E EB 77 23     |    ! 8~ w# #~ w
00D0    EB 23 7E EB 77 23 EB 23 7E EB 77 23 EB 23 7E EB     | #~ w# #~ w# #~
00E0    77 23 EB 23 7E EB 77 23 EB 23 7E EB 77 23 EB 23     |w# #~ w# #~ w# #
00F0    7E EB 77 23 EB 23 7E EB 77 C3 32 00 FF FF FF FF     |~ w# #~ w 2

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F        0123456789ABCDE
0100    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0110    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0120    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0130    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0140    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0150    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0160    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0170    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0180    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0190    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
01A0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
01B0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
01C0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
01D0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
01E0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
01F0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
```

APPENDIX B.3

2708 EPROM LISTING
MICROPROCESSOR THREE

```
STARPLEX PROM Programmer utility  Version 1.0

PROM type 2708   PAGE NUMBER: 0001

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F        0123456789ABCD
0000    00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00      |
0010    00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00      |
0020    00 00 00 00 00 31 00 3F 3E 89 D3 EB F3 3E 80 D3      |     1 ?>    >
0030    ED 3E 00 D3 ED 3E 40 D3 ED 3E 1C D3 ED 3E AA D3      | >   >@  >   >
0040    ED 3E AA D3 ED 3E 86 D3 ED DB EC DB ED E6 40 CA      | >   >          @
0050    4B 00 DB ED E6 02 CA 52 00 DB EC D3 E8 47 32 00      |K      R     G
0060    38 DB ED E6 02 CA 61 00 DB EC 4F 32 01 38 78 FE      |8     a.  02 8
0070    12 CA 7F 00 FE 13 C2 82 00 79 D3 E8 C3 82 00 79      |          y
0080    D3 E9 C3 2C 00 FF FF FF FF FF FF FF FF FF FF FF      |   ,
0090    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
00A0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
00B0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
00C0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
00D0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
00E0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
00F0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F        0123456789ABCD
0100    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0110    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0120    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0130    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0140    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0150    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0160    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0170    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0180    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0190    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
01A0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
01B0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
01C0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
01D0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
01E0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
01F0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
```

APPENDIX B.4

2708 EPROM LISTING
MICROPROCESSOR FOUR

```
STARPLEX PROM Programmer utility  Version 1.0

PROM type 2708   PAGE NUMBER: 0001

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F        0123456789ABCD
0000    00 F3 00 00 00 00 00 00 00 00 00 00 00 00 00 00      |
0010    00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00      |
0020    00 00 F3 31 00 3F 3E 92 D3 E7 3E 9B D3 EB 3E 00      |   1 ?>   >
0030    32 00 38 21 FF 38 3E 00 77 23 7D FE FF C2 36 00      |2 8! 8> w#}
0040    3E 80 D3 ED 3E 00 D3 ED 3E 40 D3 ED DB E8 47 E6      |>   >   >@
0050    10 CA 30 02 3A 00 38 B8 CA 33 02 78 32 00 38 78      |  0 : 8  3 x2
0060    FE 10 C2 71 00 32 FF 38 CD 66 01 CD E7 01 C3 A8      |  .q 2 8 f
0070    00 78 FE 11 C2 83 00 32 FF 38 CD 66 01 CD A7 01      | x     2 8 f
0080    C3 A8 00 78 FE 12 C2 9C 00 32 FF 38 CD 66 01 DB      |   x     2 8 f
0090    E9 32 02 39 DB EA 32 03 39 C3 A8 00 78 FE 13 C2      | 2 9  2 9   x
00A0    36 02 32 FF 38 CD 66 01 21 FF 38 3E 1C D3 ED 3E      |6 2 8 f ! 8>
00B0    AA D3 ED 3E AA D3 ED 3E 33 D3 ED DB ED E6 01 CA      |   >   >3
00C0    BB 00 3E AA D3 EC DB ED E6 01 CA C6 00 3E AA D3      |  >           >
00D0    EC DB ED E6 01 CA D1 00 7E D3 EC 23 DB ED E6 01      |         ~  #
00E0    CA DC 00 7E D3 EC 23 DB ED E6 01 CA E7 00 7E D3      |   ~  #
00F0    EC 23 3A FF 38 FE 13 C2 FF 00 DB E8 32 02 39 DB      | #: 8       2

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F        0123456789ABCD
0100    ED E6 01 CA FF 00 7E D3 EC 23 DB ED E6 01 CA 0A      |       ~  #
0110    01 7E D3 EC 23 DB ED E6 01 CA 15 01 7E D3 EC 23      | ~  #       ~
0120    DB ED E6 01 CA 20 01 7E D3 EC 23 DB ED E6 01 CA      |       ~  #
0130    2B 01 7E D3 EC 23 DB ED E6 01 CA 36 01 7E D3 EC      |+ ~  #     6 ~
0140    DB ED E6 01 CA 40 01 3E 00 D3 EC DB ED E6 01 CA      |     @ >
0150    4B 01 3E 40 D3 ED 21 FF 38 3E 00 77 23 7D FE 08      |K >@  ! 8> w#}
0160    C2 59 01 C3 4C 00 3E FF D3 E6 CD 27 02 00 00 00      | Y  L >    '
0170    DB E5 32 00 39 DB E4 2F 32 01 39 C9 3E FE D3 E6      |  2 9  /2 9 >
0180    CD 27 02 00 00 00 DB E5 32 02 39 DB E4 2F 32 03      | '       2 9
0190    39 3E FD D3 E6 CD 27 02 00 00 00 DB E5 32 04 39      |9>    '
01A0    DB E4 2F 32 05 39 C9 3E FC D3 E6 CD 27 02 00 00      |  /2 9 >    '
01B0    00 DB E5 32 02 39 DB E4 2F 32 03 39 3E FB D3 E6      |   2 9  /2 9>
01C0    CD 27 02 00 00 00 DB E5 32 04 39 DB E4 2F 32 05      | '       2 9
01D0    39 3E FA D3 E6 CD 27 02 00 00 00 DB E5 32 06 39      |9>    '
01E0    DB E4 2F 32 07 39 C9 3E F9 D3 E6 CD 27 02 00 00      |  /2 9 >    '
```

```
01F0    00 DB E5 32 02 39 DB E4 2F 32 03 39 3E F8 D3 E6      |   2 9  /2 9> 

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F       0123456789ABCD
0200    CD 27 02 00 00 00 DB E5 32 04 39 DB E4 2F 32 05      | '       2 9  /
0210    39 3E F7 D3 E6 CD 27 02 00 00 00 DB E5 32 06 39      |9>     '        2
0220    DB E4 2F 32 07 39 C9 3E 08 D3 E7 3E 09 D3 E7 C9      |  /2 9 >   >
0230    C3 4C 00 C3 4C 00 C3 4C 00 FF FF FF FF FF FF FF      | L  L  L
0240    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0250    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0260    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0270    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0280    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0290    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
02A0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
02B0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
02C0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
02D0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
02E0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
02F0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F       0123456789ABCD
0300    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0310    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0320    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0330    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0340    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0350    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0360    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0370    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0380    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
0390    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
03A0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
03B0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
03C0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
03D0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
03E0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
03F0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
```

APPENDIX B.5

2708 EPROM LISTING
MICROPROCESSOR SIX

```
STARPLEX PROM Programmer utility  Version 1.0

PROM type 2708   PAGE NUMBER: 0001

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F        0123456789ABCD
0000    00 F3 31 E0 3F 3E 07 D3 00 CD 50 03 CD 65 03 21
0010    00 00 22 00 3E 22 02 3E CD A2 03 CD 65 03 CD AC
0020    03 CD 3D 03 CD 50 03 CD 5A 00 CD 78 00 3E FF 32
0030    96 FE 21 00 00 22 00 3E 22 02 3E DB F6 E6 0F FE
0040    0D C2 4E 00 3E 00 32 01 3E 3E FF 32 96 FE DB F6
0050    E6 0F FE 0B C2 80 00 C3 1B 00 21 00 00 22 86 FE
0060    22 88 FE 22 8A FE 22 8C FE 22 8E FE 22 90 FE 22
0070    92 FE 3E 00 32 94 FE C9 3A 94 FE 1F D2 78 00 C9
0080    2A 86 FE EB 21 00 00 22 86 FE 7A FE F6 C2 9F 00
0090    7B FE B0 C2 9F 00 21 E0 EE CD D6 01 C3 B4 00 7A
00A0    FE FE C2 B4 00 7B FE 80 C2 B4 00 21 B0 F6 CD D6
00B0    01 C3 FA 00 2A 88 FE EB 21 00 00 22 88 FE 7A FE
00C0    C7 C2 D3 00 7B FE D0 C2 D3 00 21 00 C0 CD D6 01
00D0    C3 FA 00 7A FE CF C2 E8 00 7B FE A0 C2 E8 00 21
00E0    D0 C7 CD D6 01 C3 FA 00 7A FE D7 C2 FA 00 7B FE
00F0    70 C2 FA 00 21 A0 CF CD D6 01 2A 8A FE EB 21 00

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F        0123456789ABCD
0100    00 22 8A FE 7A FE C7 C2 19 01 7B FE D0 C2 19 01
0110    21 00 C0 CD D6 01 C3 40 01 7A FE CF C2 2E 01 7B
0120    FE A0 C2 2E 01 21 D0 C7 CD D6 01 C3 40 01 7A FE
0130    D7 C2 40 01 7B FE 70 C2 40 01 21 A0 CF CD D6 01
0140    2A 8E FE EB 21 00 00 22 8E FE 7A FE DF C2 5F 01
0150    7B FE 40 C2 5F 01 21 70 D7 CD D6 01 C3 86 01 7A
0160    FE E7 C2 74 01 7B FE 10 C2 74 01 21 40 DF CD D6
0170    01 C3 86 01 7A FE EE C2 86 01 7B FE E0 C2 86 01
0180    21 10 E7 CD D6 01 2A 90 FE EB 21 00 00 22 90 FE
0190    7A FE DF C2 A5 01 7B FE 40 C2 A5 01 21 70 D7 CD
01A0    D6 01 C3 CC 01 7A FE E7 C2 BA 01 7B FE 10 C2 BA
01B0    01 21 40 DF CD D6 01 C3 CC 01 7A FE EE C2 CC 01
01C0    7B FE E0 C2 CC 01 21 10 E7 CD D6 01 00 CD 65 03
01D0    CD 50 03 C3 7C 03 3E 20 D3 01 3E 20 D3 02 3E 28
01E0    D3 02 3E 20 D3 02 3E 00 D3 03 16 02 06 32 0E 32
```

```
01F0    1E 00 3E 22 D3 01 3E 00 32 05 3E 3E A0 D3 02 3E      |  >"  > 2 >> 

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F       0123456789ABCD
0200    20 D3 02 7E 23 D3 01 DB 00 A2 CA 1E 02 1C C2 07      |   ~#
0210    02 3A 05 3E 3C 32 05 3E C2 07 02 C3 6C 03 7E D3      | : ><2 >    l
0220    01 5A DB 00 A2 CA 2F 02 1C C2 22 02 C3 6C 03 23      | Z    /   "  l
0230    7E D3 01 0C C2 21 02 5A DB 00 A2 CA 45 02 1C C2      |~     ! Z    E
0240    38 02 C3 6C 03 23 7E D3 01 0C C2 37 02 5A DB 00      |8  l #~    7 Z
0250    A2 CA 5B 02 1C C2 4E 02 C3 6C 03 23 7E D3 01 0C      |  [   N  l #~
0260    C2 4D 02 5A DB 00 A2 CA 71 02 1C C2 64 02 C3 6C      | M Z    q   d
0270    03 23 7E D3 01 0C C2 63 02 5A DB 00 A2 CA 87 02      | #~     c Z
0280    1C C2 7A 02 C3 6C 03 23 7E D3 01 0C C2 79 02 5A      |  z  l #~     y
0290    DB 00 A2 CA 9D 02 1C C2 90 02 C3 6C 03 23 7E D3      |               l #
02A0    01 0C C2 8F 02 5A DB 00 A2 CA B3 02 1C C2 A6 02      |      Z
02B0    C3 6C 03 23 7E D3 01 0C C2 A5 02 5A DB 00 A2 CA      | l #~       Z
02C0    C9 02 1C C2 BC 02 C3 6C 03 23 7E D3 01 0C C2 BB      |         l #~
02D0    02 5A DB 00 A2 CA DF 02 1C C2 D2 02 C3 6C 03 3E      | Z              l
02E0    FF D3 03 3E 20 D3 01 3E 00 06 00 0E FD 3C C2 ED      |   >   >      <
02F0    02 04 C2 ED 02 0C C2 ED 02 3E 00 D3 03 CD 3D 03      |          >

ADDR    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F       0123456789ABCD
0300    3A 00 3E A7 C2 27 03 3A 02 3E 3C 32 02 3E C2 26      |: >  ' : ><2 >
0310    03 3A 03 3E 3C 32 03 3E FE 18 C2 26 03 3E 00 D3      | : ><2 >   & >
0320    F6 3E FF 32 00 3E C9 3A 01 3E 3C 32 01 3E FE 64      | > 2 > : ><2 >
0330    C2 3C 03 3E 00 D3 F6 3E 00 32 01 3E C9 3E 00 06      | < >   > 2 > >
0340    00 0E FD 3C C2 43 03 04 C2 43 03 0C C2 43 03 C9      |   < C   C   C
0350    3E FF D3 03 3E 20 D3 01 3E 20 D3 02 3E 28 D3 02      |>   >   >   >(
0360    3E 20 D3 02 C9 3E 00 3C C2 67 03 C9 3E 00 32 96      |>    > < g  >  2
0370    FE CD 50 03 CD 3D 03 3E FF 32 96 FE DB F6 E6 0F      |  P  = > 2
0380    FE 0B C2 3B 00 DB F5 2F E6 F0 FE E0 C2 3B 00 3E      |   ;   /      ;
0390    21 D3 01 3E 20 D3 02 3E A0 D3 02 3E 20 D3 02 C3      |!  >   >   >
03A0    3B 00 DB F6 E6 0F FE 0F C2 A2 03 C9 DB F6 E6 0F      |;
03B0    FE 0B CA AC 03 C9 00 00 00 00 00 00 00 00 00 00      |
03C0    00 00 00 00 00 00 00 00 21 77 AA 22 98 FE C3 2D      |         !w "
03D0    00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
03E0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
03F0    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF      |
```

APPENDIX C.1

LINK MAP FILE
MICROPROCESSOR ONE

STARPLEX(TM) LINK MAP OF FILE FDS1:UP1.BIN 7/ 2/1982 10:34:22

PUBLIC SYMBOLS

0165 CLOCK 0A4E ED 0007 EDRET 0161 RESED
00A1 RETURN 0BD8 SRSTRT

MODULE [UP1] CODE [0000H] DATA [ ]

0593 ABORT 05BC C20 05C2 C21 05C8 C22
05CE C23 05D4 C24 05DA C25 068A C26
0684 C27 067E C28 0678 C29 0672 C2A
06DC C2B 06D6 C2C 06D0 C2D 06CA C2E
06C4 C2F 05FC C80 0602 C81 0608 C82
060E C83 0636 C84 063C C85 0642 C86
0648 C87 064E C88 0405 CALCON 0542 CALDE
0165 CLOCK 03DB CO11 03BC CODCK 03E6 CSPS
033B DATMO 016C DEBNC 038E DISA 0397 DISB
03A0 DISC 03B3 DISD 0007 EDRET 031E ENDIT
0329 ENDX 2000 EVENTA 200C EVENTB 0164 EVNTR
0547 FSO 00C7 GO 092A IMOON1 093B IMOON2
0919 IMOON3 0058 INIT 014A IPAGA 08BD IPAGAI
0429 IPDIS 08F2 IPEO 0901 IPEVNT 06A2 IPPHO
025C IPR1CH 0271 IPR2CH 0690 IPRES 04F8 IPSTO
08B3 IPTIME 0961 ISETB1 0965 ISETB2 096F ISETB3
0977 ISETB4 097C ISETB5 0981 ISETB6 0986 ISETB7
098B ISETB8 0990 ISETB9 0994 ISETBA 099E ISETBB
09A3 ISETBC 09A8 ISETBD 09AD ISETBE 09B2 ISETBF
09B7 ISETBG 09BC ISETBH 09C1 ISETBX 00F3 KEYSC
00FC LOEDC 0488 LPDIS 02A5 LPR1CH 069C LPRES
0654 LPSIN 051D LPSTO 0599 LPSTP 09D9 LPTIM1
09CD LPTIM2 09E9 LSETB2 09F3 LSETB3 09FB LSETB4
0A00 LSETB5 0A05 LSETB6 0A0A LSETB7 0A0F LSETB8
0A14 LSETB9 0A18 LSETBA 0A22 LSETBB 0A27 LSETBC
0A2C LSETBD 0A31 LSETBE 0A36 LSETBF 0A3B LSETBG
0A40 LSETBX 094C MIPP 0810 MOON1 0821 MOON2
07FF MOON3 0832 MSPP 00DC NOGO 01BB NUMB
00EE OFLAG 00D5 ONAG 00EA ONANG 036D OUTDA
03EF PDITES 00B4 RESCAL 0161 RESED 00A1 RETURN
013C RIAGA 0290 SEN10 0241 SEN11 0233 SEN12
0225 SEN13 02B4 SEND10 0283 SEND11 0847 SETBY1
084B SETBY2 0855 SETBY3 085D SETBY4 0862 SETBY5
0867 SETBY6 086C SETBY7 0871 SETBY8 0876 SETBY9
087A SETBYA 0884 SETBYB 0889 SETBYC 088E SETBYD
0893 SETBYE 0898 SETBYF 089D SETBYG 08A2 SETBYH
08A7 SETBYX 07A3 SPAGAI 0408 SPDIS 07D8 SPEO
07E7 SPEVNT 002F SPINIT 0195 SPR1CH 01AA SPR2CH
0696 SPRES 0614 SPSIN 04E7 SPSTO 05E0 SPSTP
017A SPTC 0799 SPTIME 07C9 STAR1 07D2 STAR2
07C0 STAR3 06FA STIME 03CD STODA 00B9 TELST
06E2 TEST1 06E8 TEST2 06EE TEST3 06F4 TEST4
09E5 TIMELP 02BE TRANS 02DA TXREO 02E5 TXRE1
02F0 TXREA 02FC TXREB 0308 TXREC 0313 TXRED
0095 WAITST 08E3 WSTAR1 08EC WSTAR2 08DA WSTAR3
0048 ZER1 0035 ZERO

```
MODULE [ED]              CODE [0A4EH]      DATA [      ]

0CD7 AA          0D50 ABLE1         0CE3 ABX         0CF6 ABY
0E89 ADMTPD      0EA2 BRAVO         0AF5 CALAMP      0C55 D3NEG
1016 DEIPEV      0A8F DSI6F         0A4F DSW0        0A5F DSW1
0A67 DSW2        0A6F DSW3          0A77 DSW4        0AE7 DSW5
0A87 DSWN5       0A4E ED            0B63 IPAMST      0B96 IPD749
0F3A IPED        0B5C IPP           0B72 IPPNTR      0B8D IPWRDT
0AD4 ISWBF1      0DB3 KSPA          0BAD LPAMST      0B4D LPCAL
0BCF LPMBX       0BA6 LPPCAL        0BBC LPPNTR      0B9C LPTEST
0E31 LTAFR       0E6E MULTSR        0F0D NEG1        0F03 NEG2
0F1A NEG3        0D21 NEXT          0F26 POS2        0E52 RIED
0E55 RIED1       0DEB RSPED         0B07 SAMP        0C6D SDED
0C4D SETFF       0EF3 SETMAX        0E38 SETSPE      0ECF SFTLMT
0E7E SFTRMT      0EAE SFTRT         1007 SHFIDP      0E5F SHFTDP
0FA9 SIGEQU      0C41 SIGNP         0DB0 SKIP        0BDE SPAGIN
0B1D SPAMST      0AA0 SPDFS1        0BF1 SPED        0E48 SPEDE
0CB1 SPLTAF      0D8C SPNC1         0B13 SPP         0B23 SPPNTR
0C8C SPSCG       0C15 SPSCGP        0D7E SPSTAR      0D2F SPTPS
0BD8 SRSTRT      0C45 SSET00        0AB3 SSPF0       0ABE SSPF1
0E02 STAKIP      0FC8 SUBPL         0EF9 SUBSR       0AA8 WBF1
0F82 WD3NEG      0B3E WRC009        0B47 WRC7D9      0F9A WSDED
0F72 WSET00      0F7A WSETFF        0F6E WSIGNP      0E43 ZEOC
0C96 ZSPSC

                LOWEST     HIGHEST    LENGTH
ABSOLUTE             0           0         0
CODE                 0        1028      1029
DATA                 0           0         0
COMMON               0           0         0
STACK             1029        1128       100
MEMORY            1129        FFFF      EED7
EXECUTION ADDRESS                0

    0 DUPLICATED PUBLIC DECLARATION(S).
    0 UNRESOLVED EXTERNAL REFERENCE(S).
```

APPENDIX C.2

LINK MAP FILE
MICROPROCESSOR TWO

```
STARPLEX(TM) LINK MAP OF FILE FDS1:UP2.BIN          10/29/1981  14:39:58

PUBLIC SYMBOLS


MODULE [UP2]              CODE [0000H]      DATA [      ]

0032 AGAIN          00C6 MOVE1          00CC MOVE2          00D2 MOVE3
00D8 MOVE4          00DE MOVE5          00E4 MOVE6          00EA MOVE7
00F0 MOVE8          00F6 MOVE9          005E RXRE1          0069 RXRE2
0074 RXRE3          007F RXRE4          008A RXRE5          0095 RXRE6
00A0 RXRE7          00AB RXRE8          00B6 RXRE9          0000 START
0057 SYND1          0001 UPTHR

                LOWEST     HIGHEST    LENGTH
ABSOLUTE             0           0         0
CODE                 0          FB        FC
DATA                 0           0         0
COMMON               0           0         0
STACK               FC         1FB       100
MEMORY             1FC        FFFF      FE04
EXECUTION ADDRESS                0

    0 DUPLICATED PUBLIC DECLARATION(S).
    0 UNRESOLVED EXTERNAL REFERENCE(S).
```

APPENDIX C.3

LINK MAP FILE
MICROPROCESSOR THREE

```
STARPLEX(TM) LINK MAP OF FILE FDS1:UP3.BIN          5/28/1982  11:36:56

PUBLIC SYMBOLS


MODULE [UP3]              CODE [0000H]      DATA [      ]

007F DATA2          0082 ENDIT          0052 RXRE1          0061 RXRE2
0000 START          004B SYND1          002C UPTHR


                LOWEST     HIGHEST    LENGTH
ABSOLUTE             0           0         0
CODE                 0          84        85
DATA                 0           0         0
COMMON               0           0         0
STACK               85         184       100
MEMORY             185        FFFF      FE7B
EXECUTION ADDRESS                0

    0 DUPLICATED PUBLIC DECLARATION(S).
    0 UNRESOLVED EXTERNAL REFERENCE(S).
```

APPENDIX C.4

LINK MAP FILE
MICROPROCESSOR FOUR

```
STARPLEX(TM) LINK MAP OF FILE FDS1:UP4.BIN          5/28/1982  11:38:31

PUBLIC SYMBOLS


MODULE [UP4]              CODE [0000H]      DATA [      ]

0071 DATA1          0083 DATA2          009C DATA3          0140 ENDIT
014B ENDY           01A7 IPSR           0230 LASTA          0233 LASTB
0236 LASTC          01E7 LPSR           0036 MEMZ           00A8 OUTPUT
004C RECST          0166 SPSR           0000 START          0227 STROB
00C6 TXRE1          00D1 TXREA          00DC TXREB          00E7 TXREC
00F2 TXRED          00FF TXRED1         010A TXREE          0115 TXREF
0120 TXREG          012B TXREH          0136 TXREI          00BB TXREO
0159 ZERO


                LOWEST     HIGHEST    LENGTH
ABSOLUTE             0           0         0
CODE                 0         238       239
DATA                 0           0         0
COMMON               0           0         0
STACK              239         338       100
MEMORY             339        FFFF      FCC7
EXECUTION ADDRESS                0

    0 DUPLICATED PUBLIC DECLARATION(S).
    0 UNRESOLVED EXTERNAL REFERENCE(S).
```

APPENDIX C.5

LINK MAP FILE
MICROPROCESSOR SIX

```
STARPLEX(TM) LINK MAP OF FILE FDS1:TAPEW.BIN          1/30/1982  10:28:56

PUBLIC SYMBOLS

0000 INITRC


MODULE [TAPEW]          CODE [0000H]       DATA [      ]

004E CHCKSL         0080 CHCKWR         0078 CK8005         0326 CNR1RT
033C CNR2RT         0365 DEL1MS         001B DELAYF         02ED DELNOW
033D DL1SEC         01CC END            021E END1           022F END1SH
0245 END2SH         025B END3SH         0271 END4SH         0287 END5SH
029D END6SH         02B3 END7SH         02C9 END8SH         02DF END9SH
0221 HERE1S         0237 HERE2S         024D HERE3S         0263 HERE4S
0279 HERE5S         028F HERE6S         02A5 HERE7S         02BB HERE8S
02D1 HERE9S         0207 IN1            0343 INCA           0327 INCCN2
0000 INITRC         0140 IP1            015F IP12           0174 IP13
0186 IP2            01A5 IP22           01BA IP23           037C ISDSWF
008A LP1T           009F LP2T           0367 MS1            01D6 PLSRST
003B RECYCL         036C RESDEL         0350 RESET1         01CD RETURN
005A RPNTRS         0222 SHOT1          0238 SHOT2          024E SHOT3
0264 SHOT4          027A SHOT5          0290 SHOT6          02A6 SHOT7
02BC SHOT8          02D2 SHOT9          00B4 SP1            00D3 SP12
00E8 SP13           00FA SP2            0119 SP22           012E SP23
0018 START1         03AC SWCL           03A2 SWOPN          002D ZERO2

                  LOWEST     HIGHEST    LENGTH
ABSOLUTE               0           0         0
CODE                   0         3D0       3D1
DATA                   0           0         0
COMMON                 0           0         0
STACK                3D1         4D0       100
MEMORY               4D1        FFFF      FB2F
EXECUTION ADDRESS                  0

     0 DUPLICATED PUBLIC DECLARATION(S).
     0 UNRESOLVED EXTERNAL REFERENCE(S).
```

APPENDIX D

OPERATIONAL INSTRUCTIONS
DWWSSN DRS TELEMETRY SYSTEM

FORM: DWT-1
FORM BY: CLARK
ASL 02/22/82

DWWSSN DRS-TELEMETRY DAILY ROUTINE CHECKLIST

1. Check and correct clock. (See the Time Check and Correction Procedure for the Systron Donner clock, Form DWT-23.) Be sure time correction is noted in logs.

   NOTE: Change the tape once a week (See Tape Change Procedure, Form DWT-3.)

2. Mark the position of the tape reel with a small piece of tape on the cover. This will be used as a reference mark later to be sure the tape is moving.

3. Change helicorder record, stamp, and mark it. Be sure drum is indexed properly so hours will be in center of record.

4. Calibrate the SP and LP as usual. (See Calibrator Control Switch Designation, Form DWT-22.)

5. Before leaving, verify that the clock display and the DRS System On Light is on continuously, no flicker. Also check the position of the tape reel and be sure it has moved with respect to the small piece of tape put on in Step 2. If it has not moved, the system has stopped recording and must be re-started. (Note "Data Gap" on tape log and re-start as in Step 7 of Tape Change Procedure, Form DWT-3.)

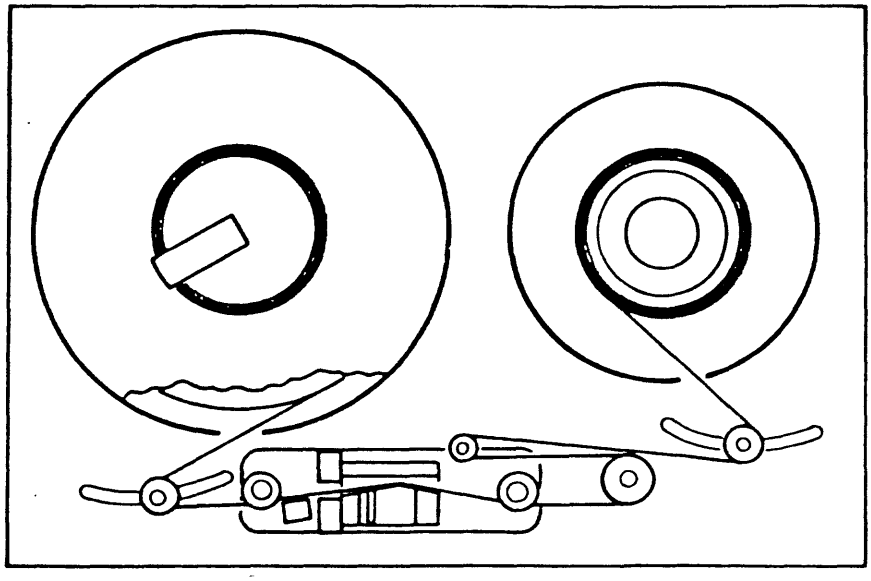
DWWSSN TAPE CHANGE PROCEDURE
(Normally once-a-week)

1. Check clock and correct as needed. (See Time Check and Correction Procedure, Form DWT-23.)

2. On Digital Recording System (DRS), set Master Switch D to position 14 and turn Master Key, release Master Key, pause 2-3 seconds (tape should move, again turn Master Key and tape again should move). Observe at least two End-of-file marks being put on tape (tape will space forward), then change switch D back to original position and turn Master Key.

3. Push "On-Line" buttom on tape deck so that "On-Line" light goes out. Then push "Rewind" buttom. When tape stops rewinding, push "Rewind" buttom again and remove tape. Put hold-down strip on end of tape and put tape seal about reel. Write approximate time off (to nearest minute) on mag tape ID sticker. Put tape and tape log in shipping box and use franked label to send to Albuquerque Seismological Laboratory (ASL).

4. Open a new reel of tape and remove tape seal and hold-down strip. Mount on tape unit and thread according to diagram:



NOTE: Once a week, clean head and rollers with cottom swab dipped in alcohol. Head cover flips up to the right. DO NOT CLEAN CAPSTAN WITH ALCOHOL!!! Clean capstan once a month with damp rag dampened with clean water.

5. After tape has been threaded, push "Load" button. Tape will space forward and stop at BOT (Beginning-of-Tape) marker. (It may take 15 or 20 seconds to stop if the leader is long.)

6. Peel off the next sequential mag tape ID sticker and stick on side of tape reel. Write approximate time on sticker to nearest minute (use next minute coming up on clock).

7. Close tape deck door. Do the following operations in the order shown:

   A. Depress Intel Unit Reset Switch (alarm will come on).
   B. Depress Intel Unit Interrupt Switch (ON light goes off).
   C. Set Master Switch B to _____, C to _____, and D to _____.
   D. Turn Master Key. The alarm should turn off. If not, turn Intel Unit off, then on and begin at Step 7A.
   E. Depress System Control Start Switch (ON light will go on).
   F. Depress "On Line" button on tape deck.

8. Mark the position of the tape with a small piece of tape for later observation. Change the helicorder record. Mark the first minute with the year, day number, hour, and minute. Stamp and mark the record just removed.

9. Observe the tape deck has moved tape, i.e. written one or more records.

DWWSSN DRS TELEMETRY SYSTEM
INITIAL OPERATIONAL PROCEDURES
CONTROL UNIT

1. Connect main 115 VAC system power cord into a 115 VAC power socket.

2. Turn on TOPAZ Backup Power Units.

3. Insure all AC power cords from individual system units are connected to the red 115 VAC power strips. The only exceptions are the TOPAZ units, fan unit, and helicorder units.

4. Turn on:

   A. Modem
   B. D/A Multiplexer Distributor
   C. Helicorders and associated amplifiers
   D. Kennedy Tape Recorder
   E. Intel Microprocessor System (alarm, alarm light, and no-go light should turn on)
   F. Systron Donner Clock (set clock as per Clock Set Instructions, Form DWT-23)

5. Set System Configuration (set system as per Tape Change Procedure, Form DWT-3)

   A. T Switch 1-9
   B. B Switch SP Event Detect
   C. C Switch IP Event Detect
   D. D Switch type of recording

6. Load blank magnetic tape in recorder, press LOAD TAPE SWITCH (see Tape Change Procedure, Form DWT-3)

7. Press Start switch, red ON LIGHT comes on.

8. Turn MASTER KEY. If remote is on and working properly -

   A. ALARM and ALARM LIGHT goes off.
   B. GO LIGHT comes on and T SWITCH value is displayed.
   C. Selected analog channels are recorded on helicorders.

If all the above, THE SYSTEM IS WORKING.

   D. Place Kennedy Tape Recorder ON LINE.

If system writes records, i.e. moves tape, THE SYSTEM IS OPERATIONAL.

NOTE: Observe the Modem XMIT DATA light, CARRIER DETECT light, and the RCV DATA light blinking pattern. The XMIT DATA light means the main unit is transmitting commands to the remote unit. The CARRIER DETECT light and RCV DATA lights mean the remote unit is transmitting data to the main unit. Note the difference between the blinking lights. This is because the main unit transmits four words per 50 millisecond data period (20 samples per second). The remote unit transmits eleven words per 50 millisecond data period.

9. Calibration: (see Calibrator Control Switch Designations, Form DWT-22)

   A. Any ABORT CODE transmitted will blink the remote CALIBRATOR DISPLAYS. This is an excellent way to test the main to remote telemetry link operation. (It requires an operator at the remote site.)

   B. Set the F SWITCH to zero (0) and press the CALIBRATION ACTIVATE switch. This aborts any calibration in progress and recycles the CALIBRATOR.

   C. Select appropriate calibration by the F SWITCH and select the appropriate calibration level by the LEVEL SWITCHES. Press CALIBRATION ACTIVATE SWITCH to start calibration. Note the time required to complete calibration and observe the calibration on the helicorders. An ABORT will terminate any calibration immediately.

10. Alarms:

   A. Initially ALARM is on continuous until main system is operational. GO LIGHT, visible data, and MODEM lights indicate REMOTE UNIT is operational.

   B. LOW TAPE ALARM comes on when 80% of magnetic tape is used. Pressing the ALARM RESET SWITCH will silence the alarm for another 100 records. Then the LOW TAPE ALARM will come on again.

   C. NO RECORD WRITE ALARM will come on for one second and go off automatically when the main unit cannot write data records to the Kennedy Tape Recorder system.

FORM: DWT-21
FORM BY: CLARK
ASL 02/22/82

DWWSSN DRS TELEMETRY SYSTEM
OPERATIONAL PROCEDURES
REMOTE UNIT

1. Connect main 115 VAC system power cord into a 115 VAC power socket.

2. Turn on TOPAZ Backup Power Units.

3. Insure all AC power cords from individual system units are connected to the red 115 VAC power strips. The only exceptions are the TOPAZ units, and fan unit.

4. Turn on:

   A. Modem
   B. Intel microprocessor system
   C. Data Precision Constant Current Calibrator

5. Observe the Modem XMIT DATA light, CARRIER DETECT light, and RCV DATA light blinking pattern. The CARRIER DETECT light and RCV DATA lights mean the main unit is transmitting data to the remote unit. Constant CARRIER DETECT light means the main unit is connected via the telephone system to the remote unit. If the RCV DATA light is blinking it means the main unit is transmitting control data to the remote unit. If the XMIT DATA light is blinking it means the remote unit is transmitting data to the main unit. Note the difference between the blinking lights. This is because the main unit transmits four words per 50 millisecond data period (20 samples per second). The remote units transmit eleven words per 50 millisecond data period.

6. Calibration:

   A. Any ABORT CODE transmitted by the main unit will blink the remote CALIBRATOR DISPLAYS. This is an excellent way to test the main to remote telemetry link operation as well as the remote receive microprocessor (UP 3) and calibrator microprocessor (UP 5) and associated current calibrator.

   B. Any CALIBRATION CODE transmitted by the main unit will be visible as to type, level, period of calibration.

   C. Any ABORT CODE will immediately stop any calibration and reset the CALIBRATOR.

7. If the above steps are completed the remote unit is working.

DAILY DWWSSN DRS TIME CHECK AND CORRECTION PROCEDURE (SYSTRON DONNER)

1. Turn on WWV radio. Check Systron Donner Timing System, Model 8110 Digital Clock as per Time Lamp Synchronization Test, Scope Synchronization Test, or Standard Berkeley Time Check Test.

   A. Time Lamp Synchronization Test:

   Observe WWV lamp and ON TIME lamp. If a proper WWV time tick is present, the WWV lamp will be on during the WWV time tick. If the Systron Donner Timing System is within a few milliseconds, the ON TIME lamp will blink with the WWV signal. (See Synchronization Using ON TIME Lamp Procedures.) The ON TIME light will blink. If the ON TIME lamp is not blinking simultaneously with the WWV lamp, use the Scope Synchronization Test described below.

   B. Scope Synchronization Test:

   1) Connect the vertical input of the scope (0.5/div and 2 mS/div) to the TICK and PED BNC on the front panel of the unit.
   2) Observe the pedestal and tick on a common baseline.
   3) Measure the lead or lag time error. If error is greater than 50 milliseconds, reset the Systron Donner Timing System and log time correction.*

   NOTE: If time system is within 50 milliseconds do not reset until the magnetic tape is changed, then reset the Systron Donner Timing System and log time corrections.

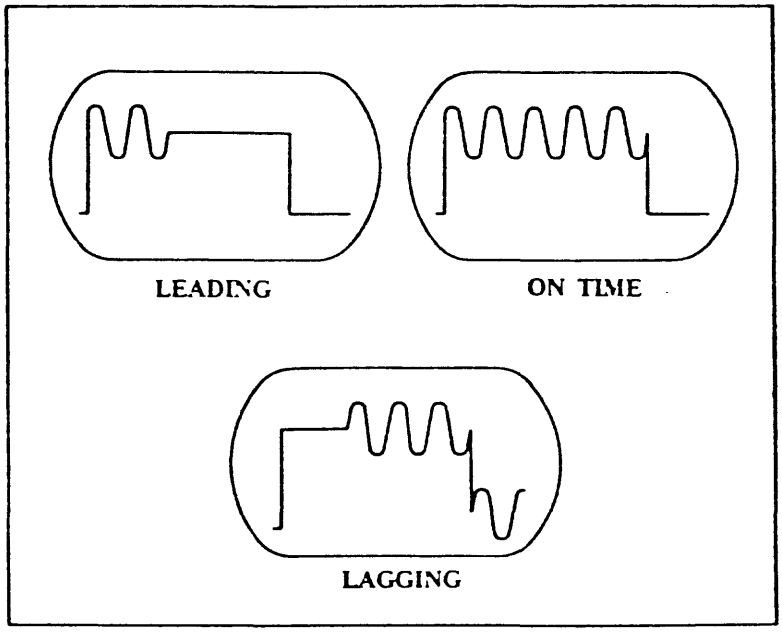


FIGURE 1 - TICK AND PEDESTAL

* Any uncertainty in the propagation delay time must be added to these figures.

2. During initial set-up or large timing errors, use the following procedures to set-up and operate the Systron Donner Timing System.

   A. Preset Time and Propagation Delay:

      1) Use the PRESET thumbwheel switches to set in desired start time.
      2) Use the PRESET/RESET toggle switch to enter data into the displays. In the RESET mode the display registers are to set to all zeros. In the PRESET mode, the data values of the thumbwheel switches are entered into the display registers.
      3) Use your choise of Manual Start, External Start, or WWV Start (see Systron Donner Manual, Option S11A External/WWV Synchronization).
      4) Check Timing System Synchronization by TIME lamp or SCOPE method. Adjust timing system for zero millisecond error. (See Systron Donner Manual, Option S11A External/WWV Synchronization.)

   B. Manual Start:

      1) Place MODE switch in HOLD position.
      2) Place START switch in MANUAL position.
      3) Preset time by thumbwheel switches to desired start time. Press PRESET switch. Desired start time is visible in displays.
      4) Listen to WWV and at place MODE switch to RUN position when you want the system to start.
      5) Use the TIME LAMP and/or SCOPE method of synchronization.

   C. Synchronization Using ON TIME Lamp:

      1) Position the PER SEC switch to 1 mS.
      2) Hold the ADV/RET switch in the RET position until the ON TIME lamp stops flashing.
      3) Hold the ADV/RET switch in the ADV position until the ON TIME lamp flashes and then stops flashing; note how many flashes this requires.
      4) Hold the ADV/RET switch in the RET position for 1/2 the number of flashes counted in this position less 2.
      5) Synchronization is now accurate to within +2mS*.

   D. Synchronization Using a Scope:

      1) Connect the vertical input of the scope (0.5/div and 2 mS/div) to the TICK and PED BNC on the front panel of the unit.
      2) Observe the pedestal and tick on a common baseline.
      3) Select a convenient rate on the PER SEC switch and, using the ADV/RET switch, superimpose the tick and pedestal as shown in Figure 1.
      4) Return the PER SEC switch to OFF.
      5) Synchronization is now accurate to within +100 mS*.

* Any uncertainty in the propagation delay time must be added to these figures.

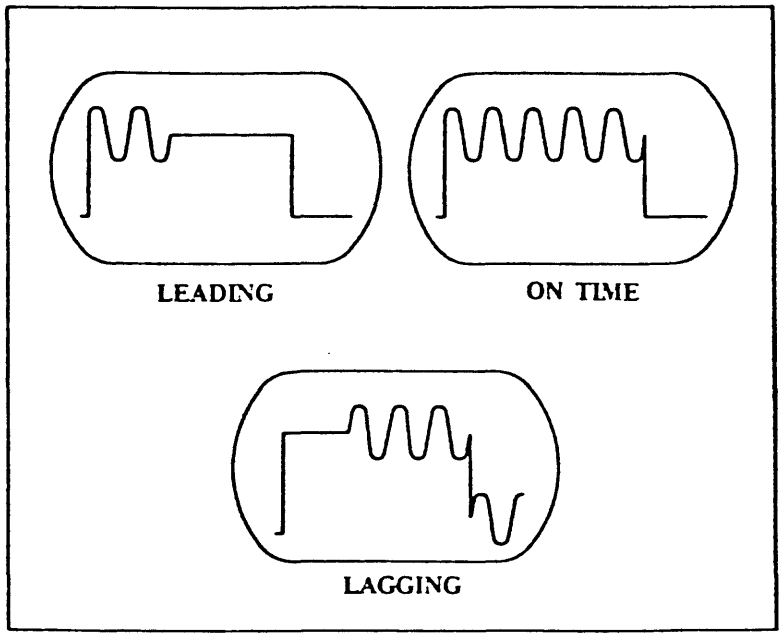


FIGURE 1 - TICK AND PEDESTAL

E. WWV Synchronization Start:

1) WWV Synchronization allows full synchronization of the clock or generator to radio stations WWV in Fort Collins, Colorado or WWVH in Puunene, Maui, Hawaii.
2) WWV Sync Input: Unit will detect the WWV (1 kHz) or WWVH (1.2 kHz) second ticks with a minimum input level of 0.5 Vrms.
3) Equipment Required:
   (A) WWV Receiver: Tick Output: 0.5 Vrms, minimum.
   (B) Oscilloscope: Vert: 0.5 V/div, 100 kHz bandwidth, minimum
   Horiz: 0.5 to 5 mS/div. (Oscilloscope required only when precision must be better than +3 mS.)
4) Setup:
   (A) Connect the Tick Output of the receiver to the "WWV IN" BNC on the rear of the Time Code Generator (TCG).
   (B) Adjust the Tick Output of the receiver for about 3V p-p (1.5 V p-p minimum). This will correspond to about 1 V p-p on the TICK and PED BNC.

5) Start-Up:
(A) Note that the TICK lamp is flashing one each second.
(B) Set the 3 PROPAGATION DELAY switches (XX.X ms) to the calculated time required for the signal to propagate from the transmitter to the receiver.
(C) Place the Mode switch in HOLD position.
(D) Momentarily position the START switch to MANUAL.
(E) Place the Mode switch in the STOP position for a minimum of 1 second.
(F) Position the Mode switch to HOLD.
(G) Make certain that a good clean tick signal is present; then position the START switch to AUTO and hold for 1 second.
(H) The unit is now synchronized to within +10 mS*. Synchronization using an ON TIME lamp or scope may be performed for greater accuracy.

F. External Synchronization Start:

1) The clock or generator is automatically started in sychronism with an external pulse. Starting accuracy to within 1 micro/sec can be expected exclusive of start pulse rise time delay. Controls are included for advancing or retarding the time base at precise rates to allow resynchronization without interruption of time accumulation.
2) External Start Pulse: A positive going level change of +4.5 V, minimum, for duration of not less than 5 micro/sec. Input impedance in 10 kΩ. Up to 50 V may be applied without damage.
3) Setup:

NOTE: The TICK and ON TIME lamps are not used in the EXT Start Mode.

(A) The propagation delay switches may be used if applicable; if not, set them to 00.0 ms.
(B) Position the Mode switch to STOP for 1 second, minimum.
(C) Method #1: Position the Mode switch to HOLD. Position the START switch to AUTO and hold it until the next pulse occurs. Preset desired start time as described elsewhere in this manual.
(D) Method #2: Preset the desired start time. Set the Mode switch to GEN or RUN. At some time before the start pulse will occur, position the START switch to AUTO and hold it there until after the start pulse has occurred.

The unit is now synchronized to within 1 micro/sec of the start pulse. The instrument may be started manually at any time by positioning the Mode switch to GEN or RUN and then momentarily positioning the START switch to MAN. The unit may first be preset if desired while the Mode switch is in STOP.

* Any uncertainty in the propagation delay time must be added to these figures.

DWWSSN DRS TELEMETRY PROGRAM
Thumbwheel Switch Settings

FORM: DWT-8
FORM BY: CLARK
ASL 02/22/82

Switch Position	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Switch T(Telemetry Test Value)	0	1	2	3	4	5	6	7	8	9	X don't use	X don't use	X don't use	X don't use	X don't use	X don't use
Switch B (SP event detection constants) KSP	2.67	3.20	2.46	3.20	3.56	2.46	3.05	3.56	2.46	2.91	3.20	3.56	2.29	2.67	3.20	4.00
STA SP	16	16	8	8	8	8	8	8	16	16	16	16	32	32	32	32
LTA SP	64	64	64	64	64	128	128	128	128	128	128	128	128	128	128	128
Switch C (IP event detection constants)	100	200	300	400	500	600	700	800	900	1000	1600	2200	2800	3600	4200	4800
Switch D (Re-	SP Ev.* / IP Ev.* / All LP	All SP / No IP / All LP	No SP / All IP / All LP	All SP / All IP / All LP	No SP / IP Ev.* / All LP	SP Ev.* / No IP / All LP	--Continuous LP only(no SP, no IP)----------								End of File Mark	

Note: SP off limit = 10 minutes, SP on limit = 30 minutes.

IP off limit = 12 minutes.

*"SP Ev." means only SP events, not continuous SP data, are recorded. (Same meaning for "IP Ev.")