

UNITED STATES DEPARTMENT OF THE INTERIOR
GEOLOGICAL SURVEY

AUTOMATIC REZEROING CIRCUIT FOR
BORE-HOLE STRAINMETER

by

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Open-File Report No. 86-190

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AUTOMATIC REZEROING CIRCUIT FOR BORE-HOLE STRAINMETER

1. ABSTRACT

An electronic circuit has been designed to automatically rezero bore-hole volumetric strainmeters operated by the U. S. Geological Survey. The auto-rezero (AR) circuit operates on ± 12 VDC at ~ 80 mW. The AR circuit consists of two threshold monitoring comparator circuits. The first circuit monitors the high gain output from the strainmeter and when the output exceeds a preset threshold the circuit will automatically open and close an electronic valve in the strainmeter causing a release of built up pressure which rezeros the output. The threshold must be exceeded for the duration of a programmable time period between 16 seconds and 68 minutes before the strainmeter will be rezeroed. The second comparator circuit monitors the unity gain output from the strainmeter to provide a fail safe against physical damage from events with periods less than the time delay of the amplified section. This circuit will rezero the strainmeter after the threshold is exceeded for a programmable period of milliseconds. The rezeroing is accomplished using relay closures making the circuit versatile with respect to voltage requirements and for other applications.

2. INTRODUCTION

The U. S. Geological Survey (U.S.G.S.) operates bore-hole volumetric strainmeters along the San Andreas Fault in an effort to detect strain changes associated with earthquake activity (Johnston, et. al., 1986) The strainmeters have a finite range and must be rezeroed periodically to remain within the range of telemetry and to prevent physically damaging the instrument. Rezeroing these instruments required personnel to travel to the sites and manually rezero the instruments. The auto-rezero (AR) circuit has been designed to eliminated the manual rezeros and will rezero the strainmeters when a predetermined value is exceeded. The strainmeters are rezeroed by opening and closing an electronically controlled valve.

3. THEORY

If high amplitude strain signals at seismic frequencies are to be detected the AR circuit should not trigger on these signals, but still trigger before any physical damage occurs to the instrument. To achieve this protection two pair of comparators were used in the design of the AR circuit.

One pair of comparators are designed to monitor the highest gain channel and trigger at a threshold determined by the telemetry system used. The comparator outputs are connected to a programmable time delay circuit and the threshold voltage must be exceeded for the duration of this programmed time before the valve in the strainmeter is opened. After opening the valve, another identical time delay is used to control closing the valve. This high gain section will control the majority of rezeros.

The second pair of comparators are designed as a fail safe to protect the instrument from physical damage and will protect the strainmeter from high amplitude signals at periods less than the time delay programmed for the amplified gain section. This pair of comparators monitor the unity gain channel and the outputs are connected to the valve opening section via a programmable time delay circuit which is designed for noise immunity. The process for closing the valve is the same as mentioned above.

Different model instruments require different voltages to open and close the valves. The AR circuit does not provide the voltage, but provides two DPDT, one ampere, relay closures. The two relays, one to open and the other to close the valve, enable different voltages to be applied to different model strainmeters. The relays also allow the AR circuit to be used for any application where analog inputs are used to control external devices. Figure 1 is a block diagram of the AR circuit.

4. DESIGN

High impedance on the inputs to the AR circuit insure the signals from the strainmeter are not loaded. Both inputs to the AR circuit have a voltage follower or buffer in front of the comparators. The voltage follower used is an OP-07 operational amplifier, but any pin compatible operational amplifier or buffer will work. Refer to schematic in appendix I.

Both pairs of comparators are designed using a single LM139A low power quad comparator. Each comparator pair is designed with a negative and positive threshold with a minimum of 0.15 VDC of hysteresis. The outputs from each comparator have a diode (1N914) to ground, preventing any negative transition which allows compatibility with the digital CMOS circuitry.

The unity gain comparator section is designed to prevent damage to the strainmeters from large high frequency strain events. The comparators are set to trigger a rezero if the input is greater than 1.8 VDC or less than -1.8 VDC. These threshold voltages can be monitored at pins 11 and 16, on the LM139A, respectively. The outputs from the comparators are run through a NAND gate (4093) so if either goes low a high will activate the time delay circuitry. The unity gain section will normally never be activated, due to the thresholds of the amplified gain section.

The amplified gain section is identical to the unity gain, but the threshold levels are adjusted to match the range of the telemetry system used. Telephone line telemetry systems use thresholds of 4.8 and - 4.8 VDC, while the satellite telemetry systems use thresholds of 9.5 and - 9.5 VDC. These threshold voltages can be monitored at pins 15 and 16 on the LM139A, respectively. The outputs from the comparators are run through a NAND gate (4093) so if either goes low a high will activate the time delay circuitry. The amplified gain section will monitor the strainmeter output with the highest gain and will keep the strainmeter output from exceeding the range of the telemetry system.

After either the unity or the amplified gain comparators are exceeded a programmable time delay section is activated prior to opening the strainmeter valve. The unity time delay section can be programmed for delays between 1-255 milliseconds. The amplified time delay section can be programmed for delays between 16 seconds and 68 minutes. Standard settings are one minute for the amplified and 5-10 milliseconds for the unity. The delay on the unity section is designed to prevent any noise spikes from causing the valve to open and the delay on the amplified section is to prevent large seismic events from causing the valve to open. Both delay sections use a divide-by-N counter (40103) which can be programmed to divide by 1 to 255. The reference frequencies for the time delay sections are from the clock section.

The clock section consists of a counter/divider (4020) and an oscillator/divider (4060). The RC oscillator of the 4060 is adjusted (R1) to 16.4 KHz. This provides a 1 KHz output on pin 7 and a 4 Hz output on pin 1 of the 4060. The 4 Hz output is divided by the 4020 to provide a 0.067 Hz (16 second period) output on pin 4. The 1 KHz and 0.067 Hz frequencies are used as clock frequencies for the unity and amplified time delay sections. The 4 Hz frequency is used in the valve opening and closing sections.

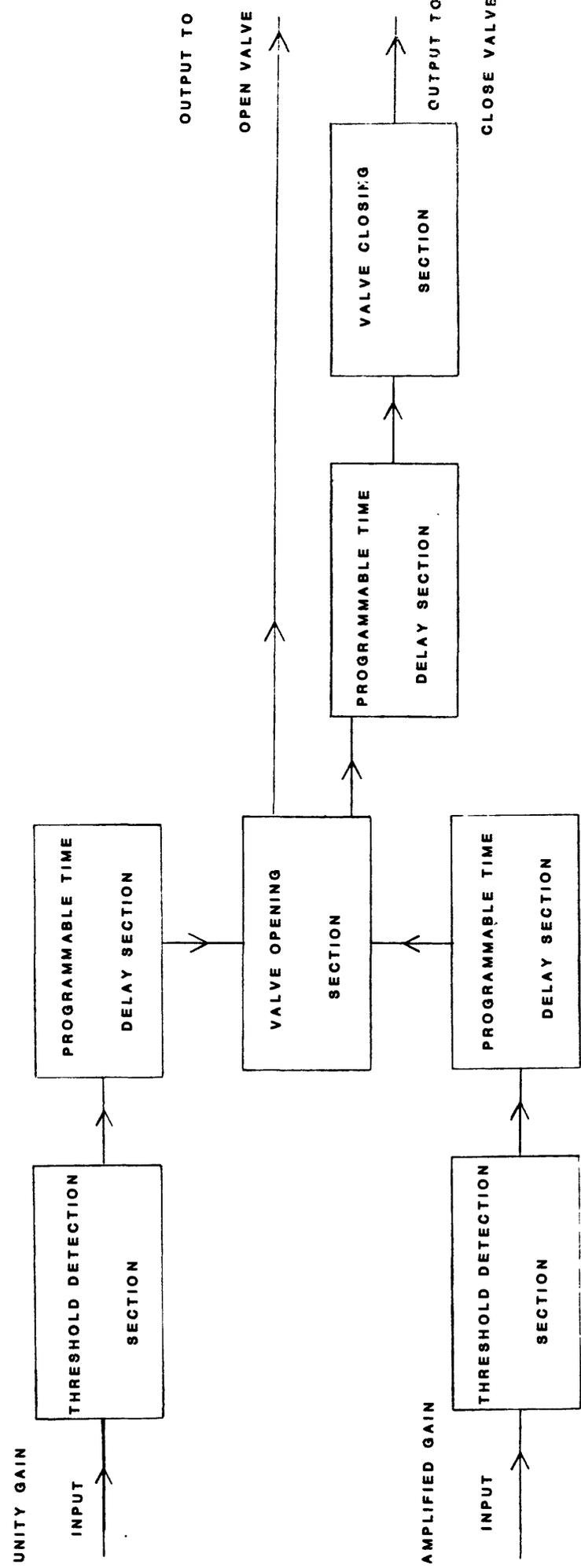


FIGURE 1. Block diagram of automatic zeroing circuit for U. S. G. S. bore hole strainmeter

If either comparator section exceeds its threshold for the duration of the programmed time delay, then the valve opening section is activated. The valve opening section is activated when the output from either 40103 counter sets a J-K flip flop (4027) which enables a counter (4520). The first positive transition from the 4 Hz reference frequency clocks the 4520 which drives a darlington (MPSA14) and a power transistor (MJE1090). The transistor powers the relay (Teledyne 732D) which provides the voltage to open the strainmeter valve and release the built up pressure. The second positive transition from the 4 Hz reference frequency resets the valve opening circuitry and activates the valve closing section.

The valve closing section has a time delay identical to those discussed above. The reset pulse from the 4520 in the valve opening section sets a J-K flip flop (4027) which enables a divide-by-N counter (40103). The counter can be programmed for a time delay between 16 seconds and 68 minutes and the standard setting is one minute. After the time delay, the output of the counter enables a counter (4520). The first positive transition from the 4 Hz reference frequency clocks the 4520 which drives a darlington (MPSA14) and a power transistor (MJE1090). The transistor powers the relay (Teledyne 732D) which provides the voltage to close the strainmeter valve. The second positive transition from the 4 Hz reference frequency resets the valve closing circuitry and completes the rezeroing process.

To prevent the digital electronics from attaining a random state when the circuit is powered, a schmitt trigger gate (4093) and a RC are used to reset the digital circuits upon powering the board.

5. SET-UP PROCEDURES

1) Adjusting threshold values for the unity gain section

Ground the amplified input, put a variable voltage source into the unity gain input, adjust resistance of R34 and R35 for the negative value (TP1) and adjust resistance of R22 and R23 for the positive value (TP2) until output at pin 11 (TP3) of the 4093 (UN08D) goes high at -1.8 and +1.8 volts. Check to insure there is a minimum of 0.15 volts of hysteresis by adjusting R25 and R30.

2) Adjusting threshold values for the amplified gain section

Ground the unity input, put a variable voltage source into the amplified gain input, adjust resistance of R18 and R19 for the negative value (TP4) and adjust resistance of R8 and R9 for the positive value (TP5) until output at pin 10 (TP6) of the 4093 (UN08C) goes high at -4.8 and +4.8 volts. Check to insure there is a minimum of 0.15 volts of hysteresis by adjusting R11 and R44.

3) Adjusting clock reference frequencies

Adjust R1 until the frequency at pin 9 of the 4060 (UN01) equals ≈ 16.4 KHz. The output at pin 7 (TP21) should be ≈ 1 KHz, the output at pin 1 (TP18) should be ≈ 4 Hz, and the output of pin 4 (TP19) of the 4020 (UN02) should have a period of ≈ 16 seconds. The accuracy of these frequencies is not critical, but the 16.4 KHz output should be adjusted to within 5%. If different ranges for the time delays are required the frequency can be adjusted as needed.

4) Time delay for amplified section

Exceed the threshold value of the amplified gain input while monitoring pin 6 (TP7) of the 4093 (UN08B) to insure the output goes low after the programmed time delay. The reference clock and the signal which exceeds the threshold are not in phase and can cause the programmed delay to be plus a fraction of one cycle of the reference frequency (≈ 16 seconds). For a one

minute delay the rotary switch is set to 4 and the delay should be between 64 and 80 seconds after the threshold is exceeded.

5)Time delay for unity section

After grounding the amplified input. Exceed the threshold value of the unity gain input while monitoring pin 7 (TP20) of the 4093 (UN08B) to insure the output goes low after the programmed time delay. A scope will have to be used because the output will be low for only 1 msec. every 6-11 msec. depending on the programmed time delay.

6)Valve opening section

Check test points 10, 11, and the relay closure to insure the valve opening section is operational. All the check points will go high for ≈ 250 milliseconds. Check pin 1 of the 4027 (UN10A) and pin 15 (TP18) of the 4027 (UN10B) to insure the reset is operational. Pin 1 goes low and pin 15 goes high after the 250 milliseconds pulse which opens the valve.

7)Valve closing time delay section

Check the output at pin 14 & 15 (TP14) of the 40103 (UN11) to insure it goes low after the programmed time delay. The delay can be a fraction of one cycle more than indicated by the rotary switch.

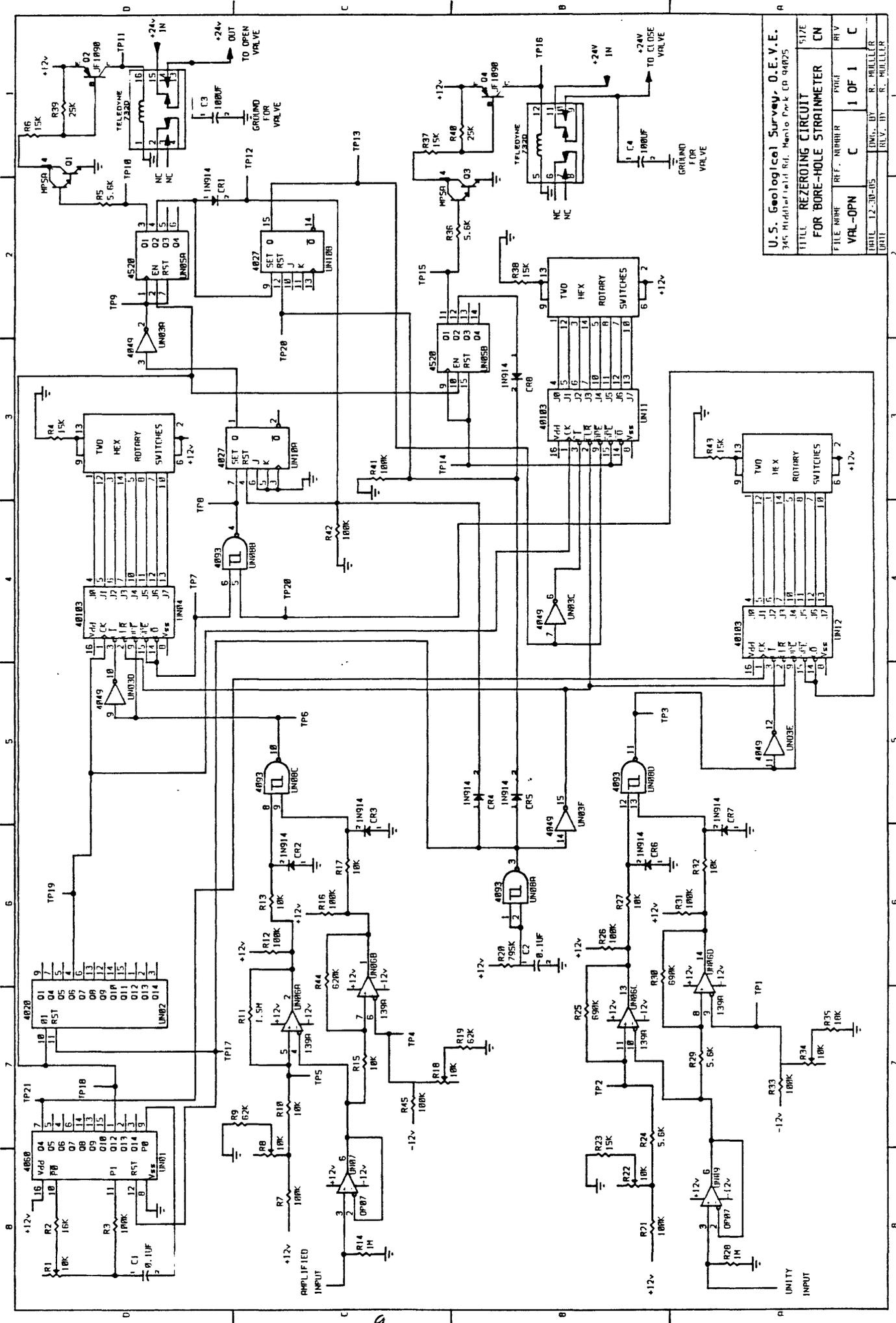
8)Valve closing section

Check test points 15, 16, and the relay closure to insure the valve closing section is operational. All the check points will go high for ≈ 250 milliseconds. Check pin 15 (TP13) of the 4027 (UN10B) to insure it goes low which resets the circuit.

REFERENCES

Johnston, M. J. S., Borchardt, R. D., and Linde, A. T., Short
Period Strain (0.1-1000s): Near Source Strain Field
For Earthquake (M=3.2) Near San Juan Bautista, Calif-
ornia, J. G. R., 1986, submitted

APPENDIX I



U.S. Geological Survey, D.E.V.E.	
745 Middlefield Rd., Menlo Park, CA 94025	
TITLE REZERGING CIRCUIT	
FILE NAME	517E
REF. NUMBER	FIG. 1
VAL-OPN	C
VAL-CLOSE	1 OF 1
REV. BY	R. MULLER
DATE	12-30-05
DRN	R. MULLER

APPENDIX II

Test Points For AR Circuit

- TP1 negative reference voltage for unity comparator
- TP2 positive reference voltage for unity comparator
- TP3 positive transition when unity comparator is exceeded
- TP4 negative reference voltage for amplified comparator
- TP5 positive reference voltage for amplified comparator
- TP6 positive transition when amplified comparator is exceeded
- TP7 negative transition for one clock period when amplified comparator is exceeded for a period greater than the programmed time delay
- TP8 positive transition when amplified comparator is exceeded for a period greater than the programmed time delay.
- TP9 negative transition to control opening the valve
- TP10 positive transition (~250 msec. duration) to open valve.
- TP11 +12 VDC applied to relay for opening valve
- TP12 short (nanoseconds) reset pulse for valve opening circuit and starts valve closing process
- TP13 positive transition to start valve closing procedure
- TP14 negative transition for one clock period to control closing the valve
- TP15 positive transition (~250 msec.duration) to close the valve.
- TP16 +12 VDC applied to relay for closing the valve
- TP17 positive reset pulse on powering up the circuit
- TP18 ~4 Hz clock output (~250 msec. period) used for timing valve opening and closing
- TP19 ~0.0625 Hz clock output (~16 sec. period) used for time delay of counter for the amplified channel and valve closure
- TP20 positive transition when unity comparator is exceeded for a period greater than the programmed time delay.
- TP21 ~1 KHz clock output (~1 msec. period) used for time delay of counter for the unity channel

APPENDIX III

Parts List For AR Circuit

INTEGRATED CIRCUITS

UN01	CD4060BE	RCA
UN02	CD4020BE	RCA
UN03	CD4049UBE	RCA
UN04	CD40103BE	RCA
UN05	CD4520BE	RCA
UN06	LM139AN	SIGNETICS
UN07	OP-07	PRECISION MONOLITHIC
UN08	CD4093BE	RCA
UN09	OP-07	PRECISION MONOLITHIC
UN10	CD4027BE	RCA
UN11	CD40103BE	RCA
UN12	CD40103BE	RCA

CAPACITORS

C1	0.1 μ F	25VDC	N/A
C2	0.1 μ F	25VDC	N/A
C3	100 μ F	50VDC	SPRAGUE , TVA-1310
C4	100 μ F	50VDC	SPRAGUE , TVA-1310

DIODES

CR1-CR8	1N914	N/A
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RELAYS	732D , DPDT	TELEDYNE
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TRANSISTORS

Q1	MPSA14	MOTOROLA
Q2	MJE1090	MOTOROLA
Q3	MPSA14	MOTOROLA
Q4	MJE1090	MOTOROLA

RESISTORS

R1	10K	POT	OPTIONAL
R2	16K		ALL RESISTORS 1/4 watt , 5%
R3	100K		
R4	15K		
R5	5.6K		
R6	15K		
R7	100K		
R8	10K	POT	OPTIONAL
R9	62K		
R10	10K		
R11	1.5M		
R12	100K		
R13	10K		
R14	1M		

R15	10K		
R16	100K		
R17	10K		
R18	10K	POT	
R19	62K		
R20	795K		
R21	100K		
R22	10K	POT	OPTIONAL
R23	15K		
R24	5.6K		
R25	795K		
R26	100K		
R27	10K		
R28	1M		
R29	5.6K		
R30	690K		
R31	100K		
R32	10K		
R33	100K		
R34	10K	POT	
R35	18K		
R36	5.6K		
R37	15K		
R38	15K		
R39	25K		
R40	25K		
R41	100K		
R42	100K		
R43	15K		
R44	620K		
R45	100K		