UNITED STATES DEPARTMENT OF THE INTERIOR

GEOLOGICAL SURVEY

Circuitry of the U. S. G. S. Telluric Profiler

by

Robert L. Seeley

Donald B. Hoover

and

Charles L. Tippens

Open File Report 87-332

1987

Table of Contents

INTRODUCTION

The electronic circuitry for the telluric profiling receiver described in this paper has evolved over the past ten years from the work of a number of U.S.G.S. employees. The first telluric profiler built and used by the U.S.G.S. was developed from a system described by Byer(1977). Details of the U.S.G.S. circuitry were described by Rohret and others (1975). This was a low frequency system operating near 0.033 Hertz which used a small x-y recorder for readout of data.

A multi-frequency system was next developed with a digital readout covering the frequency range of 0.0167 to 25 Hz in fourteen steps. This system was built to evaluate the use of multiple frequencies and to improve the reliability of the readout. The new digital readout proved particularly useful for displaying results from higher frequency signals which derive primarily from spherics. Using these higher frequencies proved to be quite effective for rapid reconnaisance surveying.

The receiver described in this paper was developed based upon the experience gained from these earlier systems. A new design incorporated the digital readout features of the previous telluric profiling receiver with a selection of frequencies in the audio-magnetotelluric (AMT) band (ie about 7 Hz to 20 kHz). The analog circuits used in this design follow very closely the circuits used in the U.S.G.S. audio-magnetotelluric 5 channel receiver which has been extensively field checked. This new instrument, although specifically designed as a telluric profiler, may be used as a two channel scalar AMT receiver with the addition of a magnetic field sensor.

GENERAL DESCRIPTION

The Telluric Profiler is a portable, two channel receiver that indicates the amplitudes of the two received signals as well as the agreement between the channels as received and when one of the channels has been phase shifted. As shown in the block diagram in figure 1, the receiver contains high gain (up to 130 dB of selectable gain), low noise (below 10 nanovolt input levels) amplifiers, selectable band pass filters, fixed notch filters, precision (full wave) rectifiers, and integrators with selectable time constants. Analog multipliers are used to determine the in phase and quadrature phase agreement between the two channels. Integrated voltages representing the two channels (A and B), the in phase (A*B), and the quadrature (QUAD) signals are sampled and held for analog-to-digital conversion and liquid crystal display(LCD). Sampling is initiated when input signals exceed a threshold value selected by the operator. Low power integrated circuitry and LCDs enable operation of the profiler for six hours without recharging its batteries.

Funtional Description

As indicated in the system block diagram (figure 1) and the receiver gain distribution diagram (figure 2), the input signals are received, amplified, filtered, rectified, and integrated from two different channels (A and B). The in-phase and quadrature relations between the channels are determined before the incoming signals are rectified and integrated. A comparator is adjusted by the operator in the field to trigger the sample and hold (S/H) circuitry on large incoming signals. Analog-to-digital (A/D) converters digitize the "held" signals and supply four liquid crystal displays (LCDs) with data for displaying the respective amplitudes of A, B, in-phase (A*B), and quadrature (QUAD) signals. A fifth LCD displays overload conditions detected when analog voltages exceed preset limits for the input amplifiers, the band pass filters, or the analog multipliers used to obtain A*B and quadrature signals. Unsafe battery conditions are also displayed on the fifth LCD. When desired, a Mode switch connects the two input channels to a precision spectrum signal generator for calibrating the system or shorts the inputs (to ground) for quickly checking that the self noise generated by the system is low.

As shown in figure 2, the receivers possess up to 84 dB of selectable gain and several band pass and notch filters. The band pass filters select one of 16 different center frequencies (2.7, 4.5, 7.5, and 14 Hz multiplied by either 1, 10, 100, or 1000). The eight notch filters remove 60 Hz and its harmonics caused by power line interference. After amplification and filtering, the signals are high pass (above 1.6 Hz.) filtered to eliminate d.c. offset; full wave, precision rectified; and then integrated over one of eight possible time periods (.01, .03, .1, .3, 1, 3, 10, or 30 seconds). These signals are externally available at banana plugs for strip-chart recording and drive panel meters for immediate display. Both outputs enable the operator to determine if data are "good" by observing the rise and fall time, coherency, and amplitudes of incoming signals visually. The integrated signals are then sampled and displayed in one of three possible ways (peak, free, or slow).

Figures 3 and 4 show the input circuitry used on boards 1 (for channel A) and 3 (for channel B). Each channel has a 24 dB buffer/amplifier to insure that signal amplitude is above the receiver noise floor and a selectable 0-24 dB attenuator to prevent overload for large input signals. These amplifier/attenuators are immediately followed by another (0 dB) buffer and the first of three band pass filters. The band pass filter frequencies and Qs are selected by resistors connected by analog switches (HI-201-5s) and controlled by lines (MS1234 and FS1234) from the front panel frequency and frequency multiplier switches. The frequency and Q are also selected by capacitors connected by field effect transistors and controlled by lines (MSJ1234) from the front panel frequency multiplier switches. Q is the ratio of the center frequency of the band pass filter to its bandwidth (the difference in frequencies between the -3 dB points on the amplitude response curve). Following the first band pass filter is a 0 or 18 dB amplifier used to keep signal amplitudes in the appropriate range of operation for the second band pass filter and the first four of eight notch filters (shown in figure 4). Note that order of notch filter frequencies has been set to eliminate the largest expected interference amplitudes first. This order (ie. fundamental, then 3rd harmonic, then 2nd harmonic, etc.) prevents saturation in subsequent filters and enables the maximum dynamic range of signal amplitude.

Figures 5 and 6 show the remaining four notch filters, the third band pass filter, the high pass (d.c. restoration) filter, the precision rectifier, the integrator, and meter driver circuitry duplicated on boards 2 (channel A) and 4 (channel B). Following the four notch filters is a 0 to 42 dB amplifier that selects gain in steps of 6 dB from the front panel (switch GS12345678), and the third band pass filter which is controlled in the same way as the first two band pass filters. The high pass filter has a cutoff frequency (1.6 Hz) which is lower than the lowest selectable band pass center frequency (2.7 Hz) and removes d.c. signals caused by operational amplifier offsets which would cause errors when the signal is rectified and integrated. The integration time constant is selected by a front panel switch which connects one of eight resistors to charge a single 20 microfarad capacitor. A high input impedence operational amplifier (OP-05) buffers the integrated voltage to the externally connected banana plugs providing signal to a strip chart recorder and a driver for meters on the front panel of the receiver.

Figure 7 shows the front panel switches that select the band pass filter center frequencies and Q, the 0 to 42 dB amplifier's gain, and the precision spectrum generator's signal amplitude. Figures 8 and 9 are schematics for the operator threshold adjustment to control the sampling of output signals, and the phase shift (to get quadrature components) and in-phase analog multiplier sections. The multipliers (AD534s) supply signal to the A*B and quad integrators irrespective of the polarity of the input signals.

The phase shift for the quadrature multiplier is changed to match the band pass filter's center frequency (using FS1234 and MSJ1234). The integration times are selected by analog switches (HI-201-5s) and controlled (TC12345678) by the same switch that selects the integration time for channels A and B (fig.6).

Figure 10 is a schematic of the sample and hold mode controlled by a front panel 3 position switch (peak-free-slow), the battery low detection circuitry, and the overflow display logic to drive the Error LCD and overload buzzer. Also shown are the voltage regulators used to drop battery voltages to safe levels for the use of the digital logic and LCD devices.

Figure 11 shows the connection of one of four analog-to-digital converters used to digitize and display the digital values of the amplitude of the A, B, A*B (in phase) and A*B (quadrature) signals. Decimal points are connected on the LCDs so that normal data has the range of 0.000 to 1.999 and overloads cause 0.0.0.0 to 1.9.9.9 to appear.

Figure 12 is the schematic for the precision spectrum generator board (#7). The precise spectrum is generated by reading data stored in a read-only-memory (ROM) at speeds dependent upon the frequency band selected (using FS1234 and MS1234) on the front panel. Switches (HI-201-5s) controlled by the frequency selection switch signals (FS1234 and MS1234) divide a high frequency (140 kHz) clock rate down and update the address register controlling the ROM to match output data rates with the filter frequency being used. The data stored in the ROM is a signal having precisely known broad band spectral characteristics as computed using an inverse Fourier transform. The phase of each spectral line is computed to vary randomly to provide even distribution of energy from the calibrator over the period of repetition of reading through the ROM. Appendix I is a listing of the hexadecimal values stored in the ROM to generate the precisely controlled spectrum. Additional details of the "precision spectrum generator" were disclosed in a patent application by Cooke, Watts, and Seeley(1982).

Figure 13 is the layout of connectors, switches, potentiometers, LCDs, and meters used for the front panel. Generally, signal flows from left to right and adjustments, displays, and outputs are in that order. The wiring connections between the seven boards needed for this system's operation are listed in Appendix II.

ACKNOWLEDGEMENTS

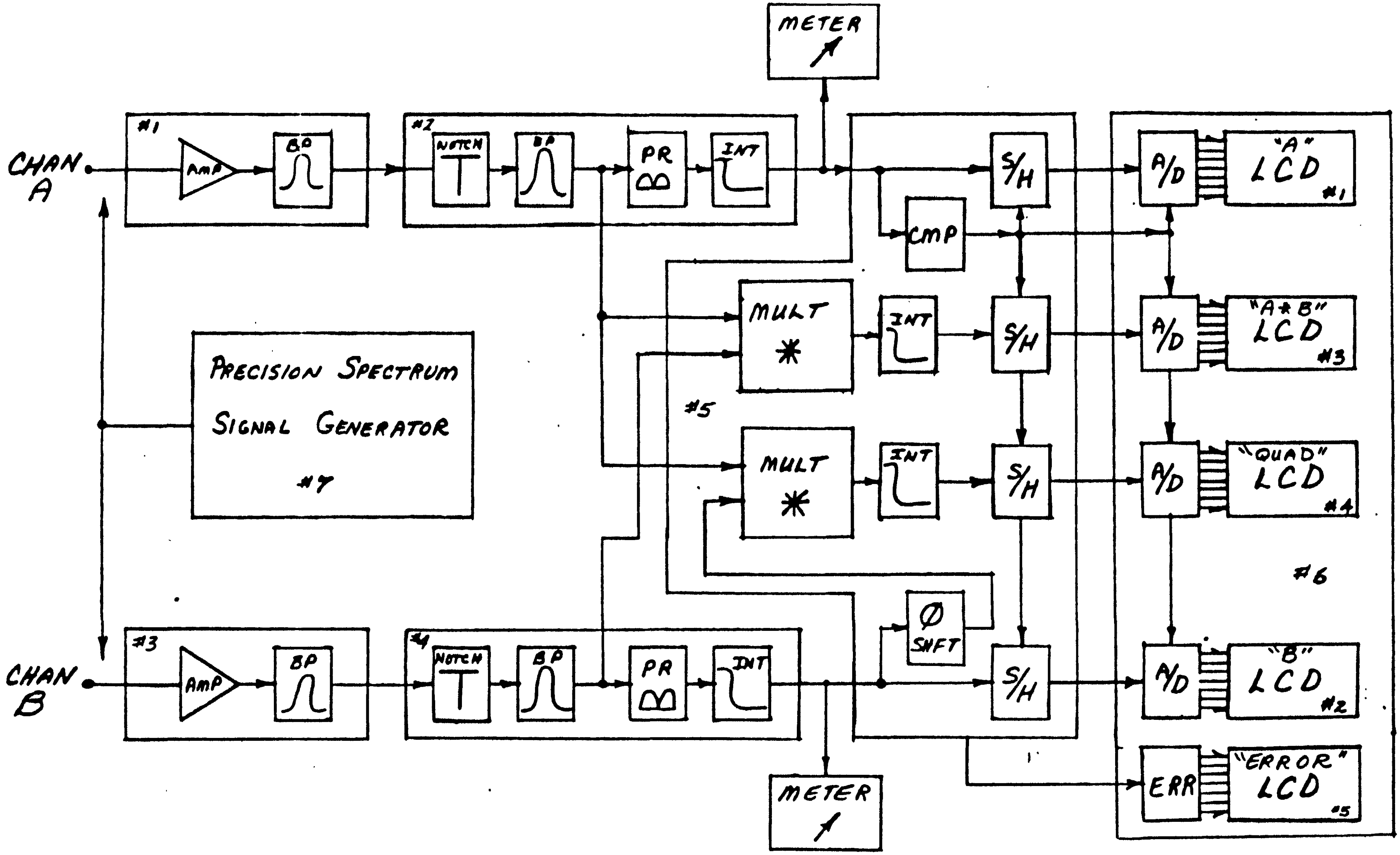
The electronic circuitry herein described has evolved over several years from the work of many U.S.G.S. employees. Frank Frischknecht, Roger Lescelius, and Donald Rohret first developed a telluric system and published (1975) schematics. That system was improved by Donald Hoover and Charles Tippens. Recent additions have included variable state filters by James Cook, a low noise amplifier/filter layout by Tippens, digitizing integrated voltages, error detection, display using a liquid crystal display (LCD), and a precision spectrum calibration signal generator.

References

Cooke, J.E., Watts, R.D., and Seeley, R.L., report of invention "precision spectrum generator", memo: Br. of Electromagnetism and Geomagnetism to Admin. Office, U.S. Dept. of Interior, 1982.

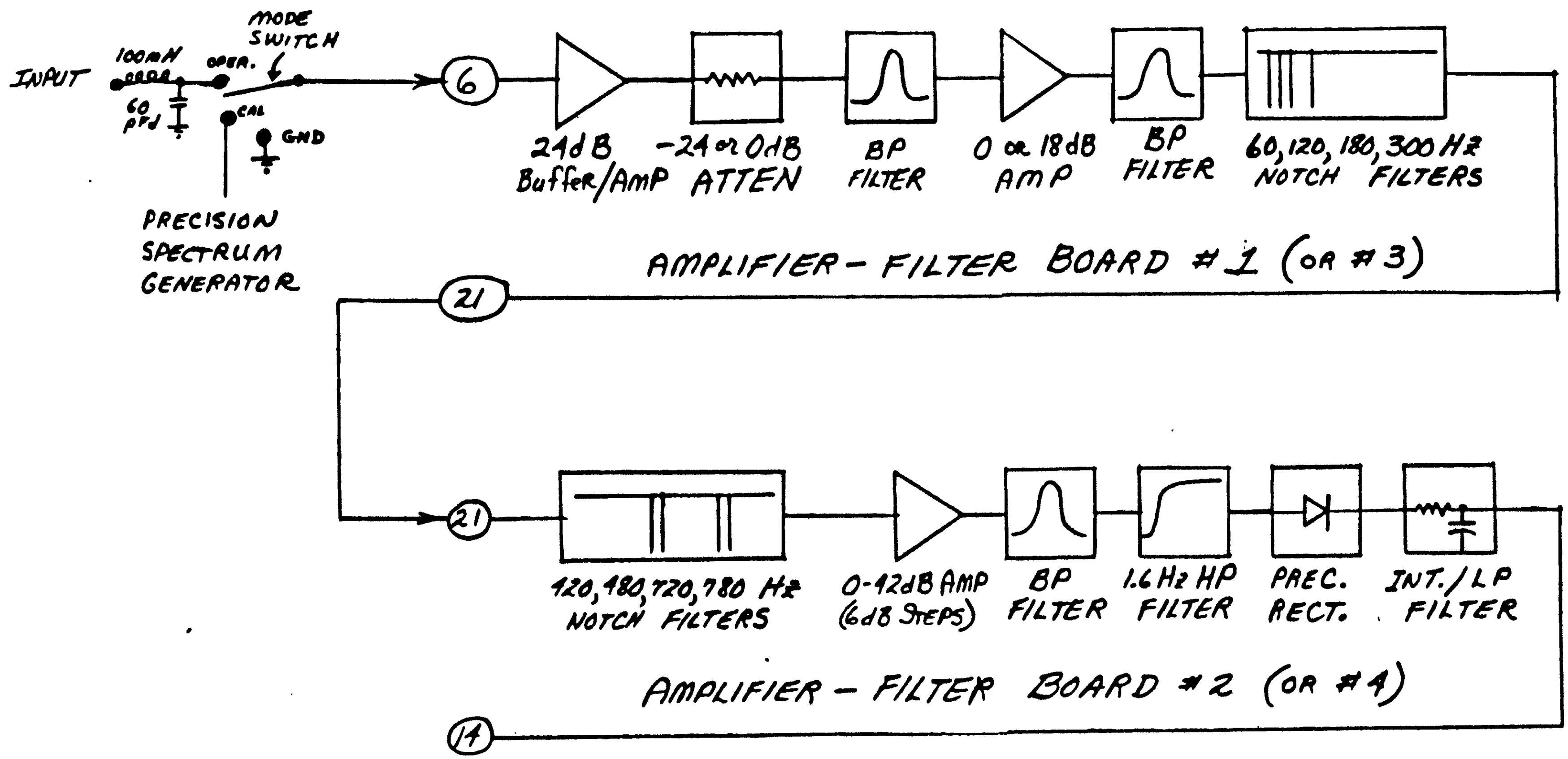
Beyer, J.H., 1977, Telluric and D.C. resistivity techniques applied to the geophysical investigations of Basin and Range geothermal systems Part III: Laurence Berkeley Lab. Univ. of Calif. Report LBL-6325 3/3.

Rohret, Donald H., Lescelius, Roger H., and Frischknecht, Frank C. - Schematic diagrams and parts list for portable telluric current profiler, Open File Report 75-641, 1975.



BLOCK DIAGRAM – TELLURIC PROFILER

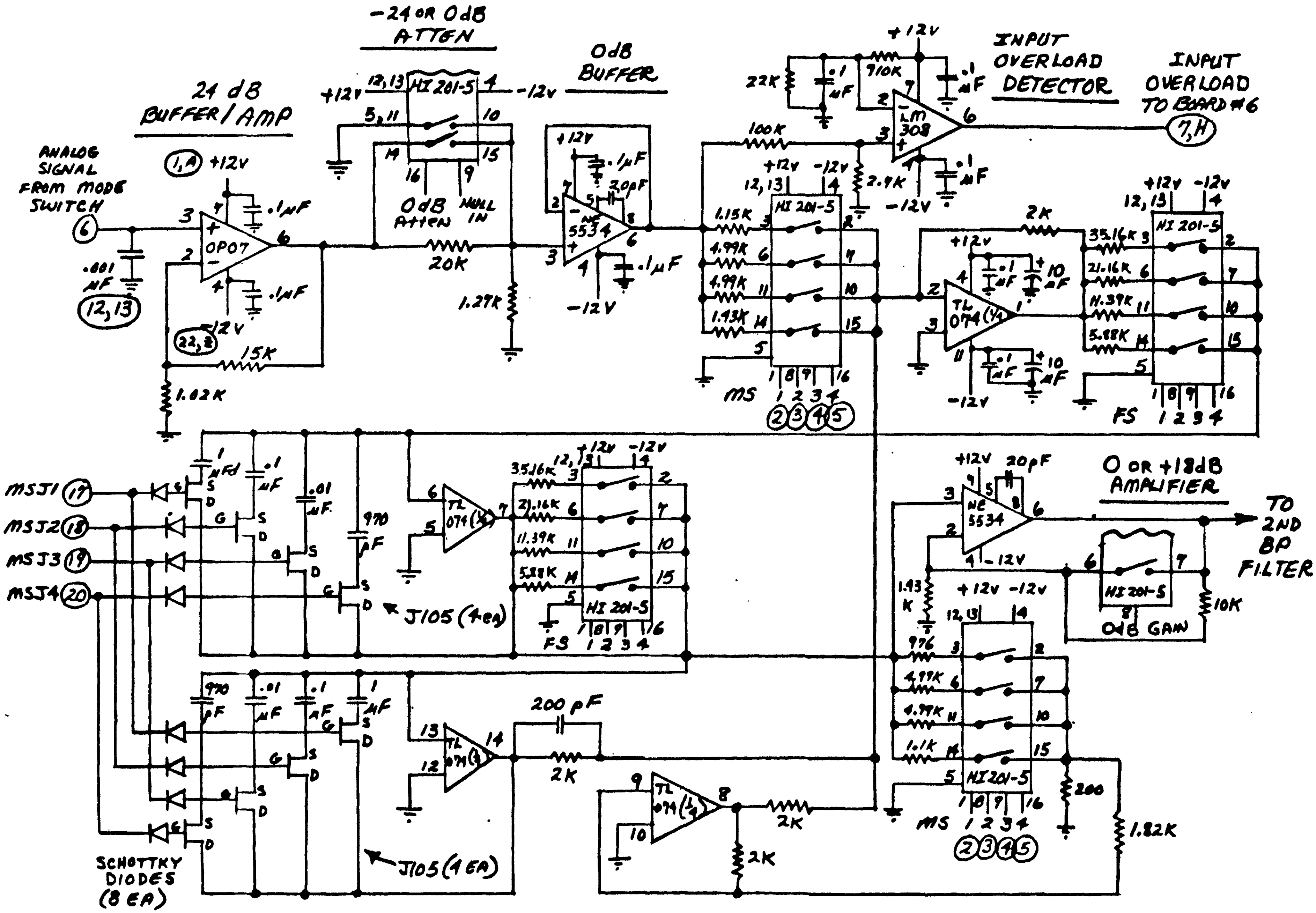
R.L. SEELEY
3 APRIL 1985



GAIN SWITCH POSITION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
-24dB, 0dB ATTEN	-24	-24	-24	-24	0	0	0	0	0	0	0	0	0	0	0	⏚
0dB, +18dB AMP	0	0	0	0	0	0	0	0	+18	+18	+18	+18	+18	+18	+18	0
0 to 42dB AMP	0	+6	+12	+18	0	+6	+12	+18	+6	+12	+18	+24	+30	+36	+42	0
TOTAL VARIABLE GAIN	-24	-18	-12	-6	0	+6	+12	+18	+24	+30	+36	+42	+48	+54	+60	0
BUFFER AMP. GAIN	+24	+24	+24	+24	+24	+24	+24	+24	+24	+24	+24	+24	+24	+24	+24	—
SELECTABLE GAIN (dB)	0	+6	+12	+18	+24	+30	+36	+42	+48	+54	+60	+66	+72	+78	+84	NULL

BLOCK DIAGRAM AND GAIN DISTRIBUTION OF AMPLIFIER - FILTERS FOR THE TELLURIC PROFILING SYSTEM

R.L. Seeley 11AUG86

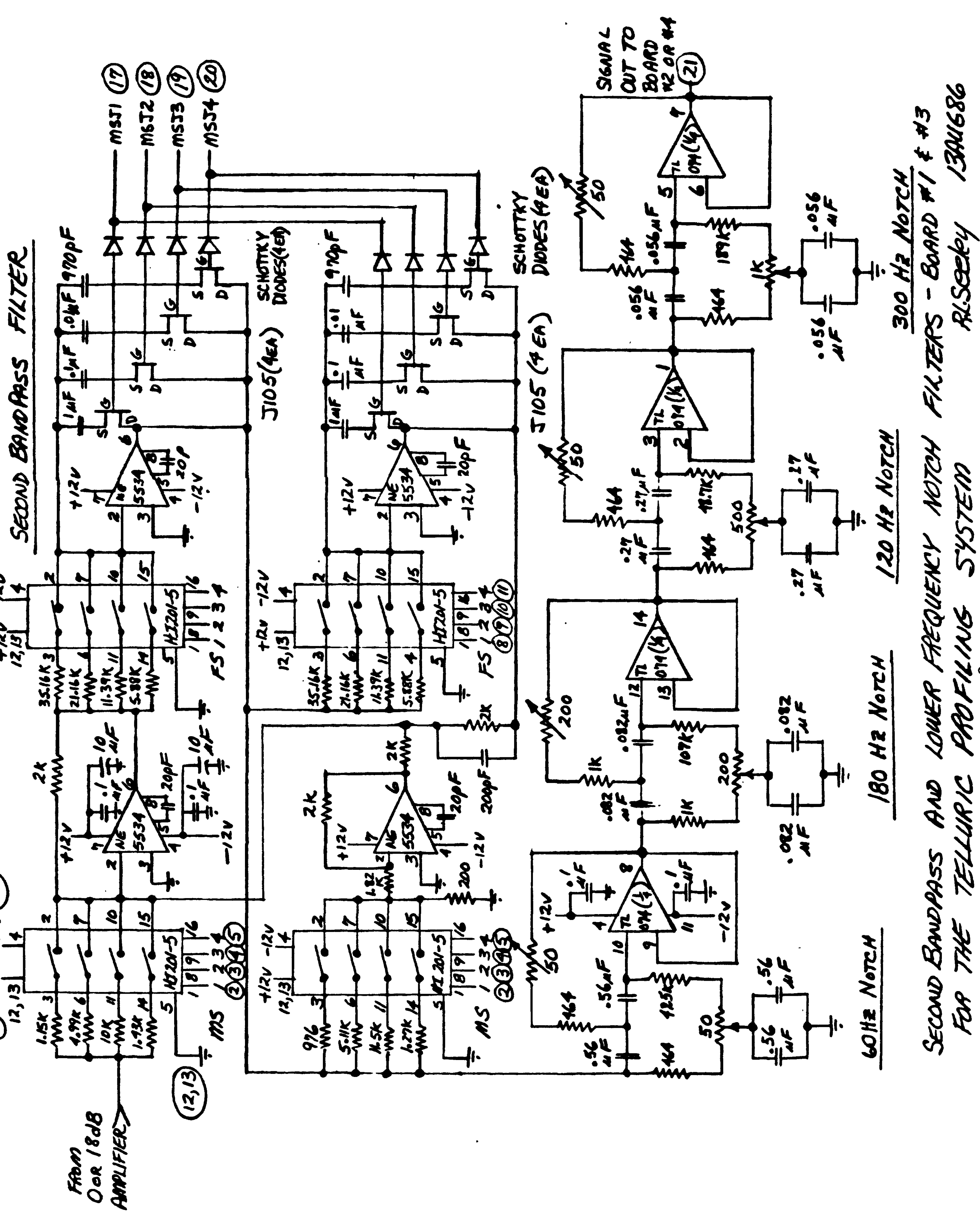


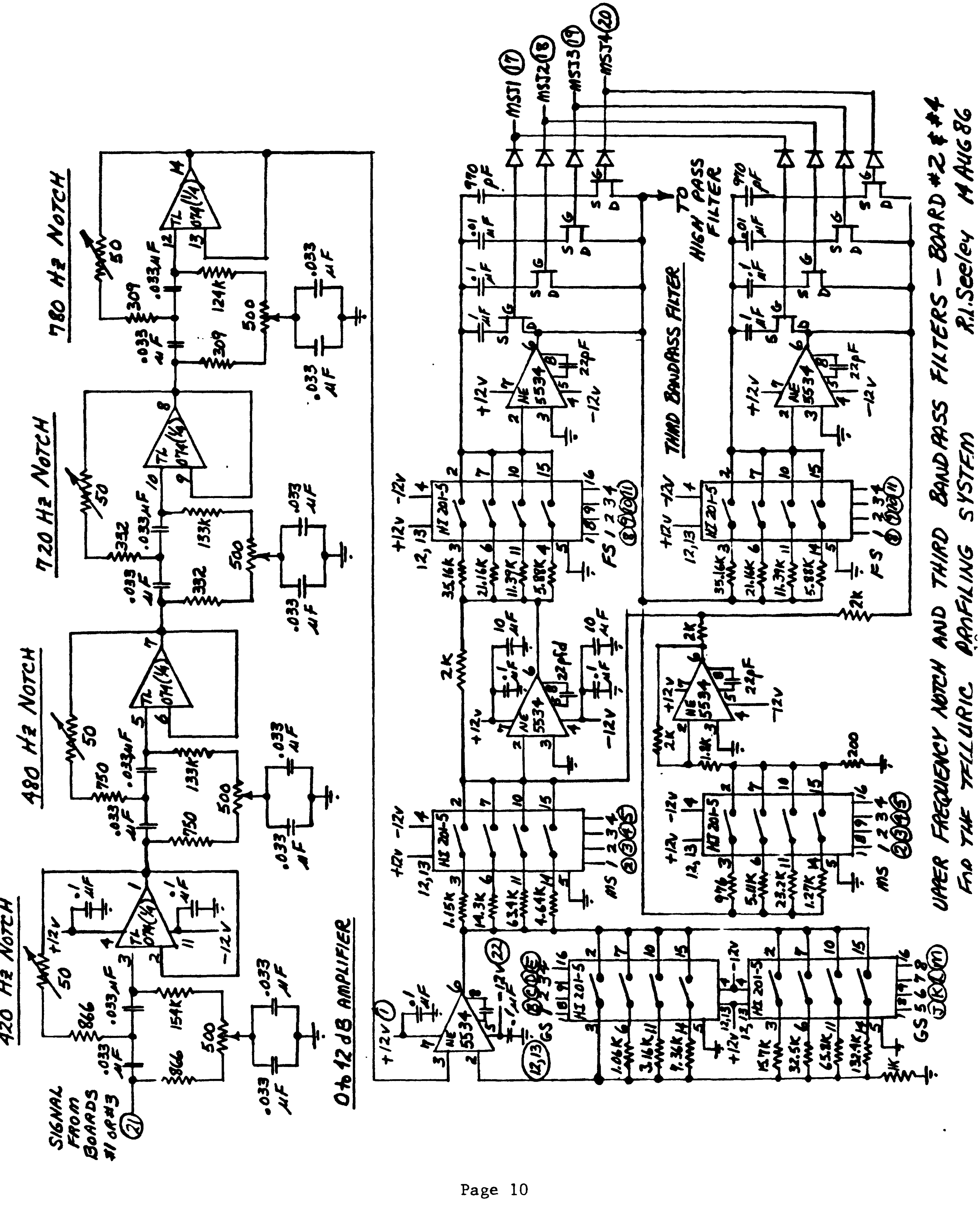
FIRST BANDPASS FILTER

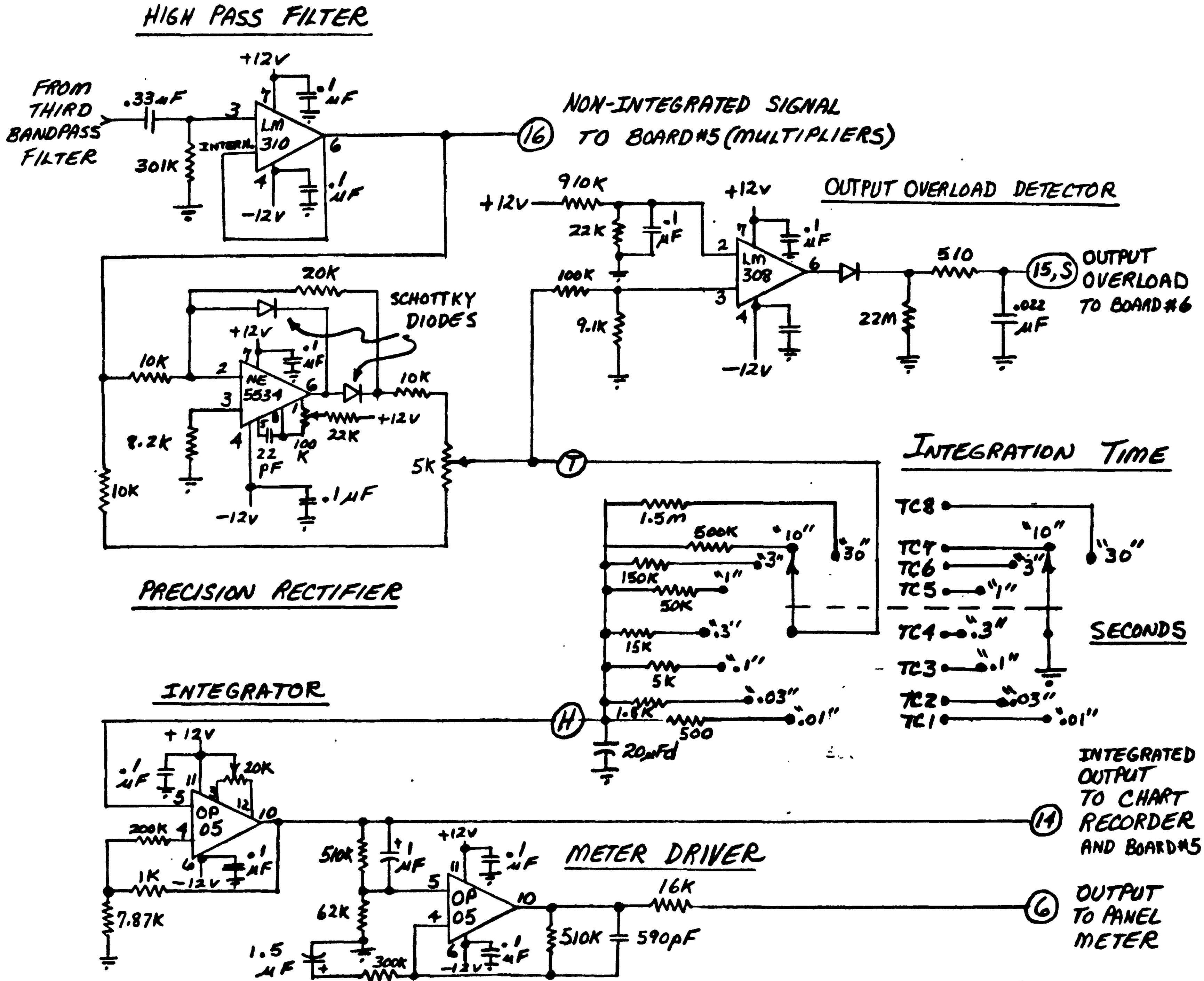
(X) = BOARD EDGE CONNECTION

FRONT END - AMPLIFIER/FILTER BOARD #1 & #3
OF THE TELLURIC PROFILING SYSTEM

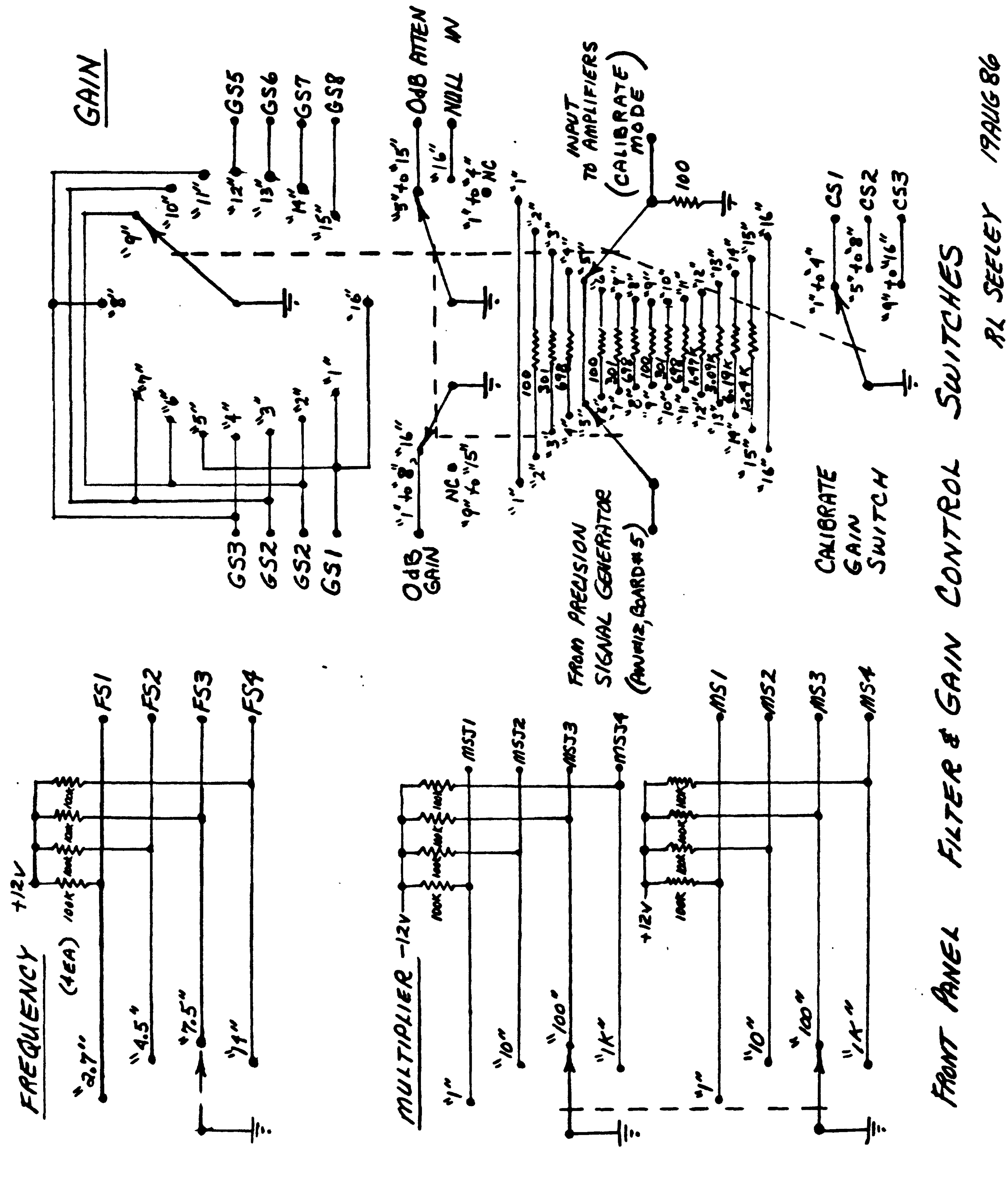
RL Seeley 12AUG 86

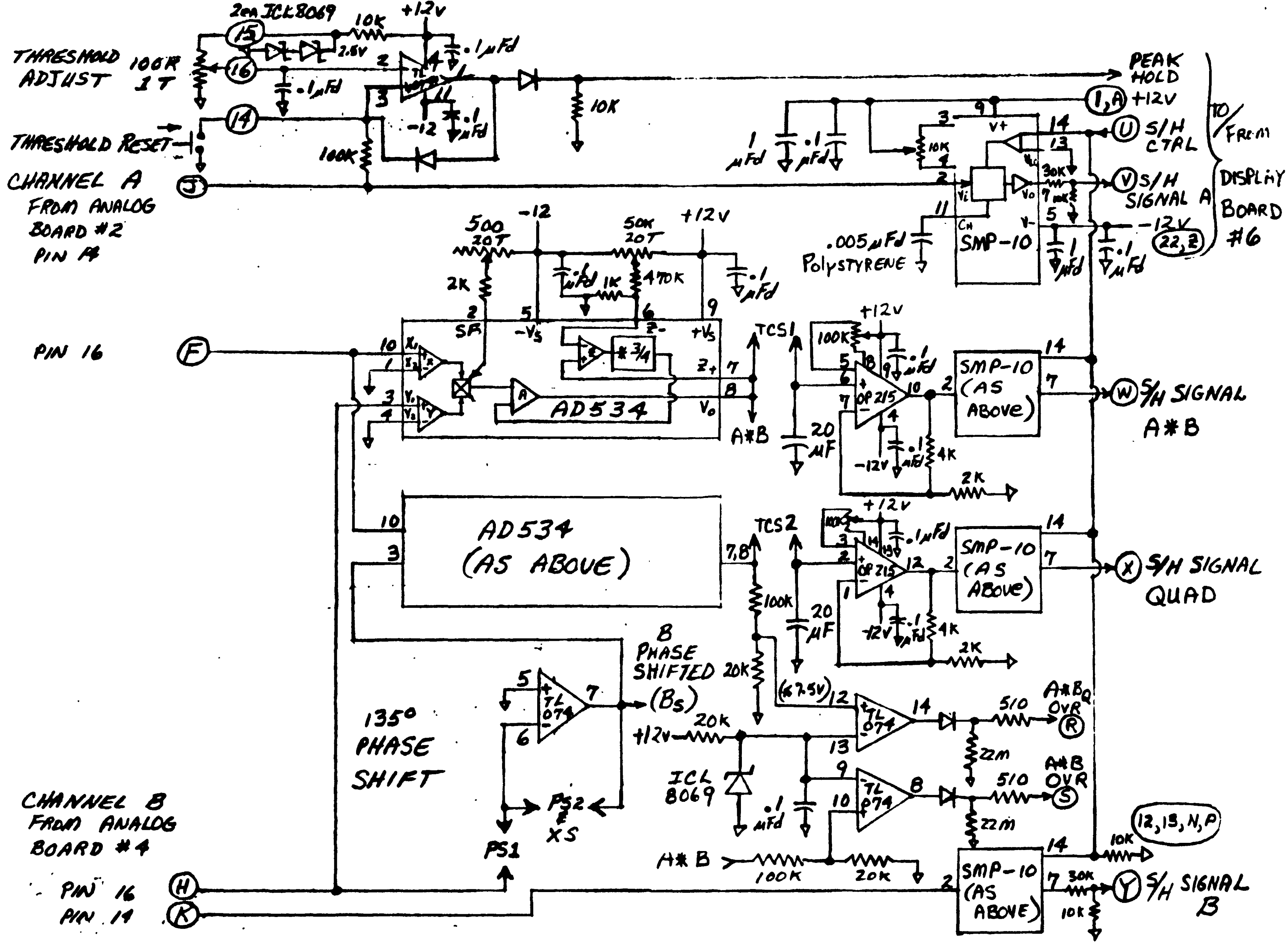

SECOND BANDPASS FILTER
SECOND BANDPASS AND LOWER FREQUENCY NOTCH FILTERS - BOARD #1 & #3
FOR THE TELLURIC PROFILING SYSTEM
60Hz NOTCH
180 Hz NOTCH
120 Hz NOTCH
300 Hz NOTCH
FROM 0 OR 18dB AMPLIFIER
SIGNAL OUT TO BOARD #2 OR #4
SCHOTTKY DIODES (4EA)
J105 (4EA)
MSJ1
MSJ2
MSJ3
MSJ4
HI201-5
NE 5534
TL 074 (1/4)
MS 1 2 3 4
FS 1 2 3 4


UPPER FREQUENCY NOTCH AND THIRD BANDPASS FILTERS — BOARD #2 & #4
FOR THE TELLURIC PROFILING SYSTEM
R.I. Seeley 4 AUG 86
420 Hz NOTCH
480 Hz NOTCH
720 Hz NOTCH
780 Hz NOTCH
0 to 12 dB AMPLIFIER
THIRD BANDPASS FILTER
SIGNAL FROM BOARDS #1 OR #3
TO HIGH PASS FILTER
MSJ1
MSJ2
MSJ3
MSJ4



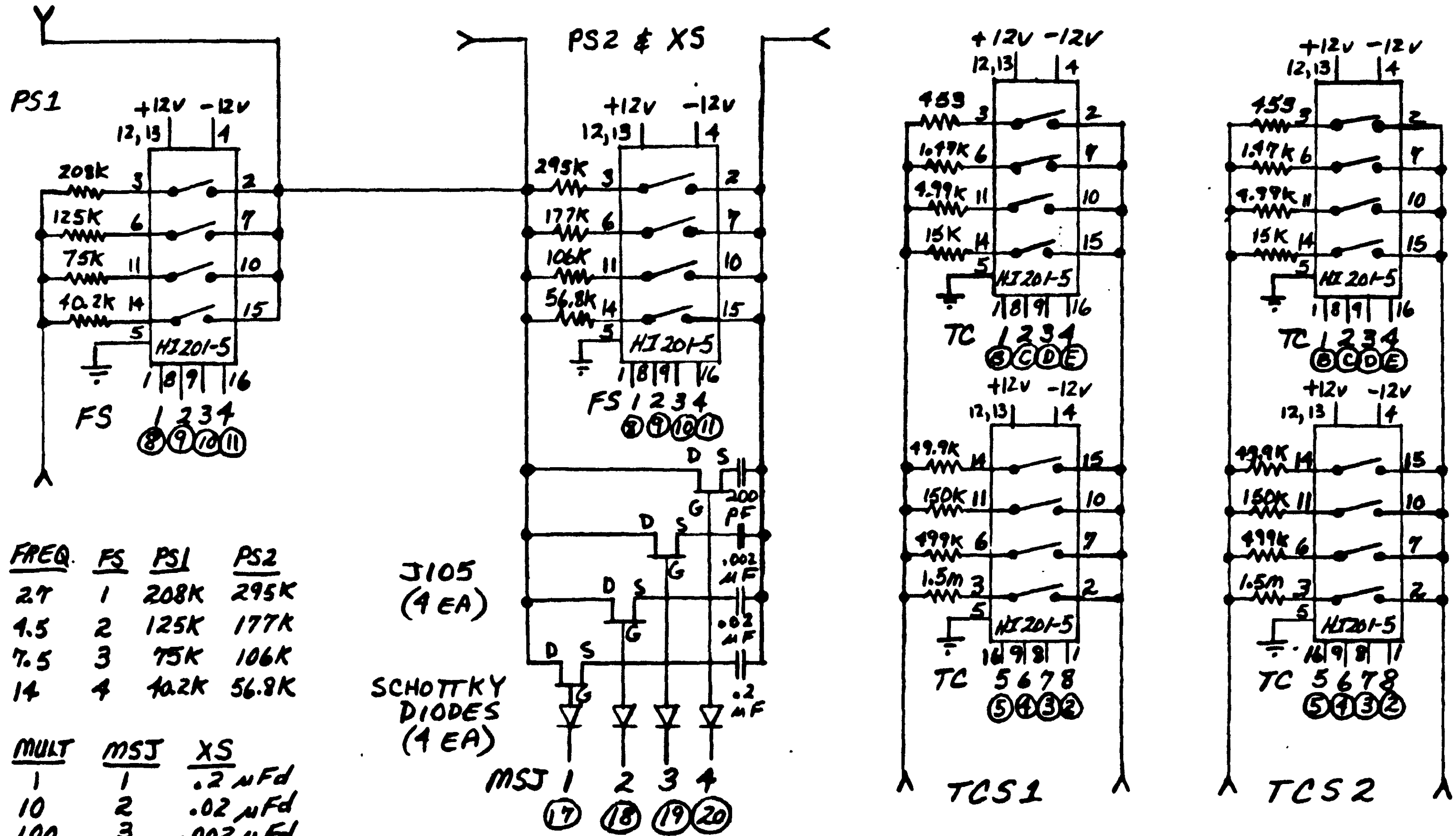
HIGH PASS FILTER, PRECISION RECTIFIER, INTEGRATOR — BOARD #2 & #4
FOR THE TELLURIC PROFILING SYSTEM
R.L. Seeley 15 AUG 86


FRONT PANEL FILTER & GAIN CONTROL SWITCHES
RL SEELEY
19AUG86
FREQUENCY
(4EA)
+12V
100K
"2.7"
"4.5"
"7.5"
"11"
FS1
FS2
FS3
FS4
MULTIPLIER
-12V
"1"
"10"
"100"
"1K"
MSJ1
MSJ2
MSJ3
MSJ4
MS1
MS2
MS3
MS4
GAIN
GS1
GS2
GS3
GS5
GS6
GS7
GS8
0dB GAIN
0dB ATTEN
NULL IN
NC
"1" to "8", "16"
"9" to "15"
"5" to "15"
"1" to "4"
INPUT TO AMPLIFIERS (CALIBRATE MODE)
FROM PRECISION SIGNAL GENERATOR (ANNIIZ, BOARD #5)
100
301
698
CALIBRATE GAIN SWITCH
CS1
CS2
CS3
"5" to "8"
"9" to "16"



PEAK ADJUST AND MULTIPLIERS
FOR THE TELLURIC PROFILING SYSTEM — BOARD # 5

R.L. Seeley
12 APRIL 85



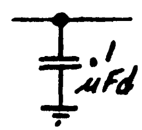
FREQ.	FS	PS1	PS2
2.7	1	208K	295K
4.5	2	125K	177K
7.5	3	75K	106K
14	4	40.2K	56.8K

MULT	MSJ	XS
1	1	.2 µFd
10	2	.02 µFd
100	3	.002 µFd
1K	4	200 pFd

INT. TIME	TC	TCS1	TCS2
.01 Sec.	1	500	500
.03 Sec.	2	1.5K	1.5K
.1 Sec.	3	5K	5K
.3 Sec.	4	15K	15K
1 Sec.	5	50K	50K
3 Sec.	6	150K	150K
10 Sec.	7	500K	500K
30 Sec.	8	1.5m	1.5m

MS 1,2,3,4
FS 1,2,3,4
MSJ 1,2,3,4
GS 1,2,3,4,5,6,7,8
TC 1,2,3,4,5,6,7,8

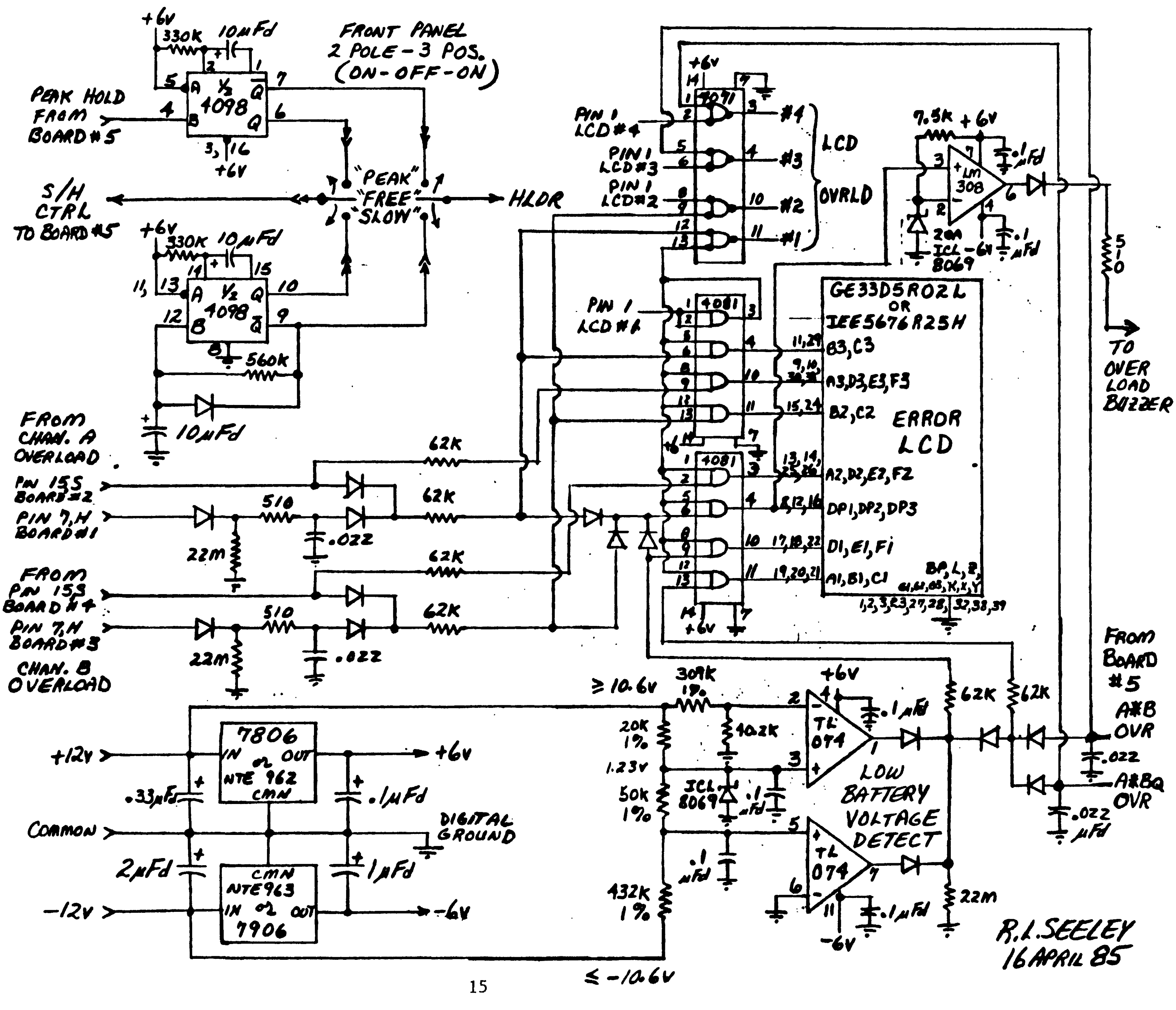
ALL OF THESE SWITCH CONTROL LINES HAVE A .1 µF DECOUPLING CAPACITOR TO GROUND

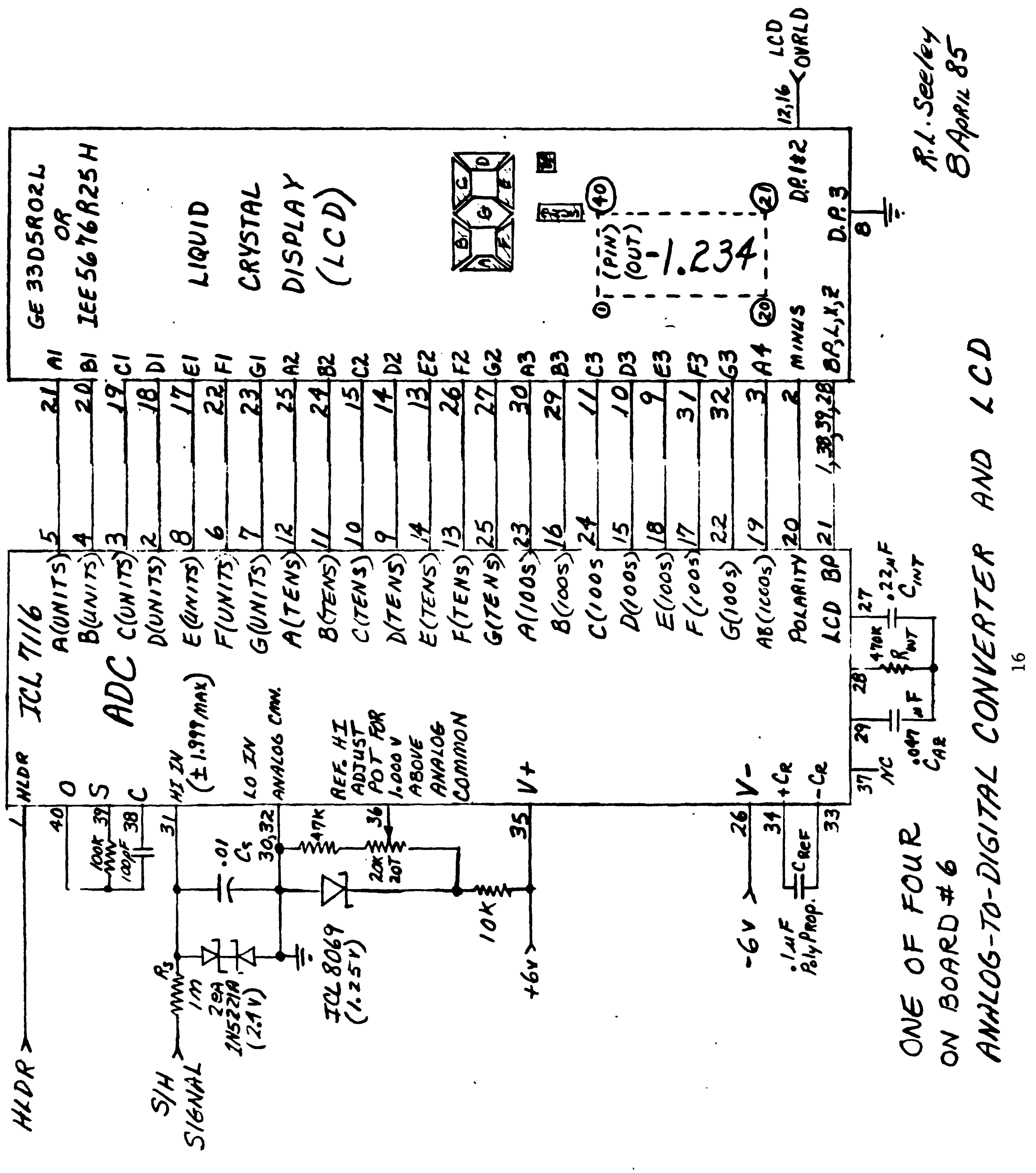


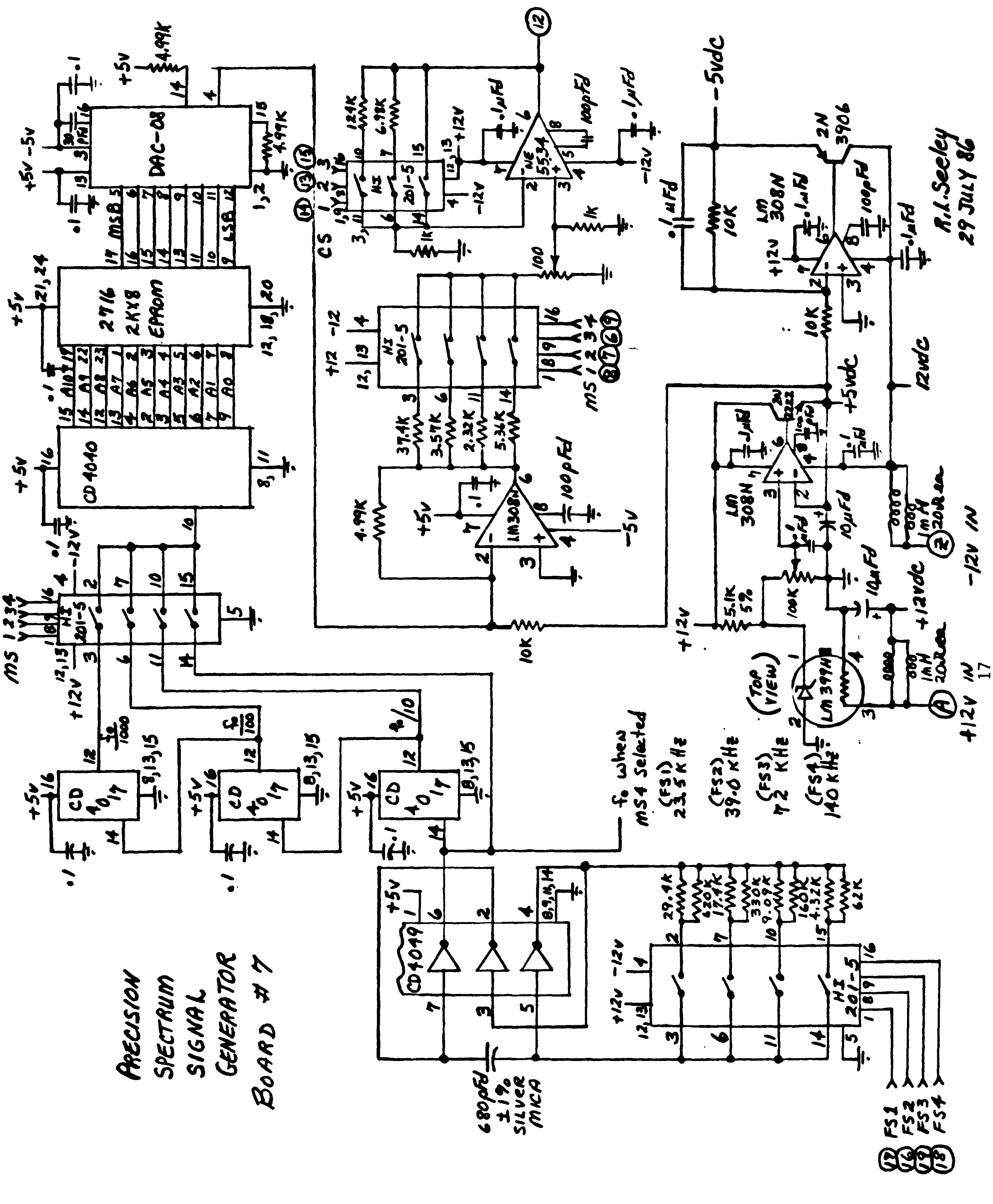
MULTIPLIER PHASE SHIFT (PS) AND INTEGRATION (TCS) CONTROL BOARD #5 FOR THE TELLURIC PROFILING SYSTEM

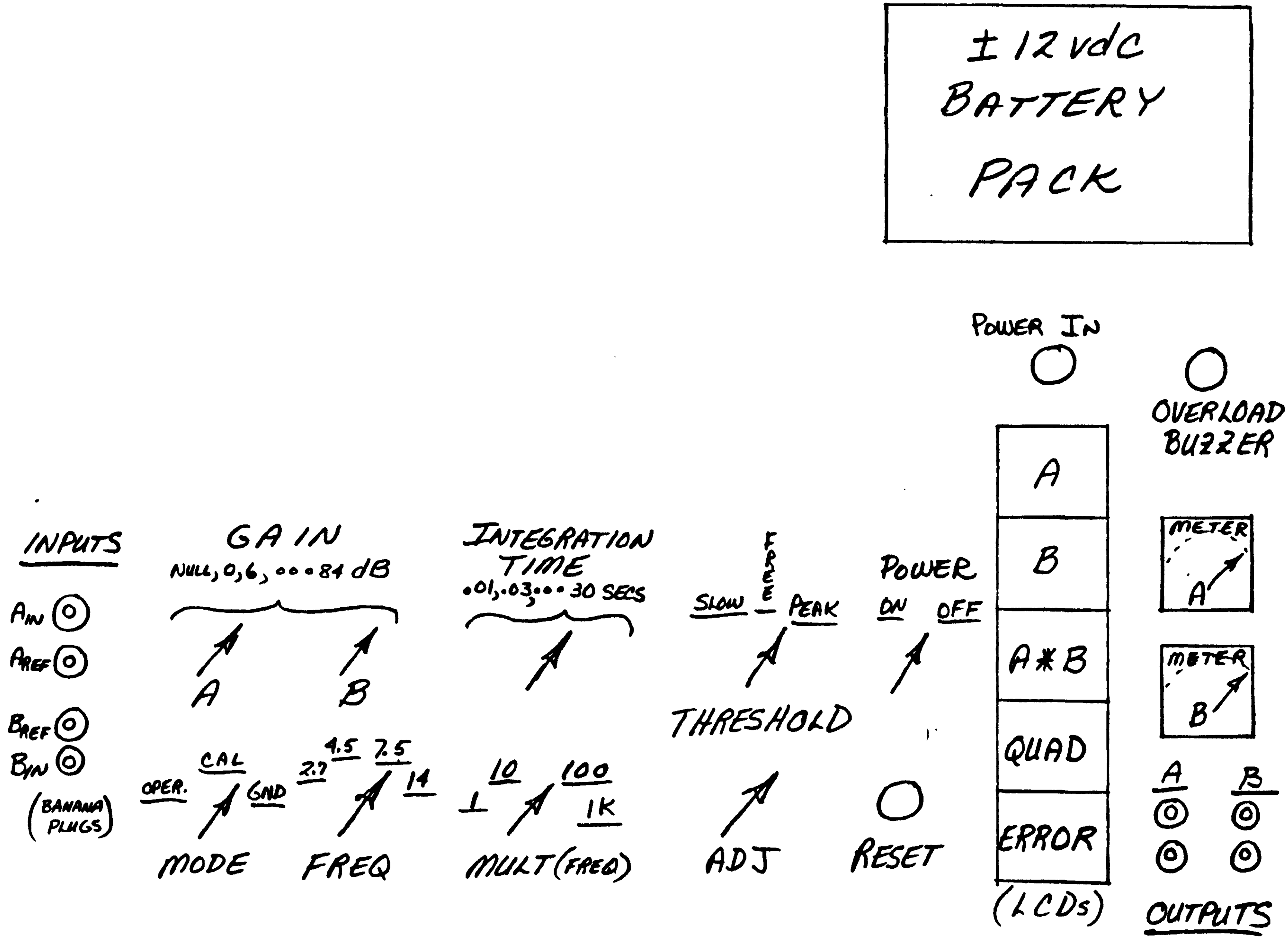
R.L. SEELEY 18AUG86

SAMPLE TIMING AND ERROR LOGIC - BOARD #6




ANALOG-TO-DIGITAL CONVERTER AND LCD
ONE OF FOUR
ON BOARD #6
R.L. Seeley
8 April 85
ICL 7116
ADC
GE 33D5R02L
OR
IEE 5676R25H
LIQUID
CRYSTAL
DISPLAY
(LCD)
-1.234
(PIN)
(OUT)
HLDR
S/H
SIGNAL
LCD
OVRLD
ICL 8069
(1.25V)
1N5221A
(2.4V)
REF. HI
ADJUST
POT FOR
1.000 V
ABOVE
ANALOG
COMMON
HI IN
(±1.999 MAX)
LO IN
ANALOG COM.
POLARITY
LCD BP
MINUS
+6V
-6V
.1μF
Poly Prop.


PRECISION SPECTRUM SIGNAL GENERATOR BOARD #7
R.L. Seeley
29 JULY 86
DAC-08
2716 2KX8 EPROM
CD4040
CD4017
CD4049
HI 201-5
NE 5534
LM308N
LM399H (TOP VIEW)
2N3906
2N2222
680pFd ±1% SILVER MICA
fo when MS4 Selected
(FS1) 23.5 KHz
(FS2) 39.0 KHz
(FS3) 72 KHz
(FS4) 140 KHz
FS1 FS2 FS3 FS4
+12V IN
-12V IN
+12vdc
12vdc
-5vdc
+5vdc



FRONT PANEL LAYOUT (NOT TO SCALE) FOR THE TELLURIC PROFILER

R.L. SEELEY 20 AUG 86

APPENDIX I

Read Only Memory (ROM) Data for Calibration Signal Generator

Location (hex)	Data (hex)							
0000	99	7E	6A	8F	AC	86	4E	52
0008	8C	BB	AB	66	3E	6B	B2	AB
0010	69	5B	8D	9A	6F	6A	99	9A
0018	5F	58	A2	C0	74	31	20	BA
0020	C0	79	4D	61	85	96	9E	93
0028	67	4C	7B	BA	9F	50	56	A9
0030	AF	5C	4E	A3	B3	5A	48	AA
0038	C6	5D	2F	8D	C6	81	53	8C
0040	A2	5D	4B	A1	CC	82	3E	5B
0048	96	A3	90	7A	6B	74	87	82
0050	75	8D	A3	7A	4C	6D	A8	9D
0058	72	75	82	6D	74	A7	20	53
0060	50	AE	C1	5A	2D	8C	D4	98
0068	4A	57	87	96	94	8C	73	68
0070	81	8B	70	78	AD	A7	52	33
0078	85	CB	A4	62	60	79	78	80
0080	A2	A3	6D	4C	72	A4	9E	75
0088	69	7D	8A	84	81	82	78	71
0090	84	9D	90	67	5D	7D	98	9A
0098	8E	75	56	5E	9D	C1	0D	4A
00A0	57	94	A3	85	75	79	79	7C
00A8	8C	8F	7B	6F	79	87	8F	8E
00B0	79	5F	6E	A0	A8	75	56	76
00B8	9A	91	79	78	7D	7C	81	8C
00C0	88	7A	72	73	83	9D	9E	6B
00C8	43	70	BF	BA	60	36	77	BD
00D0	A4	5D	53	8B	A7	84	66	7C
00D8	91	77	66	8E	B0	86	50	5E
00E0	8D	9A	98	98	70	3B	62	C4
00E8	BF	53	42	A8	BE	51	29	95
00F0	E2	A1	4E	4D	6A	7E	A9	C2
00F8	89	3F	4D	89	99	92	A0	93

APPENDIX I (continued)

Read Only Memory (ROM) Data for Calibration Signal Generator

Location ---> (hex) / Data(hex) \

Location (hex)								
0100	55	40	81	B9	A2	72	67	73
0108	7F	88	86	7D	83	8E	7B	67
0110	82	9E	7A	56	85	BC	8F	44
0118	5A	A1	A1	76	7B	91	26	59
0120	79	A6	9D	74	63	73	8C	96
0128	80	67	7A	A1	91	5A	60	9F
0130	AA	6E	54	81	A4	92	74	68
0138	67	7F	AA	AB	73	4A	62	8B
0140	9D	A3	97	68	42	64	A3	AF
0148	90	7E	71	55	58	97	C9	A7
0150	5D	3F	5E	96	BB	A7	64	42
0158	70	AA	A3	72	64	7C	0E	8A
0160	80	77	77	85	8B	7A	72	89
0168	99	7F	62	6C	8A	99	99	88
0170	60	49	79	C0	B6	66	45	73
0178	95	87	89	A1	86	45	4F	AC
0180	CF	7D	36	60	AB	A9	78	69
0188	77	7B	80	90	8D	78	7A	88
0190	71	59	89	CC	A5	3A	2D	92
0198	CE	9A	5F	6A	84	7C	33	83
01A0	94	95	89	6D	56	6D	A1	AD
01A8	87	6A	6D	6F	74	93	AA	8D
01B0	65	67	79	79	89	AA	9A	5B
01B8	4E	87	A3	83	79	95	86	53
01C0	60	A5	B2	79	5B	78	8A	7F
01C8	80	8F	8A	77	72	77	7C	8E
01D0	9D	88	60	5F	87	A1	92	78
01D8	6D	72	81	8C	89	81	7E	7C
01E0	78	7E	88	80	75	85	9B	83
01E8	5A	65	97	A8	8B	6F	63	66
01F0	8A	B5	9E	52	45	93	BE	86
01F8	52	70	9D	8F	6F	74	8A	8F

APPENDIX I (continued)

Read Only Memory (ROM) Data for Calibration Signal Generator

Location ---> (hex) / Data(hex) \

Location (hex)								
0200	83	70	69	82	A5	97	67	5C
0208	7C	8F	8E	96	8F	60	4B	84
0210	BA	99	61	6A	8B	82	6D	7E
0218	98	97	84	67	51	75	2E	BA
0220	58	30	89	C9	8A	48	6F	A3
0228	8C	74	8A	86	5B	68	A7	AC
0230	73	61	7C	7D	73	8E	A2	84
0238	6D	7A	71	5B	8D	D4	A4	2E
0240	33	A7	C3	72	5F	9E	98	4E
0248	55	AA	B6	6B	53	8D	A8	79
0250	53	6F	A0	AA	86	5C	5C	83
0258	9A	8D	82	85	79	64	33	99
0260	98	77	75	87	7A	6C	8B	A0
0268	73	55	8F	BF	7E	30	60	C5
0270	BF	63	45	79	9B	8D	80	82
0278	79	72	84	94	82	6A	71	8D
0280	9A	8B	6F	60	73	9A	A3	82
0288	65	6F	84	83	80	8D	90	79
0290	6A	77	85	86	8E	95	79	55
0298	6B	A8	AB	6B	51	85	2A	84
02A0	5B	72	9A	94	79	77	7D	73
02A8	73	93	AB	8A	4F	49	89	C6
02B0	B3	61	33	5E	AD	C4	8F	52
02B8	4F	82	A6	94	70	75	90	84
02C0	60	6D	A4	A9	6E	53	7E	A0
02C8	88	6D	7A	8C	89	80	77	6D
02D0	7B	9F	9C	67	56	87	A6	84
02D8	6A	7F	86	6F	7D	A5	00	53
02E0	59	9E	AF	7B	60	79	8C	83
02E8	79	78	84	9F	9C	58	2F	82
02F0	E8	B9	39	34	98	AA	68	74
02F8	C1	A4	2D	29	AE	E9	87	32

APPENDIX I (continued)

Read Only Memory (ROM) Data for Calibration Signal Generator

Location --->
(hex) / Data(hex) \

Location								
0300	65	B1	96	55	66	A9	A7	64
0308	55	91	AA	70	4A	80	C0	A6
0310	5F	48	66	8F	AF	B0	7E	46
0318	53	8B	9B	8A	98	A6	2B	24
0320	4D	C3	E6	90	3D	44	79	98
0328	9D	99	8B	6C	54	67	9C	B0
0330	87	5C	6E	93	8A	70	7B	8F
0338	7F	73	90	97	67	54	8A	AF
0340	89	67	7F	8A	68	66	9C	B1
0348	7F	58	6C	89	8B	85	81	81
0350	8A	8B	6B	50	79	BC	B5	71
0358	4C	5A	71	9A	CE	B5	3F	0A
0360	76	ED	C4	4B	3A	8B	AF	7F
0368	5A	77	A3	A3	74	50	67	9B
0370	A8	85	6C	73	7A	77	88	9E
0378	8D	63	62	8A	A0	88	6B	6D
0380	87	98	8A	6A	66	8B	A3	85
0388	61	6C	8F	98	87	77	6A	6C
0390	8E	AE	92	54	50	8B	AD	91
0398	74	77	77	6A	78	9E	24	7C
03A0	60	6C	80	87	8E	95	86	6C
03A8	69	7A	82	86	9C	A2	72	3D
03B0	5A	AD	C3	83	55	6F	8B	77
03B8	6B	94	B4	8F	52	4B	7F	AB
03C0	A5	7E	63	6D	86	8A	7D	7A
03C8	87	8F	89	78	65	65	89	B0
03D0	A2	6D	53	68	81	93	AA	A3
03D8	66	39	63	AC	B2	86	62	73
03E0	63	66	99	BC	93	50	49	81
03E8	B6	AE	6C	3B	65	BC	C0	67
03F0	3C	74	A4	90	80	92	80	4E
03F8	5F	A8	B6	7E	64	74	6E	69

APPENDIX I (continued)

Read Only Memory (ROM) Data for Calibration Signal Generator

Location --->
(hex) / Data(hex) \

Location (hex)	Data (hex)							
0400	9D	C5	89	38	4B	9B	B4	93
0408	78	68	60	7C	A4	99	6F	72
0410	8B	74	5D	93	C4	84	2F	59
0418	BD	B6	65	5C	88	82	2B	96
0420	B9	71	29	6C	D8	B8	46	3D
0428	97	B3	7B	61	83	94	82	79
0430	75	6C	81	AE	A1	58	43	86
0438	B1	8F	76	88	79	4C	6B	C3
0440	BD	54	36	90	BF	7C	49	7A
0448	B0	99	6B	63	71	7F	95	A1
0450	8C	6A	5F	6B	84	A4	A9	7E
0458	54	63	89	8C	84	9A	1F	69
0460	3E	6B	B4	B1	72	5C	80	96
0468	79	5C	76	B0	B8	73	34	53
0470	A8	BF	88	62	73	7F	6E	75
0478	9F	A7	78	59	72	8F	85	78
0480	8B	99	7E	60	6D	8D	90	82
0488	8B	93	6F	48	69	B8	C5	7C
0490	3D	4D	8A	B5	B0	7B	45	54
0498	9E	B7	7D	55	7F	A5	3F	55
04A0	75	A4	98	75	72	79	74	7E
04A8	96	91	75	73	87	7F	67	79
04B0	A6	A8	71	49	63	9C	AF	8C
04B8	67	6D	83	81	73	83	9D	92
04C0	70	63	72	86	98	99	79	5E
04C8	7A	A1	83	51	75	C0	A8	4B
04D0	44	94	AB	79	70	99	90	5A
04D8	5C	92	A2	87	7C	7E	6F	6B
04E0	89	99	82	77	8C	88	60	60
04E8	9A	B4	80	51	70	A3	93	5F
04F0	5F	98	B4	8D	58	52	77	A0
04F8	AE	93	61	50	77	9E	90	7B

APPENDIX I (continued)

Read Only Memory (ROM) Data for Calibration Signal Generator

Location (hex)	Data (hex)							
0500	8D	93	61	46	88	CA	9C	4A
0508	56	9B	A0	71	68	87	93	87
0510	7B	6E	6C	8B	A4	86	61	76
0518	96	7E	62	8B	B6	85	2C	55
0520	B0	C9	84	41	4C	8C	B7	A6
0528	74	58	5F	79	9D	B6	93	47
0530	40	97	C6	83	4B	7C	AB	7B
0538	52	85	AE	7E	5A	88	A2	71
0540	5B	8C	A2	77	6A	90	90	65
0548	69	9A	9E	72	67	87	8F	79
0550	72	83	8E	8A	7D	6F	70	87
0558	98	8B	74	6D	75	89	1C	90
0560	61	52	89	BD	9D	56	4A	7B
0568	A5	A5	89	68	5B	73	95	9C
0570	89	78	6E	70	89	9B	7E	59
0578	7A	B8	A3	4E	3D	88	B7	9C
0580	7F	7A	5D	48	86	D9	B6	42
0588	31	97	C2	71	44	92	CE	87
0590	32	57	A7	A1	79	90	A1	55
0598	1F	83	FF	C6	25	11	19	E0
05A0	94	49	62	94	93	7E	7C	80
05A8	7C	7B	7F	86	8B	84	73	74
05B0	89	89	6F	76	A4	A3	5B	3B
05B8	85	CD	A2	4C	51	9D	AC	67
05C0	46	8D	D5	A3	31	26	99	E3
05C8	A1	45	52	91	97	76	7A	91
05D0	8B	76	74	78	7A	8C	9D	83
05D8	5C	69	9B	A2	77	5D	70	93
05E0	A0	8D	66	58	7F	A9	97	6A
05E8	69	8A	8F	77	6F	7D	8E	9A
05F0	BE	61	4B	82	C2	A2	50	52
05F8	9F	AB	65	4D	8F	BA	8D	58

APPENDIX I (continued)

Read Only Memory (ROM) Data for Calibration Signal Generator

Location --->
(hex) / Data(hex) \

Location								
0600	65	8A	88	78	89	A2	8D	5A
0608	4E	7E	B0	AB	7C	5A	63	87
0610	97	81	6C	89	B1	8F	3B	39
0618	A0	DF	A1	4C	4C	77	08	97
0620	A0	81	5A	76	A5	81	45	71
0628	CB	B5	51	41	83	9A	7F	88
0630	A1	84	58	62	84	8E	96	9F
0638	7F	51	60	96	9B	78	7F	9E
0640	88	52	51	8A	B8	AF	77	43
0648	53	9C	B6	7F	5E	8B	A1	68
0650	4B	89	B6	8E	68	7A	7D	63
0658	7B	B1	9F	5B	5B	8F	10	70
0660	85	A3	7E	52	72	A3	94	72
0668	7B	86	73	6F	8C	98	87	7A
0670	71	61	72	AC	BC	77	3B	56
0678	95	B0	A5	83	53	4A	86	B6
0680	95	68	7D	93	6A	51	8B	BC
0688	94	61	6E	7D	69	7B	B9	AE
0690	4F	36	90	C7	8A	4D	6B	9B
0698	96	83	7E	67	55	87	0C	B2
06A0	46	26	80	C7	A1	67	74	91
06A8	73	50	78	BA	B1	70	52	68
06B0	7C	88	A2	AB	79	46	5E	98
06B8	9E	7F	83	98	7B	4B	5D	A1
06C0	BB	94	65	55	64	8D	B2	9D
06C8	60	54	8A	AA	81	56	6D	A0
06D0	AA	84	5A	51	7A	B2	B7	7A
06D8	45	57	94	AF	94	6D	62	7C
06E0	94	87	6D	7C	9E	8D	59	5F
06E8	A1	B0	73	52	79	9A	8C	81
06F0	85	73	60	83	AE	90	58	66
06F8	9D	99	67	62	90	A8	8A	5E

APPENDIX I (continued)

Read Only Memory (ROM) Data for Calibration Signal Generator

Location --->
(hex) / Data(hex) \

Location (hex)								
0700	56	82	B1	A1	60	54	8F	A5
0708	70	5A	93	AE	77	56	7F	97
0710	76	73	9B	96	66	66	8D	86
0718	6C	8D	B0	81	46	61	08	99
0720	88	97	86	47	48	A1	CC	90
0728	58	66	77	72	8E	B7	97	4B
0730	48	91	B6	93	69	63	71	8C
0738	A7	99	61	47	77	B6	B2	74
0740	4B	61	93	A5	8F	75	6D	74
0748	83	93	8C	6C	67	92	A9	7F
0750	55	6B	93	91	86	92	86	57
0758	55	92	B3	92	75	77	28	57
0760	84	C0	AB	66	56	6C	6D	83
0768	C6	C5	4D	06	6D	EE	CA	49
0770	2C	7F	BE	A6	67	48	6B	B0
0778	BB	75	3F	62	A1	A9	89	72
0780	62	64	92	BA	92	47	4B	94
0788	B7	9A	78	5F	4C	6A	BB	D7
0790	85	2C	39	87	BC	BC	91	51
0798	3D	76	AC	99	7A	91	18	57
07A0	30	7E	D7	BA	65	4F	66	71
07A8	89	B6	AC	61	46	7C	98	79
07B0	7C	B0	A3	47	30	8F	D5	A1
07B8	51	55	88	96	82	7B	84	88
07C0	7E	70	73	8D	9A	7E	65	7D
07C8	99	7B	5C	8A	BE	86	2D	54
07D0	CE	D0	56	28	83	C0	8E	60
07D8	7C	90	74	70	94	91	6A	74
07E0	9A	89	5D	76	AB	91	51	66
07E8	AB	A2	62	60	90	8F	70	82
07F0	A2	81	50	69	A1	9F	7F	7A
07F8	79	62	6C	A4	B3	76	50	77

APPENDIX II

Board Pin Number/Signal Name Combinations

Pin	Board #1,#3	Board #2,#4	Board #5	Board #7
1	+12 vdc	+12 vdc	+12 vdc	NC
2	MS1	MS1	TC8	NC
3	MS2	MS2	TC7	NC
4	MS3	MS3	TC6	NC
5	MS4	MS4	TC5	NC
6	Sig.In(from Mode)	Sig.Out(to Meter)	NC	MS3
7	Input Ovrld.(to Err)	NC	NC	MS2
8	FS1	FS1	FS1	MS1
9	FS2	FS2	FS2	MS4
10	FS3	FS3	FS3	NC
11	FS4	FS4	FS4	NC
12	Gnd	Gnd	Gnd	Cal.Sig.(to Atten.)
13	Gnd	Gnd	Gnd	CS2
14	NC	Int.Sig.Out(to Recrdr)	Thrshld.Reset	CS1
15	NC	Output Ovrld.(to #6)	+2.5 vdc	CS3
16	NC	Non-Int.Sig.(to #5)	Thrshld.Adj.	FS2
17	MSJ1	MSJ1	MSJ1	FS1
18	MSJ2	MSJ2	MSJ2	FS4
19	MSJ3	MSJ3	MSJ3	FS3
20	MSJ4	MSJ4	MSJ4	NC
21	Sig.Out(to #2,#4)	Sig.In(from #1,#3)	NC	NC
22	-12 vdc	-12 vdc	-12 vdc	NC
A	+12 vdc	+12 vdc	+12 vdc	+12 vdc
B	GS1	GS1	TC1	NC
C	GS2	GS2	TC2	NC
D	GS3	GS3	TC3	NC
E	GS4	GS4	TC4	NC
F	Sig.In(from Mode)	Sig.Out(to Meter)	Non.Int.A(from #2)	NC
H	Input Ovrld.(to Err)	Sig.In(from Int.)	Non.Int.B(from #4)	NC
J	FS1	GS5	Int.Sig.A(from #2)	NC
K	FS2	GS6	Int.Sig.B(from #4)	NC
L	FS3	GS7	NC	NC
M	FS4	GS8	NC	NC
N	Gnd	Gnd	Gnd	NC
P	Gnd	Gnd	Gnd	NC
R	NC	NC	Quad Ovrld.(to #6)	NC
S	NC	Output Ovrld.(to #6)	A*B Ovrld.(to #6)	NC
T	NC	Sig.Out(to Int.)	Peak Hold(to #6)	NC
U	MSJ1	MSJ1	S/H Ctrl(from #6)	NC
V	MSJ2	MSJ2	S/H Sig. A(to #6)	NC
W	MSJ3	MSJ3	S/H Sig. A*B(to #6)	NC
X	MSJ4	MSJ4	S/H Sig. Quad(to #6)	NC
Y	Sig.Out(to #2,#4)	NC	S/H Sig. B(to #6)	NC
Z	-12 vdc	-12 vdc	-12 vdc	-12 vdc