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# A LOW-POWER GEOPHYSICAL DATA-ACQUISITION SYSTEM: MODIFICATION II

by

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# MODIFICATION II

This report is a description of the data-acquisition module currently used in the U.S. Geological Survey's Ocean Bottom Seismometer (OBS). This description supercedes the description contained in U.S. Geological Survey, 1984, Major electronic circuits and components of the Ocean Bottom Instrument Package (OBIP): U.S. Geological Survey Open-File Report 84-267,69 p., 21 sheets.

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# INTRODUCTION

The design goal for the U.S. Geological Survey (USGS) Ocean Bottom Seismometer Program has been to develop a geophysical data-acquisition system (GDAS) that can meet the requirements of wide dynamic range, programmable modes of operation, large data storage capacity, small size, and low power. The instrument's intended use involved four applications: an ocean-bottom instrument package for long-term seismic studies and short-term seismic refraction studies, a four-component surface buoy with FM telemetry and digital recording for use in refraction experiments, two- and four-component land systems for use in onshore seismic studies, and a real-time, high-resolution, data-acquisition system for geophysical studies. Other specifications required the ability to acquire data for as long as three months with up to four channels of analog input, a time channel with an accuracy of 100 milliseconds over a two month period, 120 dB of dynamic range, anti-aliasing filters, event-detection capability, and timed-window capability.

The basic design for this system was developed at the U.S. Geological Survey (Ambuter and Davis, 1981) using a modular approach to maximize its usefulness. The GDAS started out as a discrete component system, using a reel-to-reel recorder for data storage. This system did show some success in data acquisition, but difficulties with the tape formatting and the playback software resulted in little useful data recovery. In addition, system flexibility, low system noise, and wide dynamic range were not achieved. In 1982, the GDAS was redesigned as a microprocessor-based system (Ambuter and Godley, 1983) using a bus structure similar to the S-100 IEEE standard (Elmquist et al., 1979) and a cartridge tape drive for data storage. A block diagram of this system is shown in Figure 1. The modular approach was maintained by designing boards for specific functions, including power control, analog conditioning, analog-to-digital conversion, system control, and data storage.

The GDAS detects analog signals from geophones and hydrophones, and records these signals as digital words on magnetic tape. There are four channels of data acquisition in the GDAS: the first three are designed to receive signals from a geophone and the fourth channel is designed for a hydrophone input. The low-level signals from the sensors are amplified to increase the signal level high enough for the analog-to-digital convertor to digitize it. The signals are then filtered to remove the unwanted high frequencies; any DC offset generated by the amplifier and filter circuits is also removed. After filtering, one channel can be connected to an event-detector circuit to permit the system to record data when a seismic signal is detected. Otherwise, the system will operate on a timed-window mode where the system will record data at a specified time only. The analog signals for each channel enter a gain-ranging amplifier that increases the dynamic range of the analog circuitry, allowing the system to record signals as small as a microvolt and as large as 30 millivolts. The resulting gain of this circuit is saved and recorded as a 4-bit gain code. The signals enter a sample-and-hold circuit, which holds the signal long enough for the analog-to-digital convertor to digitize it, and, finally, are sent to an analog-to-digital (A-D) convertor where the analog signal is converted to a 16-bit digital word. The lower 12 bits of the 16-bit word represent the result of the A-D conversion, and the upper 4 bits represent the gain code from the gain-ranging amplifier. The data word is entered into the

memory buffer and is recorded on tape after the memory buffer is filled.

Two modes of operation determine how data are placed into the memory buffer. In the timed-window mode, no data are placed into memory until the designated start time of each window has been reached. The memory buffer is then filled with data until the buffer is full; the data are then written to tape. In the event-detection mode, the memory buffer is continuously filled with data in a circular fashion and, when filled, starts over at the beginning. This continues until the event-detector indicates that a seismic signal has been detected. When this happens, the system checks to see how much data are desired beyond the event (a value that is programmed into the GDAS at start up). The memory buffer will continue to fill with data until that preset value is reached and, will then write the data to tape.

The GDAS has proven to be a useful tool when incorporated into the Ocean Bottom Seismometers (OBS's) in short-term refraction studies. The dynamic range of the data is only 90 dB, but this has not proven to be much of a handicap in these studies. FM telemetry was never implemented, and using this system as a high-resolution, seismic-reflection system is not possible because the GDAS cannot transfer the data to tape fast enough for most applications. The specifications of the current system are shown in Appendix I.

# 1. THEORY OF OPERATION

The GDAS is designed specifically for the acquisition of geophysical data in remote environments. It provides the circuitry for power distribution and communications between boards (the system bus), power regulation, system timing, system monitoring, analog signal conditioning, event detection, analog-to-digital conversion, program control, and data recording. This section describes the function of that circuitry and traces the various signals through the electronic components used. These descriptions make reference to various part numbers and connector pin numbers in the schematics listed in Figures 12 through 16 to aid in understanding the various operations.

## 1.1 SYSTEM BUS

The data-acquisition electronic package consists of six boards connected to a bus that is based on the S-100 IEEE standard (Elmquist et al., 1979). This bus consists of 100 parallel lines etched on a printed circuit board containing seven, 100-pin connectors tied to the parallel lines. These lines provide the means by which the boards communicate with each other and are divided into five groups: 1) power and ground lines, 2) address lines, 3) data lines, 4) control signal lines, and 5) undefined or spare lines. Some of the spare lines of this bus have been assigned to meet the unique requirements of the GDAS, and a complete listing of their function for each board is given in section 5. The bus used in the GDAS has several modifications to permit communication with devices not on the system bus, such as the cartridge drive, the terminal used to program the system, and a liquid crystal display. These modifications also provide a means to transfer analog signals between boards on the bus. This requires that the boards occupy specific slots on the bus. As shown in section 5.1, slot number 1 uses pins 4 through 17 to communicate with external devices. The power interface board contains the circuitry to control these devices, hence occupies slot number 1. Board numbers 2, 3, 4, and 5 are designed to pass analog signals on pins 5 through 17 and pins 55 through 67 of the bus. To properly connect the various analog signal paths together, the analog board must occupy the number 2 slot; the preamplifier board, the number 3 slot; and the analog-to-digital board, number 4 slot. The number 5 slot is left open for expansion. Slots 6 and 7 are occupied by the controller board and the cartridge controller board. Although either board can occupy either slot, external connections to the cartridge controller board are far simpler if it occupies the number 7 slot. Figure 5 illustrates the physical locations of these board on the system bus.

The power and ground lines transmit the voltages needed to power each board on the bus. As shown in section 5.1, a regulated +5 volts is available on pins 1 and 51 of the bus, and a regulated -5 volts is available on pins 21 and 54 of the bus. Regulated power is supplied on these lines to simplify design of each board (i.e., there is no need for voltage regulators on each board) and to conserve power, since one regulator consumes less power than many regulators. The system ground is the 0 volt reference for the system and is available on pins 20, 50, 67, 70, and 100 of the bus. These pins are connected together on the power interface board and are common for both analog and digital signals. An unregulated +12 volts is available on pin 2 of the bus, and an unregulated -12 volts is available on pin 52 of the bus. These voltages,

which are provided for expansion purposes, are not currently used in the system.

Address lines provide a means for the controller board to communicate with other boards on the system bus. This board is responsible for all of the system communications, and each board in the GDAS is designed to recognize a specific code word generated by the controller board when it needs to communicate. This code word is sent through the bus on the eight address lines, labeled A0 through A7, which are connected to all of the boards on the bus. Each board compares the word sent by the controller board with its own code word to determine if it is the one being addressed. The address word is constructed of the eight lines, each having one of two logic states: either a high (+5 volts) or a low (0 volts). The address word is commonly described using binary notation where a value of 1 indicates a high, and a value of 0 indicates a low. The eight binary numbers are also combined to a single number using hexadecimal notation. Hexadecimal notation is based on 16 symbols (0 through 9 and A through F) and is constructed in powers of two using the binary number generated on the eight address lines. The hexadecimal value of these lines is as follows:

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | address lines |
|---|---|---|---|---|---|---|---|---|
| 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 | hexadecimal value |

The address for the analog-to-digital board, for example, demonstrates how the various logic states can be presented in both binary and hexadecimal notation. This board responds when the following logic states are present on the bus:

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | address lines |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | +5 | +5 | 0 | 0 | 0 | voltage level |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | binary value |
| 0 | 0 | 0 | 10 | 8 | 0 | 0 | 0 | hexadecimal value |

The hexadecimal number is obtained by adding all the values together. In this case, the hexadecimal number is 10 + 8 or 18. The addressing requirements for each system function will be discussed later in this section, and both binary and hexadecimal values will be given. The binary value will aide in following the digital signal path, and the hexadecimal value will aide in following any software used in this system.

The data lines on the bus provide a means for the controller board to transmit to or receive data from other boards on the bus. The information contained on the data lines is always coupled with a specific address on the address lines, as discussed above. The address selects the board for communication and the data represents the message sent or received. There are two sets of data lines used in this bus: the data-out (DO) lines that send data from the controller board to the board being addressed, and data-in (DI) lines that send data from the board being addressed to the controller board. There are eight lines for each of these functions, and they operate in the same manner as described for the address lines.

The control lines allow the controller board to control data flow on the bus. Four of these lines are used to indicate whether data are to be received or sent. These lines are sIN (pin 46 of the bus) and pDBIN (pin 78 of the bus), which indicate to the board being addressed that data are

to be sent to the controller board, and sOUT (pin 45 of the bus) and PWR* (pin 77 of the bus), which indicate to the board being addressed that data are to be received from the controller board. VIO (bus pin 4) is an interrupt flag, sent from the analog-to-digital board to the controller board, that indicates data are available. CLOCK (bus pin 49) is the system's reference clock, and provides the time base for all boards used in the system.

The undefined lines of the bus are used by the system to pass analog signals among adjacent boards. Section 5.1 illustrates the layout of these lines on the bus, and they will be described in more detail later in this section.

## 1.2 POWER REGULATION

The power regulation circuitry in the GDAS is located on the power interface board. The part numbers and pin numbers used in this discussion are illustrated in Figure 12.

Using the GDAS for remote geophysical applications requires battery-supplied power for operation. Various components within the system require direct current (DC) voltages of +5 volts, -5 volts, +12 volts, and -12 volts. The system, however, is powered with a battery that provides only +12 volts and -12 volts. This was done for two reasons. First, it simplified the requirements for the battery (i.e., two automobile batteries could be used in land applications). Second, the electronic components that make up the system require +5 volts and -5 volts regulated to within .25 volts for proper operation. The battery voltage drops with usage and cannot, therefore, provide the necessary regulation. Instead, voltage regulators (electronic components that sense and hold the voltage to a defined level) are used to provide proper regulation to +5 volts and -5 volts. Battery voltages enter the power interface board on connector P1 using specific pins. Pins 1 and 4 have been removed so that the connector can be keyed to prevent an accidental reversing of the plug. Pins 6 and 8 supply the ground for the entire system, and are tied together to exit the board on pins 20, 50, 67, 70, and 100 of the bus connector. Again, this common ground is for both analog and digital signals. The +12 volts from the battery enter the board on pin 2 of connector P1 and first pass through a 3-amp microfuse (F2). This fuse provides protection for the battery in the event that a component failure should overload the battery capacity. The +12 volts exits the power interface board at bus pin 2 to provide this voltage to the other boards on the bus. The +12 volts also supplies power to the +5 volt regulator (Q2), which provides the regulated +5 volts to the oscillator (Y1) and to other boards on the bus via pins 1 and 51 of the bus connector. A battery backup circuit is also connected to the +12-volt input of this regulator. The circuit consists of two, 9-volt transistor batteries that maintain power to the system in the event of a power failure. This option is enabled by SW2. In addition, the backup provides for situations where the program is loaded while being powered by a bench supply before being transferred over to a field power source. The batteries provide this backup power for at least 1 hour during such an operation. The regulated +5 volts pass through a 2-amp microfuse (F5) before leaving the power interface board in order to protect the regulator from overload. The -12 volts enter the power interface board on pin 3 of connector P1 and pass through a 2-amp microfuse (F1). This voltage exits the board at bus pin 52, supplying this voltage to other

boards on the bus. The -12 volts also supplies power to the -5 volt regulator (Q3), which provides regulated -5 volts to pins 21 and 54 of the bus.

The cartridge controller board and drive in the GDAS require +5 volts, +12 volts, and -12 volts. The +12 volts and the -12 volts are not regulated because this voltage only powers the motor in the cartridge drive, and it can operate on voltages ranging from 10.5 to 14.5 volts. The +12 volts enter the board on pin 7 of connector P1 and are passed through a 2-amp microfuse (F3) to protect the battery from overload. The -12 volts enter the board on pin 3 of connector P1 and pass through a 2-amp microfuse (F1) that protects the battery. The voltage inputs are separate from the ones described earlier, providing the option of using a separate battery to power the cartridge drive. The +12 volts also supplies power to the 10-amp adjustable regulator (Q1) that is set to a value of +5.1 volts under load (while the cartridge drive is recording data) with resistor R3. This regulated +5 volts powers the logic circuits of the cartridge controller board and drive, and is separated from the +5 volts described earlier to prevent any failures in the cartridge drive from affecting the operation of the rest of the system.

The GDAS is designed as a battery-powered system that operates for long periods of time in a remote environment, and under such conditions, the battery must last as long as possible to maximize the length of time the GDAS can record data. Since the cartridge drive requires 2.5 amps of power and is only needed when writing data to tape, the voltages are switched on and off through two relays located on the power interface board. The +12 volts, entering the board on pin 7 of connector P1, are connected to pins 3 and 4 of relay K2. The -12 volts, entering the board on pin 5, are connected to pins 9 and 10 of relay K2. When the relay is engaged, +12 volts exit the board on pins 7 and 8 of the bus, and the -12 volts exit on pins 9 and 10 of the bus. These lines, in turn, are connected via an external plug to the drive. The output of the +5 volt regulator (Q1) enters relay K1. The outputs from this relay exit the board on pins 4, 5, and 6 of the bus, and enter the cartridge controller board and the cartridge drive through an external connector that is wired directly to the bus. Control signals, used to activate the relay, are usually noisy and often prevent the relay from making solid contact. A diode is used to prevent current reversals which might cause the relay to reopen after closing, and a capacitor is used to filter the noise out of the control signal. Together these components "debounce" the action of the relay. Diode CR10 and capacitor C8 are used to debounce the action of relay K2, and diode CR12 and capacitor C9 are used to debounce the action of the relay K1. These relays are activated when the controller board sends the proper data word to the power interface board via the system bus. The controller board must do two things in order to switch the relays on or off: address the power interface board and send the data (or command) word. The controller board addresses the power interface board at address OFF H (hexadecimal) or:

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | bus address lines |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | binary value |
| 83 | 82 | 29 | 30 | 31 | 81 | 80 | 79 | bus pin #s connected |

These address lines are fed into the inputs of the 8-input, NAND gate U2. This NAND gate is a switch that goes low (0 volts) when all eight of its inputs are high (+5 volts), and high if any of the inputs are low. This,

along with control signals PWR* (pin 77 of the bus) and sOUT (pin 45 of the bus), enable data to be directed to the power interface board.

Two data words control the +12 volts and -12 volts to the cartridge drive through relay K2 and are sent by the controller board, via the data-out lines of the bus. The word to enable the +12 and -12 volts is 83 H or:

| DO7 | DO6 | DO5 | DO4 | DO3 | DO2 | DO1 | DO0 | bus data-out lines |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | binary value |
| 90 | | | | | | 35 | 36 | bus pin #s connected |

The data word to disable the +12 and -12 volts is 03 H or:

| DO7 | DO6 | DO5 | DO4 | DO3 | DO2 | DO1 | DO0 | bus data-out lines |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | binary value |
| 90 | | | | | | 35 | 36 | bus pin #s connected |

Data lines DO0, DO1, and DO7 are connected to the inputs of the 8-bit, addressable latch U3, which selects one of eight outputs depending on the logic states of the three inputs. DO0 and DO1 determine which of the eight outputs is to be changed, and DO7 determines the logic level of that output. In this case, output Q3 (pin 7 of U3) will switch on or off the +12 volts and -12 volts to the cartridge drive through transistor Q5.

Two data words can be sent by the controller board to control the +5 volts to the cartridge controller card and the cartridge drive. The data word that turns the +5 volts power on is 80 H or:

| DO7 | DO6 | DO5 | DO4 | DO3 | DO2 | DO1 | DO0 | bus data-out lines |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | binary value |
| 90 | | | | | | 35 | 36 | bus pin #s connected |

The data word that turns the +5 volts power off is 00 H or:

| DO7 | DO6 | DO5 | DO4 | DO3 | DO2 | DO1 | DO0 | bus data-out lines |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | binary value |
| 90 | | | | | | 35 | 36 | bus pin #s connected |

Data lines are connected to the inputs of U3 as described above. In this case, output Q0 (pin 4 of U3) will turn on or off the +5 volts to the cartridge controller and drive through transistor Q4. To prevent controller problems, the +5 volts should be turned on first, then the +12 and -12 volts. When power is turned off, the +12 volts and -12 volts is removed first, then the +5 volts. This prevents any stray tape movement during power up and power down.

## 1.3 SYSTEM TIMING

Timing is extremely important in geophysical data-acquisition systems, because the time-of-day is the only identifier for the data being acquired. To illustrate the timing requirements, consider an array of systems deployed in an area of earthquake activity. The recorded time-of-day determines the exact moment each system detects an earthquake, and the accuracy of this time, especially between systems, directly affects the accuracy in determining the location of the earthquake (epicenter). The earthquake can be viewed as a sinusoidal wave with a frequency of 10 hertz, for example, that travels through a medium (the upper crust of the

earth) at a velocity of 5 kilometers/second. Determining the epicenter location within a ten percent accuracy translates into measuring a 500-meter wavelength to a precision of 50 meters. Because the timing required to resolve this 50 meters is 10 milliseconds, all systems in the array must maintain time accuracy to within 10 milliseconds of each other in order to maintain the 50-meter accuracy.

The time-of-day in the GDAS is maintained by a clock located on the controller board. The accuracy of this clock is determined by the oscillator that provides the counting pulses to it. The frequency required to operate the GDAS, 2,097,152 hertz, is determined by the components that make up the system. At this frequency, the accuracy of the oscillator must be within .03 hertz for the time error to be no more than 10 milliseconds at the end of a 30-day experiment. This could be achieved by using an oven-controlled oscillator, which typically has an accuracy within 0.01 hertz. The drawback, however, in using this type of oscillator is the large power consumption needed for operation. Low power versions require 250 milliamperes of power, which is three times the power consumption of the remainder of the system. The GDAS, instead, uses a temperature-compensated oscillator that requires only 3 milliamperes of power. The accuracy of this oscillator is 0.3 hertz, which translates into a time accuracy of 100 milliseconds for a thirty day experiment. The controller board, however, provides a means of measuring the clock drift that corrects the time to within 10 milliseconds. The clock drift measurement will be discussed in greater detail later in this section. The oscillator (Y1) is located on the power interface board and provides the 2,097,152 hertz clock pulses to all boards on the bus via bus pin 49 (see Figure 12).

## 1.4 SYSTEM MONITORING

The GDAS provides a means of monitoring the operation of the system performance by displaying a number on a liquid crystal display (LCD) mounted outside the system bus. The monitor typically displays the number of data events that have been recorded on tape. This information is useful in determining that the system is operating and provides a means of determining tape usage. Obviously, the display is only useful in experiments where the system can be observed. In ocean-bottom applications, where monitoring the system is impossible, the LCD counter is not used. The power interface board contains the logic necessary to drive an LCD counter via commands sent through the bus from the controller board. The following is a description of the commands that control the LCD counter and the circuitry involved (see Figure 12).

The power interface board is addressed at 0FF H (hexadecimal), as described in section 1.2. Four data words can be sent by the controller board to control the action of the LCD counter. The data word to send a low (0 volts) to the LCD clock is 01 H or:

| DO7 | DO6 | DO5 | DO4 | DO3 | DO2 | DO1 | DO0 | bus data-out lines |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | binary value |
| 90 | | | | | | 35 | 36 | bus pin #s connected |

The data word that sends a high (+5 volts) to the LCD clock is 81 H or:

| DO7 | DO6 | DO5 | DO4 | DO3 | DO2 | DO1 | DO0 | bus data-out lines |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | binary value |
| 90 | | | | | | 35 | 36 | bus pin #s connected |

The data word that sends a low to the LCD reset is 02 H or:

| DO7 | DO6 | DO5 | DO4 | DO3 | DO2 | DO1 | DO0 | bus data-out lines |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | binary value |
| 90 | | | | | | 35 | 36 | bus pins #s connected |

The data word that sends a high to the LCD reset is 82 H or:

| DO7 | DO6 | DO5 | DO4 | DO3 | DO2 | DO1 | DO0 | bus data-out lines |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | binary value |
| 90 | | | | | | 35 | 36 | bus pin #s connected |

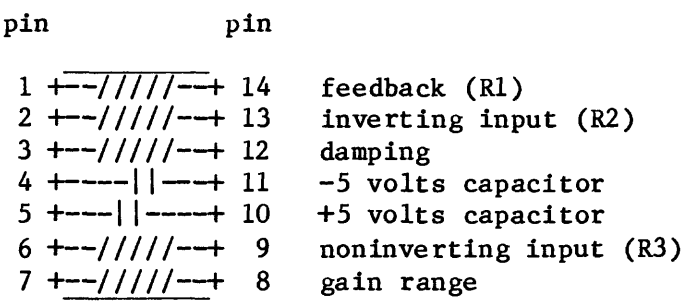
Data lines are connected to the inputs of U3, as described in section 1.2. In this case, output Q1 (pin 5 of U3) enters the LCD counter clock via pin 13 of the bus, and output Q2 (pin 6 of U3) enters the LCD counter reset via pin 14 of the bus. The LCD counter requires a falling edge (the drop from +5 to 0 volts) to increment, and a rising edge (the increase from 0 to +5 volts) to reset. In order to increment the counter, it is necessary to first set the clock high (+5 volts) and then set it low (0 volts). In order to reset the counter, it is necessary to first set the reset low and then set it high.

## 1.5 ANALOG SIGNAL CONDITIONING

The analog signal conditioning circuitry provides four functions: the amplification of the analog signals from the sensors, filtering of these signals, removal of DC offset, and waterbreak signal conditioning. This circuitry is contained on the preamplifier board and the analog board.

The analog signals from the sensors enter the GDAS on four connectors located on the preamplifier board (see Figure 14), and range in magnitude from less than one microvolt to 30 millivolts. The smallest signal detectable by the analog-to-digital board is 250 microvolts (see section 1.7), so signals must be amplified to increase the levels to the 250-microvolt detection limit of the analog-to-digital board. The preamplifier board amplifies the signals from the geophones in channels 1, 2, and 3 and from a hydrophone in channel 4. The preamplifiers U1 to U4 are low noise, wide bandwidth, instrumentation amplifiers set up to run on +5 volts and -5 volts. These amplifiers operate in two modes, inverting and noninverting. In the inverting mode, the amplifier output will be the reverse of the input: positive signals will be negative, and negative signals will be positive. This mode has a low input-impedence that can be adjusted using resistors located on the amplifier's input. The noninverting mode does not reverse the signal and provides an extremely high input-impedence. The amplifier is inverting for channels 1, 2, and 3 for best response with the resistive loads of the geophones. The gain and damping are set with resistors on headers located directly above each amplifier (see Figure 9). The amplifier is noninverting for channel 4 in order to maximize the response for the capacitive load of a hydrophone input. The gain and damping are set the same way as in the

other channels. The pin layout for these headers are as follows:




The gain of each amplifier for channels 1, 2, and 3 can be calculated by dividing the value of the feedback resistor (R1) by the value of the inverting input resistor (R2). The gain of the first three channels is set to ensure that the smallest signal levels from the geophones are increased to the 250-microvolt detection limit of the analog-to-digital board. The resistor values, used in this design, are R1 = 220,000 ohms and R2 = 825 ohms. The gain is, therefore, 266.6.

The voltage gain (VG) for the channel 4 amplifier is calculated using the equation:

$$VG = 1 + (R1/R2)$$

The hydrophone voltage output is approximately half that of the geophone voltage output, so the feedback resistor (R1) and the inverting input resistor (R2) for this amplifier are set to increase the hydrophone preamplifier output to that of the geophone preamplifiers. In this case, R1 = 5,760 ohms and R2 = 124 ohms. The gain is 466.

A damping resistor is required to maximize the response of the geophones. The damping resistor value is determined using the equation:

$$BT = BO + G^2/[4\,fm(R1 + R2)10^{-7}]$$

where BT is the total damping (for maximum flatness, BT equals 0.707), BO is the open circuit damping of the geophone, G is the transduction of the geophone (in volts/centimeter/second), f is the resonant frequency of the geophone (in hertz), m is the suspended mass of the geophone (in grams), R1 is the value of the damping resistor (in ohms), and R2 is the value of coil resistance of the geophone (in ohms). The value of each of these parameters depends on the specifications for the geophone used with the GDAS. The equation is solved for R1 to determine the damping resistor value. Once calculated, the resistor should be installed in the headers (R3 for channel 1, R8 for channel 2, and R13 for channel 3) as shown Figure 9. No damping is required for the hydrophone preamplifier (channel 4), but a 2 megaohm resistor (R18) is installed to provide a high input-impedance to the amplifier.

Digitizing an analog signal allows the data to be recorded more compactly than an analog recording does and with greater dynamic range, since a digitized signal can record a greater voltage range than is possible with analog recording. The drawback to digitizing the signals , however, is that some of the data are lost. At specific intervals of time, the magnitude of the analog signal is recorded as a digital word, and all data in between these intervals are ignored. If the magnitude is

not recorded often enough, a false image (or aliasing) results when the analog signal is reconstructed from the digital words. For example, the analog signal can be represented as a sinusoidal waveform (see Figure 2) containing a peak and a trough for each cycle. If the signal is not sampled at least twice per waveform, the reconstructed waveform will have a lower frequency. This false lower frequency signal will combine with the real lower frequency signals of the data, creating a false image in the reconstructed waveform. To eliminate this problem, all unwanted high frequency signals are filtered out of the analog data before digitizing using an anti-aliasing filter. This circuit filters out all signals with frequencies greater than one quarter of the frequency of the digitization rate, ensuring that the data will not be aliased.

The anti-aliasing filters are located on the analog board (Figure 12). After being amplified on the preamplifier board, the analog signals enter the analog board via connector J2. Connector J6 also provides a means for the analog signals to enter this board via the system bus, but is no longer used in this manner because the microvolt analog signals are unrecoverable in the electronic noise level present on this bus. The analog board contains four identical channels, each one having an anti-alias filter with cutoff frequencies determined by a resistor header. The filter circuitry is a lowpass, 8-pole Butterworth, active filter with 48dB/octave rolloff, composed of four, second-order active sections at unity gain. The Butterworth filter design was chosen because this design has the flattest response of any of the standard filter types. The cutoff frequency is set using header resistors CM1 thru CM4 (see Figure 8). The resistor value for the desired cutoff frequency can be calculated by using the equation

$$R = 4.961 \times 10^{6} / f$$

Where f = cutoff frequency in hertz and R = resistance in ohms. The cutoff frequency is determined by sample rate, which is the interval of time between digitization of the analog signals. The GDAS is capable of digitizing the signals at sampling rates of 1, 2, 4, and 8 milliseconds, which corresponds to sampling frequencies of 1024, 512, 256, and 128 hertz. The cutoff frequencies are calculated by dividing the sampling frequency by four, ensuring that at least four samples are digitized for each cycle of the analog signal. The resistor values are then calculated using the equation given above. Standard resistor values are used in the headers, so the actual cutoff frequency is modified to accommodate the use of standard resistor values. This is done by first calculating for the actual resistor value, selecting the closest standard value, and recalculating the cutoff frequency using that standard value. The following values can be used for the various sampling rates available:

| Sample Rate | Cutoff Frequency | Resistor Value |
|---|---|---|
| 8 milliseconds | 30 hertz | 165.0k ohms |
| 4 milliseconds | 60 hertz | 82.5k ohms |
| 2 milliseconds | 120 hertz | 41.2k ohms |
| 1 milliseconds | 248 hertz | 20.0k ohms |

After filtering, the signals leave the analog board through connector J7. This connector is actually a series of jumpers which provide the option to select one of three pins for each channel. The pin designations are as follows:

```
   CH1        CH2        CH3        CH4      GND
    |          |          |          |        |
 2  4  6    8 10 12   14 16 18   20 22 24    26     pin #

 1  3  5    7  9 11   13 15 17   19 21 23    25     pin #
 |  |  |    |  |  |    |  |  |    |  |  |     |
55 56 57   58 59 60   61 62 63   64 65 66    67     bus pin #
```

Pins 25 and 26 continue the ground line along the bus. In the four channel mode currently being used, pins 1 and 2 , 7 and 8, 13 and 14, and 18 and 19 are jumpered for signals leaving the board. These connections are also shown in Figure 14.

The amplifier and filter circuits in the GDAS generate a DC offset: a constant voltage that is added to the signal as it passes through each circuit. This offset, in effect, alters the zero-volt level of the analog signal above or below the zero-volt level of the system. This effect is magnified each time the signal is amplified and can reduce the ability of the analog-to-digital (A-D) converter to digitize the signal. For example, a 4 millivolt signal enters the analog-to-digital board with a DC offset of 1 millivolt added to it. If the gain-ranging amplifier amplified the this signal by a factor of 1024, the total signal level would be 5.12 volts. The A-D converter in the GDAS, which digitizes signals between -5 volts and +5 volts, could not digitize this signal and data would lost. With no DC offset, the resulting voltage would be 4.09 volts, which is well within operating range of the A-D converter. Buffer amplifiers located on the preamplifier board remove the DC offset to maximize the useful range of the signals digitized. The buffer amplifiers, setup as an inverting amplifier with unity gain, are the same for all four channels and use the quad-amplifier U5 (see Figure 12). By using the inverting mode, the geophones signals are inverted back to their original form, and the input-impedance becomes the value of the resistor on the input to each amplifier. Note that the hydrophone (channel 4) signals, however, are now inverted. The buffer amplifiers are used essentially as large resistors, forming a RC highpass filter; the capacitors are located on the output of each anti-aliasing filter. The cutoff frequency can be calculated using the following equation:

$$f = 1{,}000{,}000/2RC$$

where f is equal to the cutoff frequency, R is the resistance (150,000) in ohms, and C is the capacitance (2.2) in microfarads. These values were chosen so that each filter will block out any signal that is less than 3 hertz, including any DC offset.

The analog board also contains the circuitry for a waterbreak amplifier. This is a specialized circuit designed for applications where rectified, high-frequency data from a hydrophone are desired. Data of this type are useful in determining the average voltage level of the background noise and the average voltage level of any seismic data signal. The hydrophone (channel 4) preamplifier output provides the input to the waterbreak amplifier. This amplifier consists of a 4-pole

lowpass filter that attenuates all signals above 1800 hertz, a full-wave rectifier that converts the signal into a positive DC voltage, and a 6-pole highpass filter that attenuates all signals below 600 hertz. The output of this amplifier can be (1) recorded as a separate data channel, (2) routed to the event-detection circuitry to trigger the system on direct arrivals, or (3) summed with the anti-aliasing filter output of channel 4. The output options are configured using jumpers on connectors J3 and J4 as shown in Figure 14.

## 1.6 EVENT DETECTION

Event detection is one of the modes of operation for the GDAS. In this mode, the system does not record data until a seismic event has been detected. A seismic event is any signal that is at some predefined level above the background noise. This mode of operation is commonly used to detect earthquakes and to record refraction data where the timing of the signals are unknown. The GDAS contains the circuitry to detect these events on the analog board with a hardware event-detector (see Figure 3) that uses a short-term averager (STA) versus a long-term averager (LTA). The LTA circuit averages the observed signal level over a 5-minute time period and represents the magnitude of the background noise present as the GDAS waits for an event. The STA circuit averages the signal level over a much shorter time period (50 - 500 milliseconds, set via software control during system start-up) and represents the magnitude of all noise (background and events) detected by the GDAS. An event occurrs when the magnitude of the STA exceeds the magnitude of the LTA.

The hardware event-detection circuitry runs independently of the controller board (see Figure 13), so when an event has been detected, the board must signal the controller board through the INT* line (pin 73 of the bus). The event signal is also sent to the output port buffer U20, where it can be monitored by the controller board if the interrupt flag cannot be used. The data signal used by the event-detector originates from the channel 4 input. This input can originate at the output of the anti-aliasing filter circuit, or the waterbreak amplifier circuit, or the summation of both outputs using a summing amplifier (part of U13). These inputs are configured using jumper pads J3 and J4 as shown in Figure 8. The data signal then enters an integrating amplifier (part of U13), which provides additional filtration to ensure that the signal is within the frequency range required by the event-detector. There are three capacitors that can be connected to the feedback loop of this amplifier through jumper pad J5, and the choice of capacitor depends on the sampling rate used in the analog-to-digital board of the system. The following diagram shows the connections for J5 using the various sampling rates.

```
Jumper for .5 ms sampling          .__. ---||--- C53

Jumper for 1 or 2 ms sampling      .  . ---||--- C52

Jumper for 4 or 8 ms sampling      .  . ---||--- C51
```

The capacitor provides an additional 6 dB of attenuation to the higher frequencies filtered by the anti-aliasing filter. The signal enters the digitally controlled attenuator U22, in the feedback loop of an amplifier (part of U13), which serves as a gain-ranging device to increase the

dynamic range of the event-detector from 40 dB to 76 dB. The digital control for the attenuator comprises 6 bits from two binary counters (U21 and U25). The counting is controlled by a comparator (part of U12) set at 50 millivolts. As the signal level goes up, the gain is lowered; as the signal level goes down, the gain is increased. This circuit allows the event-detector to resolve small signals from a high background noise level.

The signal then passes through two integrating amps (part of U19) that act as lowpass filters to attenuate all signals above 1.69 hertz at the rate of 3 dB/100 hertz. This further filters the data to the frequency range of interest for event-detection. At the output of this filter, the signal splits into two directions: one path goes to the long-term averager and the other, to the short-term averager. The long-term averager (LTA) circuit is made of three amplifiers (U15) and an analog switch (U16). One of the amplifiers is used as a feedback amp to aid in holding the long-term average when the circuit is disabled. This decreases the time required for the LTA to reestablish an average after the event has occurred. The first of the two remaining amplifiers is a full-wave rectifier that adds the negative voltage of the signal to the positive voltage. The result, a wavy positive DC signal, goes into the second amplifier, which acts as a averaging "storage" device. The RC filter network and the feedback to the full-wave rectifier average the signal level over a period of time, creating a slowly changing DC signal level. This time period is calculated by simply multiplying the feedback resistor value, in ohms, by the feedback capacitor value, in farads. In the GDAS, the feedback resistor is 165,000 ohms and the capacitance is 1,700 microfarads, resulting in a time constant of 4.7 minutes. The LTA is disabled during an event to prevent the event signal from biasing the long-term average signal. The switch control logic, a flip-flop in U24, responds when the controller board sends the proper command to the bus. The command is enable when the controller board addresses the analog board at 11 H (hexadecimal) or :

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | sIN | sOUT | bus address lines |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | binary value |
| 83 | 82 | 29 | 30 | 31 | 81 | 80 | 79 | 46 | 45 | bus pin #s connected |

This address is determined by the switch settings of SW-2 (see Figure 8). The base of the analog board is set at 10 H (hexadecimal) to accommodate the existing software, and requires that the switch settings be as follows:

| 1 | 2 | 3 | 4 | switch no. |
|---|---|---|---|---|
| ._____._____._____./ . | | | | switch pos. |
| 0 | 0 | 0 | 1 | binary value |
| A7 | A6 | A5 | A4 | address lines |

Address line A3 is used to set the compare circuit enabling control of the board. A0, sOUT, and sIN are used to control data input and output from the analog board. In addition to the address, the controller board sends the command word on the data-out lines of the bus. To disable the LTA circuit, the data-out lines contain 01 H (hexadecimal) or:

| DO7 | DO6 | DO5 | DO4 | DO3 | DO2 | DO1 | DO0 | bus data-out lines |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | binary value |
| 90 | 40 | 39 | 38 | 89 | 88 | 35 | 36 | bus pin #s connected |

This command word enables the flip-flop output going to a comparator circuit (part of U12) which in turn disables the analog switch (U16). This action freezes the level of the LTA and stops the gain-ranging circuit. At this point the gain value of the digital attenuator is available to the controller board at the latch U20, which stores the gain word until it is read by the controller board. The address used by the controller board to read this data is 10 H or :

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | sIN | sOUT | bus address lines |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | binary value |
| 83 | 82 | 29 | 30 | 31 | 81 | 80 | 79 | 46 | 45 | bus pin #s connected |

The data are then presented to the bus on the data-in lines in the following format:

| | |
|---|---|
| DI0 | bit 1 of gain word |
| DI1 | bit 2 of gain word |
| DI2 | bit 3 of gain word |
| DI3 | bit 4 of gain word |
| DI4 | bit 5 of gain word |
| DI5 | bit 6 of gain word |
| DI6 | no value |
| DI7 | event flag |

Note that the event flag appears on DI7. If the interrupt flag sent by the analog board to the controller board is not used, the controller can determine when an event has occurred by continuously reading this port. The DI7 line will have a binary value of one if an event has occurred, and a value of zero if no event has occurred. This line must be polled continuously or the controller board will miss the event.

The short-term averager (STA) is identical in structure to the LTA circuit, except that the STA has no disable function and its time constant is adjustable. The STA circuit is made up of two amplifiers (part of U19) and an analog switch (U18). The analog switch is used to select a capacitor on CM-8, which determines the signal storage time. Selecting C61 yields a 0.54-second time constant; selecting C62 yields a 0.25-second time constant; selecting C63 yields a 0.11-second time constant; and selecting C64 yields a 0.05-second time constant. The capacitor is selected by the data lines that go into the analog switch which are connected to the input port (U14), allowing the STA to be selected by the controller board. This parameter can also be manually entered by installing switch SW3 (see Figure 8), which is in parallel with U14. The output of the STA circuit is fed into a comparator circuit (part of U12) along with the output of the LTA circuit. This comparator circuit also has an analog switch (U17) that selects a resistor in order

to set the threshold level of the event-detector. The selection of the threshold resistor is accomplished in the same manner as the STA value, but uses analog switch U17. Selecting R102 yields a threshold of 6 dB; selecting R101 yields a threshold of 12 dB; selecting R100 yields a threshold of 18 dB; and selecting R103 yields a threshold of 24 dB. In essence this resistor determines how much above the LTA signal level the STA signal level must be for the output to go high, indicating that an event has occurred.

To manually set the STA and threshold values to the event detector, install SW-3 and use the following switch settings:

| Switch No. | Value Selected |
|---|---|
| 1 | Threshold = 6 dB |
| 2 | Threshold = 12 dB |
| 3 | Threshold = 18 dB |
| 4 | Threshold = 24 dB |
| 5 | STA = 0.05 seconds |
| 6 | STA = 0.10 seconds |
| 7 | STA = 0.25 seconds |
| 8 | STA = 0.50 seconds |

Close one of the switches 1 to 4 to select a threshold, and close one of the switches 5 to 8 to select an STA value. The controller board selects the STA and threshold values by addressing the analog board at 10 H, as described earlier. These values are sent via the data-out lines in the following manner:

| DO7 | DO6 | DO5 | DO4 | DO3 | DO2 | DO1 | DO0 | bus data-out lines |
|---|---|---|---|---|---|---|---|---|
| | | | | 0 | 0 | 0 | 1 | Set THRESHOLD = 6dB |
| | | | | 0 | 0 | 1 | 0 | Set THRESHOLD = 12dB |
| | | | | 0 | 1 | 0 | 0 | Set THRESHOLD = 18dB |
| | | | | 1 | 0 | 0 | 0 | Set THRESHOLD = 24dB |
| 0 | 0 | 0 | 1 | | | | | Set STA = 0.05 sec. |
| 0 | 0 | 1 | 0 | | | | | Set STA = 0.10 sec. |
| 0 | 1 | 0 | 0 | | | | | Set STA = 0.25 sec. |
| 1 | 0 | 0 | 0 | | | | | Set STA = 0.50 sec. |
| 90 | 40 | 39 | 38 | 89 | 88 | 35 | 36 | bus pin #s connected |

The values are entered as one word, with the STA value filling the upper four data lines, and the threshold value filling the lower four data lines. This word also automatically enables the LTA circuit, allowing the event-detector to continue to operate. If more events are to be recorded, this data word must be sent after each event.

## 1.7 ANALOG-TO-DIGITAL CONVERSION

Converting an analog signal to a digital word allows the system to record data over a greater dynamic range Typical analog tape drives are capable of recording signals with a dynamic range of 48 dB. This means that if the maximum recorded signal is 10 volts, the smallest signal level that can be recorded is 39.1 millivolts. Digitizing the same 10 volts to a 20-bit number, as is done in the GDAS, produces a dynamic

range of 132 dB and the system can record a signal level as small as 8.3 microvolts. In remote operations where an unattended system must operate in environments of unknown background and data-signal levels, digitizing the analog signals is a significant advantage over analog recording.

The GDAS analog-to-digital (A-D) circuitry is located on the analog-to-digital board. This board consists of four identical channels of A-D conversion with the logic necessary to generate these conversions. Each channel contains a 10-bit floating-point amplifier, a sample-and-hold circuit, a 12-bit A-D converter, and output steering logic. The circuitry is shown in Figures 15, 16, and 17. Since all four channels are identical, the following discussion will refer to the channel 1 circuitry shown on figure 15. The first numeral in each IC label is an indication of channel. For example, IC U101 indicates channel 1; U401, channel 4.

Analog signals enter the board from two different locations. One entry point is through connector J3 (see Figure 10) in which the channel 1 analog signal enters on pin 1, channel 2 on pin 2, channel 3 on pin 3, channel 4 on pin 4, and the signal ground on pin 5. The second entry point is from the bus using connector J1. This is actually a series of jumpers that provide the option of selecting any three pins for each channel. The pin designations are as follows:

| CH1 | | | CH2 | | | CH3 | | | CH4 | | | GND | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | pin # |
| 1 | 3 | 5 | 7 | 9 | 11 | 13 | 15 | 17 | 19 | 21 | 23 | 25 | pin # |
| 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | bus pin # |

This configuration allows more than one A-D board to be used on the bus at one time, expanding the system to accommodate up to twelve channels. Pins 25 and 26 of the connector simply continue the ground line along the bus. In the four channel mode currently being used, pins 3 and 4, 9 and 10, 15 and 16, 20 and 21, and 25 and 26 are jumpered on the connector. This was done to correlate the inputs wired into the preamplifier board. Additional channels must be jumpered if more than one A-D board is used to pass data signals on through the bus, since the bus analog signal lines are not continuous.

The analog signal enters a gain-ranging amplifier, which extends the dynamic range of the system by providing an additional 10 bits to the digital word recorded for each sample. This corresponds to 60 dB of dynamic range that is added to the 72 dB of dynamic range provided by the 12-bit A-D converter. This circuit, developed in 1978 (Ambuter, 1979), consists of a programmable gain amplifier and a compare logic (see Figure 4) to maintain the signal level within defined limits. The compare logic automatically alters the gain of the circuit by changing the binary value loaded into the digital-to-analog converter in response to changes of the signal level. Although, the gain of the amplifier is set using 10 bits, the GDAS records a 4-bit code of the gain to conserve the amount of memory required to store each sample.

The 12-bit multiplying digital-to-analog (D-A) converter U106 is used as an attenuator to control the gain of amplifier U104 (see Figure 15). The D-A is a device containing 12-bits of binary input used to connect twelve resistors into the signal path. The binary input determines which

of the resistors is connected and sets the gain of amplifier U104. Only ten of the 12-bits of binary input are used to limit the maximum gain at 1024, and the minimum gain at 2. The D-A will decrement by a factor of two in response to an increase in signal level until a minimum gain of 2 is reached. The output of the amplifier is connected to the comparator U111, which consists of four circuits that compares the signal level with a reference voltage connected to each circuit. The four outputs indicate whether the signal level exceeds the reference voltage level at each input. One output (pin 13 of U111) is referenced at +2.2 volts and indicates a high (+5 volts) if the signal level exceeds +2.2 volts. The second output (pin 12 of U111) is referenced at -2.2 volts and indicates a high if the signal level is less (more negative) than -2.2 volts. The third output (pin 10 of U111) is referenced to +0.1 volts and indicates a high if the signal level exceeds +0.1 volts. The fourth output (pin 11 of U111) is referenced to -0.1 volts and indicates a high if the signal is less than -0.1 volts. Together, these four outputs determine the binary value that sets the gain of the amplifier. The first and second outputs are connected to an AND gate on U109, and the output (pin 11) of this gate indicates a low (0 volts) if the signal is not between +2.2 volts and -2.2 volts. The third and fourth outputs of the comparator are connected to a NAND gate on U110, and the output (pin 6) of this gate indicates a high if the signal is not between +0.1 volts and -0.1 volts. These two signals control the action of the 4-bit counter U108. The counter will increment (increase the gain) if the signal level is between +2.2 and -2.2 volts, and decrement (decrease the gain) if the signal is not within this range. The counter also stops counting (no gain changes) if the signal is between +0.1 and -0.1 volts, and continues counting (change the gain) if the signal is not within this range. The counter U108 is setup for decade counting to prevent the 4-bit output from exceeding a value of ten. The carry-out signal of this chip and the MAX output of U107 is used to inhibit counting after minimum or maximum count is achieved. The count will update every 7.63 microseconds providing enough time for the comparator to settle between gain changes. The counting rate originates from the 12-stage binary counter U22, which divides the system clock (pin 49 of the bus) to provide the desired rate (131,072 hertz). The 4-bit output of U108 is connected to the inputs of the BCD-to-decimal converter U107, which converts the output of the counter to one of ten steps that directs the D-A. Since the D-A is binary, each step is 6 dB; ten steps totals 60dB of dynamic range. Before the signal is digitized by the A-D converter, the gain-ranging amplifier is halted to prevent any gain changes that might occur while the A-D converter is digitizing the signal. The 4-bit gain word is then stored in the upper four bits of the 8-bit latch U103, which transfers this data to the bus along with the digital word generated by the A-D converter. Note that the 4-bit gain code (CODE) is a compressed value of the 10-bit binary value (GAIN) used to set the gain of the gain-ranging amplifier. The following equation illustrates the relationship between these two values:

$$GAIN = 2^{CODE}$$

The gain-ranging amplifier operates in a dynamic mode, in which the amplifier automatically adjusts its gain, or in a manual mode, in which the gain of the amplifier is fixed. These options are determined by the

controller board and transmitted through the system bus. The address required to communicate with the analog-to-digital board is 18 H (hexadecimal) or:

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | sIN | sOUT | bus address lines |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | binary value |
| 83 | 82 | 29 | 30 | 31 | 81 | 80 | 79 | 46 | 45 | bus pin #s connected |

This address is determined by the switch settings of SW-1 (see Figure 10). The base address of the analog-to-digital board is set at 18 H to accommodate the existing software, and requires that the switch settings be as follows:

| 1 | 2 | 3 | 4 | switch no. |
|---|---|---|---|---|
| ./ | .___. | .___. | .___. | switch pos. |
| 1 | 0 | 0 | 0 | switch val. |
| A4 | A5 | A6 | A7 | address line |

Address line A3 is used to set the compare circuit, enabling control of the board. sOUT and sIN are used to control the data input and data output from the analog board. In addition to the address, the controller board sends the command word on the data-out lines of the bus. The command word consists of the value needed to set the sample rate, a 4-bit gain word, and a manual/dynamic gain flag bit. The possible combinations are as follows:

| DO7 | DO6 | DO5 | DO4 | DO3 | DO2 | DO1 | DO0 | bus data out lines |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | | | | | Manual gain = 2 |
| | | to | | | | | | |
| 1 | 1 | 1 | 1 | | | | | Manual gain = 1024 |
| | | | | 0 | | | | Man/dyn flag = manual |
| | | | | 1 | | | | Man/dyn flag = dynamic |
| | | | | | 1 | 0 | 1 | Sample rate = 8 ms (128 hertz) |
| | | | | | 0 | 0 | 1 | Sample rate = 4 ms (256 hertz) |
| | | | | | 1 | 1 | 0 | Sample rate = 2 ms (512 hertz) |
| | | | | | 0 | 1 | 0 | Sample rate = 1 ms (1024 hertz) |
| | | | | | 1 | 0 | 0 | Sample rate = .5 ms(2148 hertz) |
| 90 | 40 | 39 | 38 | 89 | 88 | 35 | 36 | bus pin #s connected |

The upper four bits (DO4 to DO7) represent the 4-bit gain code used when the manual mode is selected, and is identical in structure with the gain code described above. The code is substituted for the 4-bit output of the binary counter U108. The DO3 line is the flag which indicates whether dynamic or manual mode is to be used. In the manual mode, the gain of the gain-ranging amplifier is fixed at the gain value entered in the upper four bits. In the dynamic mode, the gain will automatically adjust in response to the signal level and uses the output of the binary counter to set the gain. The lower three bits (DO0 to DO2) of the command word consist of the code necessary to set the sampling rate of the A-D converter. The sample rate will be discussed later in this section, but is presented now to fully describe the command word.

The analog signal from the gain-ranging circuit enters the sample-and-hold circuit which holds the signal level long enough for the A-D converter to digitize it. This circuit consists of the analog switch U20

and a 0.033 microfarad 1% capacitor that stores the signal level. When the switch is opened (i.e., on hold), the capacitor maintains the voltage for the A-D converter. When the switch is closed, the output of the sample-and-hold is the same as the output of the gain-ranging amplifier. The output of the sample-and-hold circuit contains the follower amplifier U105. This amplifier maintains a high-impedence output to the storage capacitor, preventing any extra loading of the capacitor that would result in a decrease in the signal level being stored.

The signal from the sample-and-hold circuit enters the A-D converter U101, which converts the magnitude of the analog signal to a 12-bit digital word. This device is set for bipolar, complimentary operation. Conversion is initiated by the timing logic and at completion, the digital word is sent to the 8-bit latches U102 and U103. The A-D converter sends a "conversion complete" signal to the timing logic when the digitization is complete; this, in turn, sets the interrupt flag to indicate to the controller board that data are ready. The controller board then reads the data from each of the four channels via the data-in lines of the bus. There are a total of sixteen bits of data (twelve from the A-D converter and four from the gain-ranging amplifier) for each channel, and since the data lines can only hold eight bits at a time, each channel must be read twice. The first eight bits, called the low byte, contain the lower eight bits from the A-D conversion, and are transferred to the bus in the following format:

Low Byte

| | |
|---|---|
| DI0 | bit 1 of data word |
| DI1 | bit 2 of data word |
| DI2 | bit 3 of data word |
| DI3 | bit 4 of data word |
| DI4 | bit 5 of data word |
| DI5 | bit 6 of data word |
| DI6 | bit 7 of data word |
| DI7 | bit 8 of data word |

The second eight bits, called the high byte, contain the upper four bits of the A-D conversion and the 4-bit gain code from the gain-ranging amplifier. The high byte is transferred to the bus in the following format:

High Byte

| | |
|---|---|
| DI0 | bit 9 of data word |
| DI1 | bit 10 of data word |
| DI2 | bit 11 of data word |
| DI3 | bit 12 of data word |
| DI4 | bit 1 of gain code |
| DI5 | bit 2 of gain code |
| DI6 | bit 3 of gain code |
| DI7 | bit 4 of gain code |

The analog-to-digital board responds to eight different addresses in order to provide the controller board with the means of reading all of the data. The following addresses send data from each channel of the A-D to the bus:

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | sIN | sOUT | bus address lines |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Low byte CH1 A-D |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | High byte CH1 A-D |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | Low byte CH2 A-D |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | High byte CH2 A-D |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | Low byte CH3 A-D |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | High byte CH3 A-D |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | Low byte CH4 A-D |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | High byte CH4 A-D |
| 83 | 82 | 29 | 30 | 31 | 81 | 80 | 79 | 46 | 45 | bus pin #s connected |

The timing required by the A-D board is the same as the digitization rate (called the sampling rate) of the A-D converter. The rate code is derived by the controller board and sent over the bus to the A-D board, as described above, where the code is stored in latch U13. The programmable counter U15 divides the clock pulse from counter U22 by the code stored in latch U13 to produce the sample rate clock. This clock initiates the action of U17, which is used as a shift register to control all of the steps required for conversion of a sample. The clock rate for each step is set at 65,536 hertz (15.26 microseconds) which is derived from U22. The following steps are required to convert a sample:

1. The gain-ranging amplifier is stopped to freeze the gain.
2. The sample/hold stores the signal level and the A-D is started.
3. Wait while A-D converts the sample.
4. Set up to send data on "Convert Complete" signal.
5. Disable the shift.

The "conversion complete" signal from the A-D converter sets the flip-flop U18, which sends a high (+5 volts) to the VIO interrupt (pin 4 of the bus). The interrupt is set low (0 volts) when the controller board reads the first data-byte from the analog-to-digital board.

## 1.8 PROGRAM CONTROL

The controller board is responsible for program control, storage of data in a circular memory buffer, communications to the user, time of day, and other input/output (I/O) functions. This board is based around the NSC-800 microprocessor, which was chosen because it is low power consumption and extensive instruction set, which reduces the amount of memory needed for the complex programs written to control the system. The board functions with a set of instructions (the software) encoded in the electrically programmable, read-only-memory (E-PROM) located on the controller board. Time-of-day is handled by a MM58167 real-time clock. An NSC-810A I/O controller handles 22 lines of bi-directional input and output, 128 bytes of random access memory (RAM), and two 16-bit timers. System memory consists of five 8 k-bytes of RAM. The circuits that

make up this board are illustrated in Figures 18 and 19.

The microprocessor (CPU) used in this system is an NSC800 (U7), an 8-bit processor, that is set up in a standard configuration with the exception of the power-down mode and the interrupt structure. The gate arrangement U28, designed to wake the CPU on an interrupt, has not worked reliably, so the power-down mode is not used. Since there is no capability to generate a clock interrupt for window modes, the CPU cannot power-down as it must stay awake to poll the clock. The CPU can be reset using the momentary switch (SW1) located on the power interface board (see Figure 7). This switch will reinitialize the controller board without removing power to the system. The switch brings the reset line (pin 75 of the bus) to ground, and is also connected to an external reset line (pin 17 of the bus) to allow the CPU to be reset by an external device.

The CPU is capable of operating with 3 different modes of interrupts: mode-0, mode-1, and mode-2, but operates using the mode-0 interrupt structure when first powered up. Interrupts are signal lines that are connected directly to the CPU. When high, they cause the CPU to jump to a specific software routine located in the controller board's EPROM. When, for example, the interrupt VIO sent from the analog-to-digital board to the CPU is high, the CPU automatically jumps to the part of the software that supplies the instructions for reading data from the A-D board. Mode-0 interrupts provide eight possible interrupts into the CPU. The software instruction "Restart 0" in this mode directs the CPU to the start of the program at power up. All interrupts generated in the GDAS system use mode-1 operation, which enables four possible interrupts to the CPU. This mode was chosen because fewer circuits were required to support it. These interrupts are also sent to the port B of the I/O controller U8 and NAND gate U28 in an attempt to use the power-down mode of the CPU. The interrupts are enabled by setting the appropriate bits of port C on U8 to prevent the CPU from accidentally shutting down. INTR* (pin 25 of U7) is normally high, so no external setting of this interrupt is necessary. RSTA (pin 22 of U7) is enabled by setting PC0 (pin 37 of U8) low, RSTB (pin 23 of U7) is enabled by setting PC5 (pin 34 of U8) high, and RSTC (pin 24 of U7) is enabled by setting PC3 (pin 1 of U8) high. PC1 (pin 38 of U8) can also be used to enable the power-down mode, which is currently not being used. The INTR* interrupt is used by the early termination button on the GDAS housing. This stops data acquisition and begins the program termination routines, which is done in software. RSTA interrupt is connected through U27 (a NOR gate) to the VIO interrupt (pin 4 of the bus) and is used by the A-D board to let the CPU know there are data available. RSTB interrupt is used by the output of timer 1 of U8. It is currently used as a error timer for the tape drive software routines. RSTC interrupt can be used by the incoming signal line of the RS232 port to wake the CPU if a terminal is connected. There is an additional input on the power-down mode gate which does not connect to the interrupts. This connection is from the timer 0 output and provides a means of waking up the CPU after a designated period of time. The nonmaskable interrupt (NMI) is connected to PC2 (pin 39 of U8) and can be used to change the system memory organization in system playback modes.

Communications to the RS232 terminal, the external satellite clock, and the internal RTC output are handled by the I/O controller U8, which has three ports available for I/O operations (labeled A, B, C). Port C is setup to initialize the interrupts as described earlier. Port B has

several functions, depending on which of the eight data lines are used. PB0 (pin 29) is used to transmit data to the RS232 connector (XMIT) via pin 28 of the bus and pin 8 of connector P2. Amplifier U15 is used as a driver to supply enough power to interface properly with any standard terminal. PB1 (pin 30) is used to enable U9 and U11 (data buffers to connector P3), which are currently not used. PB2 (pin 31) is used to reset the cartridge controller board via pin 65 of the bus. PB4 , PB5, and PB6 are used as inputs for the various interrupts as described earlier (PB4 for INTR*, PB5 for RSTA, and PB6 for the output of timer 0). PB7 (pin 36) receives the data from the RS232 connector (RCV) via pin 27 of the bus or pin 7 of connector P2 and through U15 which buffers the signals. Port A is setup as a general purpose parallel port. The design of the board indicates that all eight data lines go through data buffers U9 and U11, which are connected to P3. This, however, was never implemented. Instead, only three of the data lines are used and these are connected directly to connector P3. PA1 (pin 22) is connected to pin 2 of connector P3, and goes high when the real-time clock (U10) indicates that a second has elapsed. PA2 (pin 23) goes high when U10 indicates that a minute has elapsed, and is connected to pin 4 of P3. These two lines are used to determine the drift of the real-time clock. The outputs are connected to an oscilloscope and compared with the second and minute pulse from a satellite clock. PA5 (26) is an input by which the system can detect a pulse coming from the satellite clock that indicates a minute transition; it is connected to pin 6 of P3. This input is used by the system to synchronize the real-time clock with the satellite clock. There is also a provision at U1 for a relay that is activated when the data buffers were activated, but is not currently used.

The I/O controller has two timers available to the system. Timer 0 indicates a transition of one second. This timer uses the CPU clock (1,048,576 hertz) as a time base and, under software control, the clock is set up to divide by 64, producing a clock rate of 0.061 milliseconds. Preloading the clock with the hexadecimal value 3FFF H causes the counter to overflow once each second. Timer 1 has a time base of 256 hertz and is currently used as a time-out error trap for the cartridge drive.

The CPU uses all address locations from 3000 H to 3099 H to communicate with the I/O controller U8. A binary value of 0 in address line A15 enables the decoder U24, which enables one of the eight devices connected to its outputs as determined by the logic state of the three inputs. It is used in conjunction with decoder U23 to select all of the memory and I/O devices located on the controller board. Address line A15 is used to select U23 (a binary of 1) and U23 (a binary value of 0). Address lines A12, A13, and A14 provide the three inputs to both decoders and determine which of the sixteen devices connected to both decoders will be selected. In selecting the I/O controller U8, the address lines A12, A13, and A14 will contain binary values of 0, 1, and 1, respectively. Address lines A0-A11 are used to address a specific portion of the RAM or I/O that make up U8. The following is a list of the various locations in U8:

| ADDRESS LINES | | | | | | | | | | | | | | | | TOTAL | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | HEX VAL. | FUNCTION |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3000 | Start of Ram |
| | | | | | | to | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 307F | End of Ram |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3080 | Port A Data |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 3081 | Port B Data |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 3082 | Port C Data |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3083 | Control Reg. |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 3084 | Dir. - Port A |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 3085 | Dir. - Port B |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 3086 | Dir. - Port C |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3087 | Mode Reg. |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 3088 | Bit clr. - Port A |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 3089 | Bit clr. - Port B |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 308A | Bit clr. - Port C |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 308C | Bit set - Port A |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 308D | Bit set - Port B |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 308E | Bit set - Port C |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 3090 | Timer 0 LSB Reg. |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 3091 | Timer 0 MSB Reg. |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 3092 | Timer 1 LSB Reg. |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 3093 | Timer 1 MSB Reg. |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 3094 | Stop timer 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 3095 | Start timer 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 3096 | Stop timer 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 3097 | Start timer 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 3098 | Timer 0 mode |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 3099 | Timer 1 mode |

The total memory space available to the system is 57,344 bytes. The first 8,192 bytes of memory comprises the system EPROM U16, which contains the software needed to operate the system. 128 bytes of memory comprise the internal RAM of I/O controller U8, as described above. The rest of the memory is dedicated to the system RAMs, U2 thru U6. Only five fit on the CPU board, so a total system memory of 42,224 bytes is available to the programmer for data storage. Addressing the memory is done in the same manner as described above, using decoders U23 and U24. A binary value of 0 in A15 enables U24, and two binary values (000 and 001) in A14 through A12 selects the EPROM. All address locations from 0000 H to 1FFF H (hexadecimal) will communicate with the system EPROM U16. The only RAM device selected by U24 is U6, using two binary numbers (100 and 101) in A14 through A12, which means that all locations from 4000 H to 5FFF H will address system RAM U6. Decoder U23 selects the rest of the system RAM, which requires that A15 contain a binary value of 1. The binary values required to select each RAM device are as follows:

| ADDRESS LINE | | | | RAM DEVICE |
|---|---|---|---|---|
| A15 | A14 | A13 | A12 | |
| 1 | 0 | 0 | 0 | U5 |
| 1 | 0 | 0 | 1 | U5 |
| 1 | 0 | 1 | 0 | U4 |
| 1 | 0 | 1 | 1 | U4 |
| 1 | 1 | 0 | 0 | U3 |
| 1 | 1 | 0 | 1 | U3 |
| 1 | 1 | 1 | 0 | U2 |
| 1 | 1 | 1 | 1 | U2 |

All locations from 8000 H to FFFF H address the remaining system RAM. Hexadecimal values of 8000 H and 9FFFF H select U5; hexadecimal values of A000 H and BFFF H select U4; hexadecimal values of C000 H and DFFF H select U3; and hexadecimal values of E000 H and FFFF H select U2.

Real-time clock (RTC) U10 is used to keep track of time-of-day to within a millisecond. The time base originates with the CPU clock at a frequency of 1,048,576 hertz. This clock signal goes to the counter U14, dividing it to 32,768 hertz, and also passes through gates in U12 and U27 to allow for external start and reset of the RTC. This RTC uses a 5-bit address and a 8-bit data bus. All locations from 2000 H to 2017 H address the RTC. A value of 0 in A15 enables U24, and a binary value of 010 in A14 through A12 selects the RTC. Address line A0 through A11 are used to address a specific portion of the clock. The following is a list of the various locations:

| ADDRESS LINES | | | | | | | | | | | | | | | | TOTAL | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | HEX. VAL. | FUNCTION |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2000 | Milliseconds |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2001 | Tenths & hundredths sec. |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2002 | Seconds |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 2003 | Minutes |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 2004 | Hours |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 2005 | Day of week |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2006 | Day |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 2007 | Month |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 2008 | Latch - millisec |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 2009 | Latch - .xx sec |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 200A | Latch - sec. |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 200B | Latch - min. |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 200C | Latch - hour |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 200D | Latch - day of wk. |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 200E | Latch - day |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 200F | Latch - month |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 2010 | Interrupt status |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 2011 | Interrupt cmd. |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 2012 | Time reset |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 2013 | Latch reset |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 2014 | Time status |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 2015 | Start reg. |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 2016 | Standby interrupt |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 2017 | Test |

The above latches are used for a programmed interrupt, which is not used in the GDAS. The clock is started by loading the current time during parameter entry. Synchronizing this time with a satellite clock is done using the procedure described earlier.

## 1.9 DATA RECORDING

Acquired data are stored on a cartridge tape recorder which has a data capacity of 17.5 megabytes. This system consists of a Digidata-6440 tape drive coupled with an Alloy IDXS-100 controller board. The cartridge controller accepts data in 8,192 byte blocks, writes the data to tape, and performs read-after-write verification. The cartridge write operation is transparent to the controller board allowing continuous digital data logging at 8192 bytes per second. Refer to the instruction manuals that accompanys these devices for any discussion of operations.

## 2. SYSTEM TESTING

The following section describes testing procedures for each circuit board of the GDAS that should be done prior to any usage of the system. The procedures in this section will refer to connector and other part numbers in describing locations of test points. These part numbers are referenced to the numbers printed on the circuit board being tested and examination of the circuit board will aid in locating these test points.

### 2.1 TESTING THE POWER INTERFACE BOARD

There are six tests that must be done to verify proper operation of the power interface board. The use of a voltmeter, 10-digit frequency counter, and a Rubidium (Rb) frequency standard are necessary to conduct these tests. The system must have all boards connected and an EPROM installed on the controller board.

Input Voltage - This checks the input voltages entering the power interface board to verify that the proper voltages are present before going on to other tests. The power source, whether it is a battery or other power supply, must provide two direct current (DC) voltages to the power interface board. These voltages must be a minimum of +12 volts and -12 volts to adequately power the system. These voltages must not exceed +15 volts or -15 volts, or damage will result to the tape drive. The power source must have an 8-pin, female, Molex connector to mate with the connector J1 (see Figure 7) on the power interface board. This connector must be terminated as follows:

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | pin no. |
|---|---|---|---|---|---|---|---|---|
| BLNK | +12v | -12v | BLNK | -12v | GND | +12v | GND | voltage |

The blank keys prevent accidental misallignment when connecting this plug to the power interface board. Insert the plug and measure the voltages on the lower pins of J1. If the proper voltages are not present, check the power source for proper operation.

Bus Voltages - Voltages for the bus are located on bus pin 1 for the +5 volts, pin 54 for the -5 volts, pin 2 for the +12 volts, and pin 52 for the -12 volts. The +5 and -5 voltages should be within 0.15 volts of the given value. Both 12 volt values will read equal to the power source voltage levels as there is no 12-volt regulation. If the proper voltages are not present, refer to section 4.1 for troubleshooting.

Logic Supplies - In setting up the GDAS for operation, it is necessary to determine that the proper voltages are getting to each of the boards present in the system. Figures 8 to 11 show the location for measuring the voltages on each board. If the voltages are not present check the system bus connections.

Cartridge Drive Voltages - The measuring points for the cartridge drive voltages are at bus pins 4, 5, and 6 for the +5 volts, bus pins 7 and 8 for the +12 volts, and bus pins 9 and 10 for the -12 volts. These voltages are not sent to the cartridge drive until the two relays on the power interface board (see Figure 7) have been activated. There should be no voltage on any of the pins when the relays are open. If the proper

voltages are not present when the relays are activated, refer to section 4.2 for troubleshooting.

Oscillator - The system must be powered up for two hours to allow time for the oscillator to equilibrate. An 10-digit frequency counter, using a 10 MHz Rb standard as an external reference, is set up to measure the output of the oscillator. The probe of the counter should be connected to the test point of the oscillator as shown in Figure 7. Using the screw located on the top of the oscillator (under the screw cap), adjust the frequency to the value written on the oscillator. Be careful that no pressure is being exerted on the adjustment screw when the frequency count is being read. The adjustment should be made to within 0.1 Hz.

Reset Switch - The system should have a program E-PROM on the controller board and a terminal connected to the RS232 connector on the electronics rack (see Figure 6). Just push the reset button (see Figure 7) and see if the program will restart. The screen on the terminal should clear and display the system ram test. If this does not occur, refer to section 4.1 for troubleshooting.

## 2.2 TESTING THE PREAMPLIFIER BOARD

Testing the preamplifier board requires that you verify preamplifier operation and buffer amplifier operation. The use of an oscilloscope and a function generator are necessary for these tests.

Preamplifier - Apply a 10-millivolt, 20-Hertz sine wave to the input of each channel ( J2 is channel 1; J3 is channel 2; J4 is channel 3; and J5 is channel 4 - see Figure 9). Using the oscilloscope, measure the output of the preamplifier for each channel by connecting the scope probe on the output connector (J1). Channel 1 is pin 5; channel 2 is pin 4; channel 3 is pin 3; and channel 4 is pin 2. The gain of the preamplifier for channels 1, 2, and 3 is 266, so the output should be a sine wave with a magnitude of 2.66 volts. The gain on channel 4 is 466, so the output should be 4.66 volts.

Buffer Amplifier - First verify the operation of the analog board as described in section 2.3. Repeat the tests described above in the preamp section. To monitor the output of the buffer amps, connect the scope probe to the input connector (J3) on the A-D board (see Figure 10). Channel 1 is pin 1, channel 2 is pin 2, channel 3 is pin 3, and channel 4 is pin 4. The results should be the same, although the magnitude will drop slightly due to the filters.

Sensor Monitoring - In setting up the GDAS for deployment, it is possible to monitor the signals from the sensors to verify proper operation. Place the scope probe on the appropriate pins of J3 as described in testing the buffer amplifier, and connect the four sensor cables to the preamplifier board as illustrated in Figure 9. By tapping on the sensors, the waveforms shown on the oscilloscope should indicate the response of the sensors after being amplified, filtered, and the DC offset removed.

## 2.3 TESTING THE ANALOG BOARD

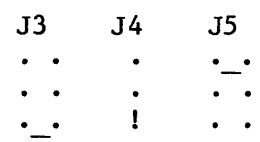
Testing the analog board requires that you verify filter response and operation of the event-detection circuits. The use of an oscilloscope, a signal generator, a +5 and -5 volt power supply, a logic signal generator, and an extender card are necessary for these tests.

Board Verification - Check the jumpers for proper connection on the analog output connector J7 as described in section 1.5. The filter cutoff frequency is set by installing resistor headers in CM1, CM2, CM3, and CM4 (see Figure 8). The following values can be used for the various sampling rates available:

| Sample Rate | Cutoff Frequency | Resistor Value |
|---|---|---|
| 8 ms | 30 Hz | 165.0 k-ohms |
| 4 ms | 60 Hz | 82.5 k-ohms |
| 2 ms | 120 Hz | 41.2 k-ohms |
| 1 ms | 248 Hz | 20.0 k-ohms |

Anti-Aliasing Filter - Apply a 20-hertz sine wave to the input connectors of each channel (located on the preamplifier board) as described in section 2.2. Attach a voltmeter or scope to the output of the filter (TP5 for channel 1; TP6 for channel 2; TP7 for channel 3; TP8 for channel 4 - see Figure 8). Then adjust the voltage level of the input so that the output equals 1 volt. Gradually increase the frequency of the sine wave until the output voltage equals 0.707 volts. This value should be 33 Hertz for the 156 k-ohm header; 66 Hertz for the 82.5 k-ohm header; 132 Hertz for the 41.2 k-ohm header; or 264 Hertz for the 20 k-ohm header. If the proper response is not observed check the capacitors used in the filter circuit.

Event Detector - Remove U14 and U26 (see Figure 8) and apply a 0.05-Hertz, 5-volt, signal to pin 1 of U26. Install jumpers on J3, J4, and J5 as follows (see Figure 8):




Install a dip switch in SW-3 and set SW3-1 and SW3-5 in the closed position with the rest in the opened position. Check the settings on the addressing dip switch (SW-2) to ensure that all positions are closed except SW2-4, which is opened. Reset the system by pushing the reset button on the power interface board (see Figure 7). Apply a 20-Hertz sine wave to the input of channel 4, and adjust the amplitude to read 1 volt at TP16 (see Figure 8). Reset the system again. Wait 20 minutes and measure the voltage at TP15, which should be between 40 and 60 millivolts. Increase the input by 20db. The voltage at resistor R104 should go high to +5 volts, and then after a short delay drop to -5 volts.

## 2.4 TESTING THE ANALOG-TO-DIGITAL BOARD

This test requires a function generator, all boards installed in the system, an EPROM installed on the controller board, and some means of playing back the data recorded on tape. As an example, Ocean Bottom Seismometer operations use the OBS EPROM (Miller, 1986) and display the recorded data on the OBS playback system (Fredricks, et al, 1984). This test provides a means of evaluating the response of the analog-to-digital board under the experimental conditions determined by the operating software.

Board Verification - Check the jumpers for proper connection on the analog input connector J1 (see Figure 10) and the switch settings of the board addressing switch SW-1, as described in section 1.8.

Analog-to-Digital Conversion - Refer to the operating instructions for the particular EPROM installed in the GDAS to program the system for three, separate series of experiments. The first series is set to record several events with the inputs to all four channels shorted (a wire is connected from the signal input pin to ground) at the input connectors J2, J3, J4, and J5 located on the preamplifier board (see Figure 9). The second series is set to record several events with a 20-Hertz, 20-microvolt (peak-to-peak) signal on each channel. This should be done one channel at a time, using the input connectors located on the preamplifier board, with the other channels shorted. The third series is set to record several events with a 20-Hertz, 20-millivolts (peak-to-peak) signal on each channel. Again, test one channel at a time with the other channels shorted. Refer to the operating instructions for the playback system being used to determine the magnitude of the data recorded on tape. Compare the recorded signals with the signal entered into the system for each series. The first series should give a good indication of the system noise level. Series two and three should give a good indication of the minimum and maximum response of the A-D board. If no signal was recorded, refer to the troubleshooting guide in section 4.5.

## 2.5 TESTING THE CONTROLLER BOARD

Testing of this board is done while using the system software. At power-up, the software automatically checks the registers of the microprocessor. If there is a failure, a "bad processor" message will be displayed on the terminal. There is also a test for the system memory built into the software, which is also done at power up, that will display any errors found to the terminal.

Clock Drift - Connect the satellite clock to the CPU board as shown in Figure 6. Connect the satellite clock seconds output to channel 1 on the oscilloscope and connect the GDAS seconds output (as described in section 1.8) to channel 2 on the scope. Set the scope to trigger off of channel 1. The system program should be terminated at this point by pushing the early termination button (see Figure 6). The time of day from the GDAS will display once a second on the screen. Compare this time with the time shown on the satellite clock, and measure the clock drift on the scope to determine the number of milliseconds the time of the GDAS has drifted from the satellite clock time.

## 2.6 TESTING THE CARTRIDGE CONTROLLER BOARD

The cartridge controller is tested by the system software by automatically writing a test record and then reading it back. The pattern read from the tape is compared to the pattern in system memory. If this test fails, the message "BAD TAPE" will appear on the terminal.

# 3. SYSTEM SETUP

The following section describes the steps necessary to start up and terminate the data-acquisition system. When programming the system, refer to the software instruction manual that pertains to the EPROM being used in the controller board.

## 3.1 STARTUP

A. Check to be sure that all boards are located in the proper slots in the electronics rack, and that a ribbon connector is installed between the preamplifier board and the analog board (see Figure 5).

B. Remove the analog card, and check that resistor headers CM1, CM2, CM3, and CM4 are the proper ones for the sampling rate desired (see Figure 8). For an 8-ms rate, use a 162k-ohm header; for a 4-ms rate, use a 82k-ohm header; for a 2-ms rate, use a 41k-ohm header, and for a 1-ms rate, use a 20.5k-ohm header. Reinstall the analog card.

C. Verify that the proper E-PROM is installed in the controller card (see Figure 11).

D. Connect a power source (battery or power supply) to the 8-pin connector located on the power interface board and check the the voltages as described in section 2.1.

E. Attach the four sensor connectors to the preamp board (see Figure 9).

F. Check the logic supply voltages (+5 volts and -5 volts) and cartridge supplies as described in section 2.1.

G. Clean the tape head of the drive using a cotton swab and denatured alcohol. Install a tape into the drive.

H. Check the signal response for each of the sensors at the connector J3 of the A-D board as described in section 2.2.

I. Let the system sit powered-up for 2 hours, then adjust the oscillator as described in the section 2.1.

J. Connect the RS232 cable from a standard computer terminal to the RS232 connector on the GDAS electronics rack (see Figure 6). The terminal should be setup for space parity, 7 data bits, 1200 baud, 1 stop bit, and no handshake lines.

K. Connect the cable from the satellite clock (if used) to the connector located on the controller card (see Figure 6).

L. Reset the system by pushing the reset button on the power interface board (see Figure 6).

M. Enter program parameters as per software instructions. Note: Disconnect the satellite clock during the tape test.

## 3.2 TERMINATION

A. Connect the terminal and push the early terminator button (see Figure 6).

B. Terminate the system program as per software instructions.

C. Check clock drift and oscillator frequency as described in section 2.1 and 2.5.

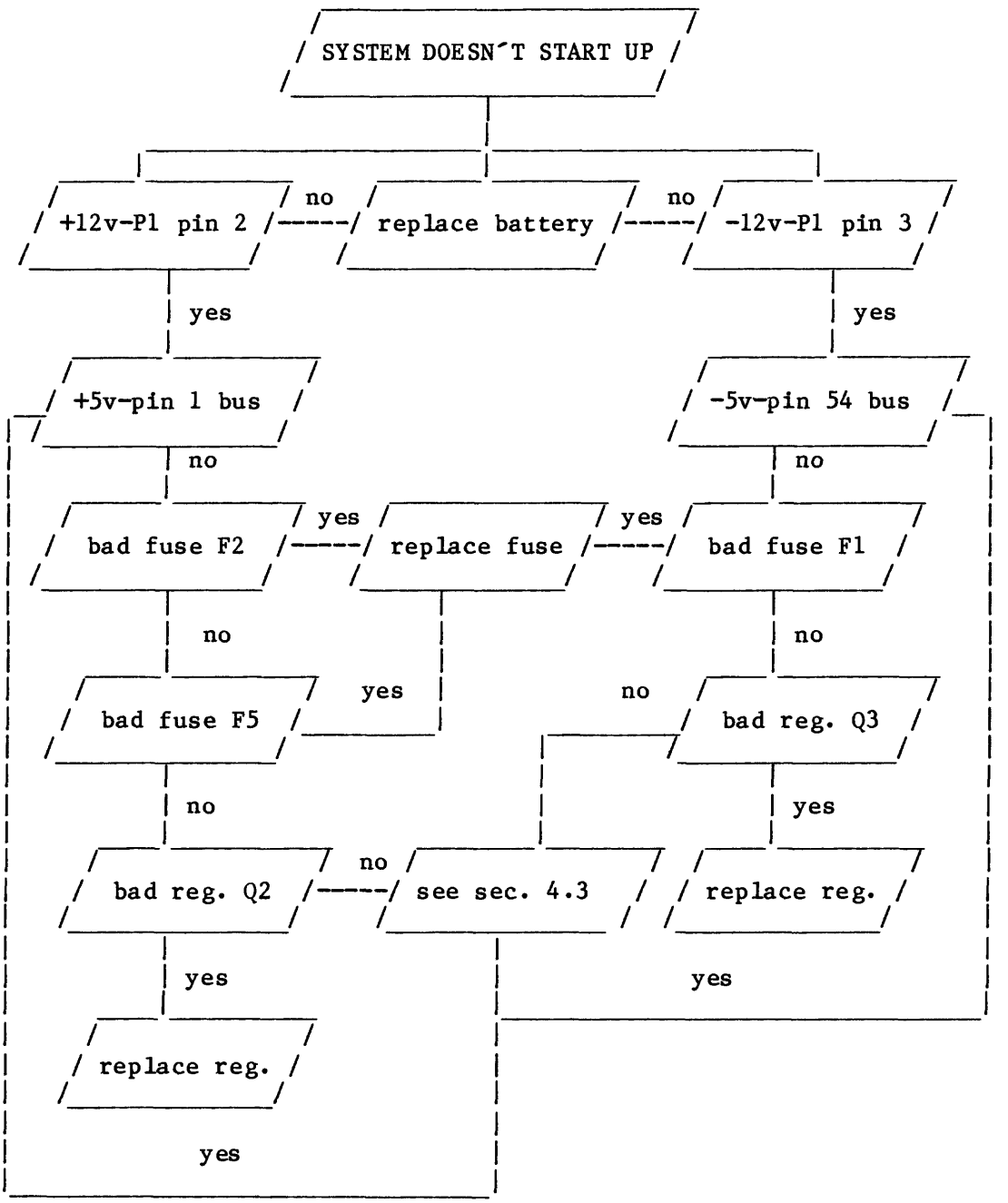
D. Remove and label the tape.

E. Measure the logic and battery voltages, as described in section 2.1.

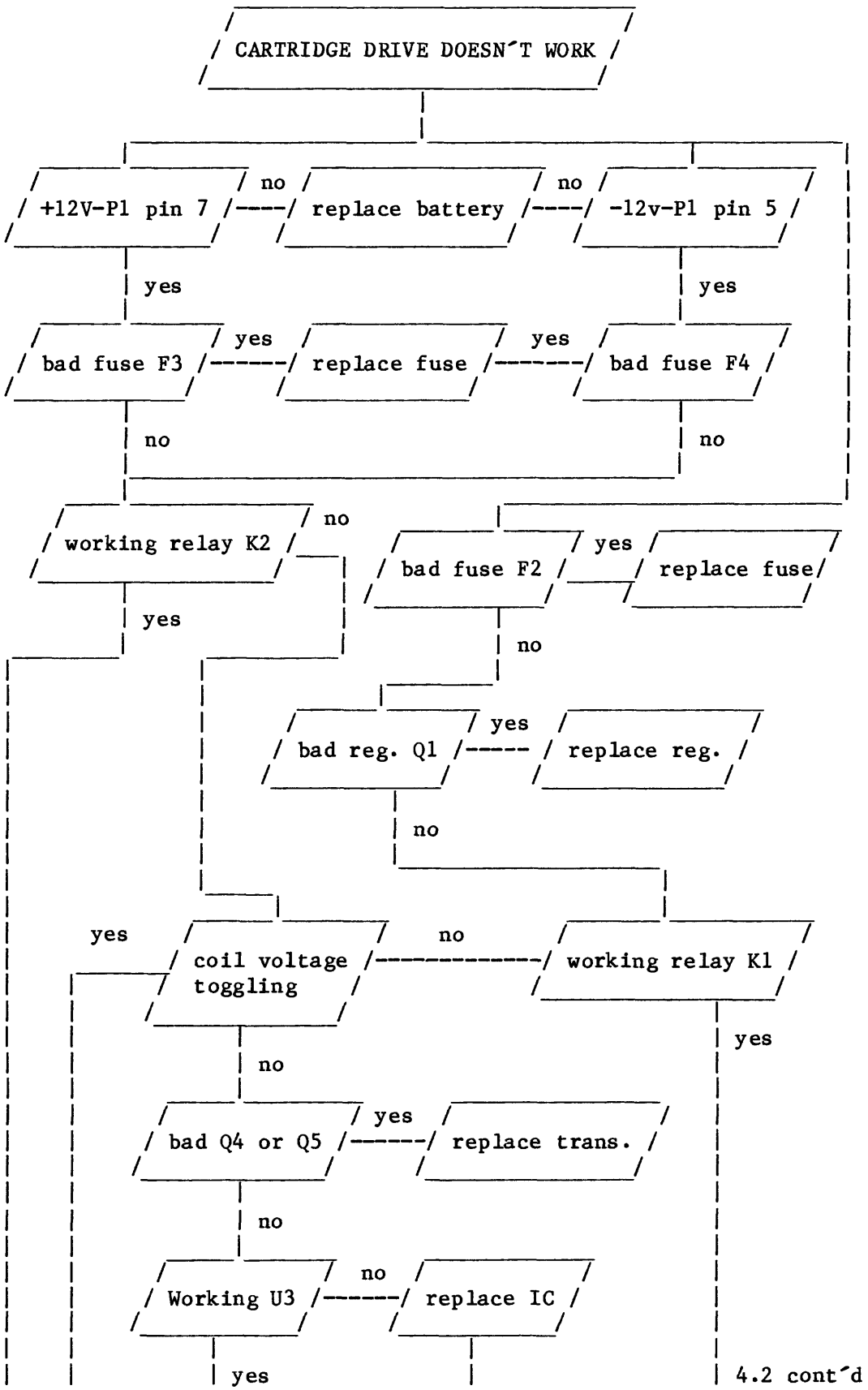
F. Remove the power.

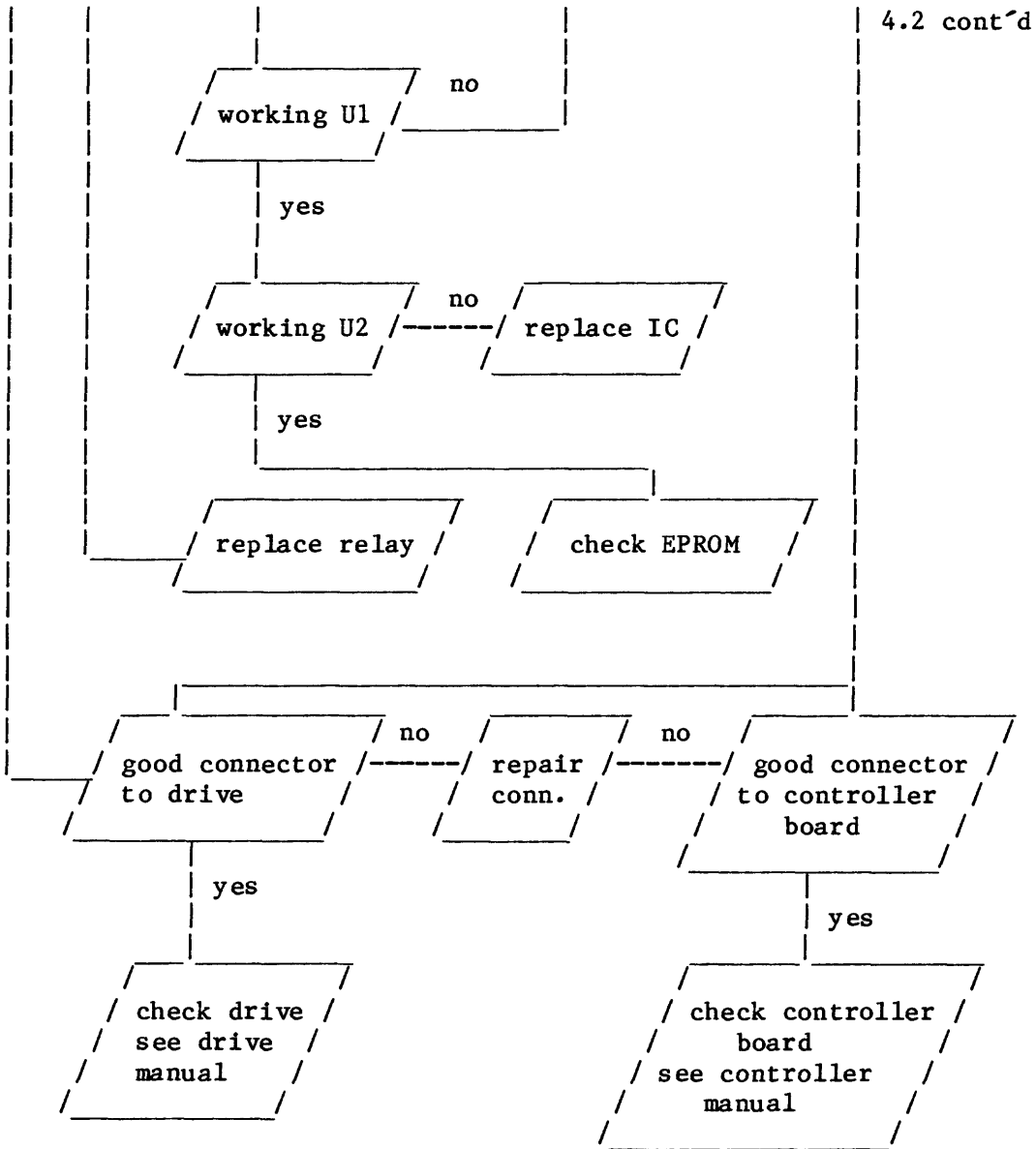
# 4. TROUBLESHOOTING

## 4.1 TROUBLESHOOTING HINTS FOR THE SYSTEM POWER

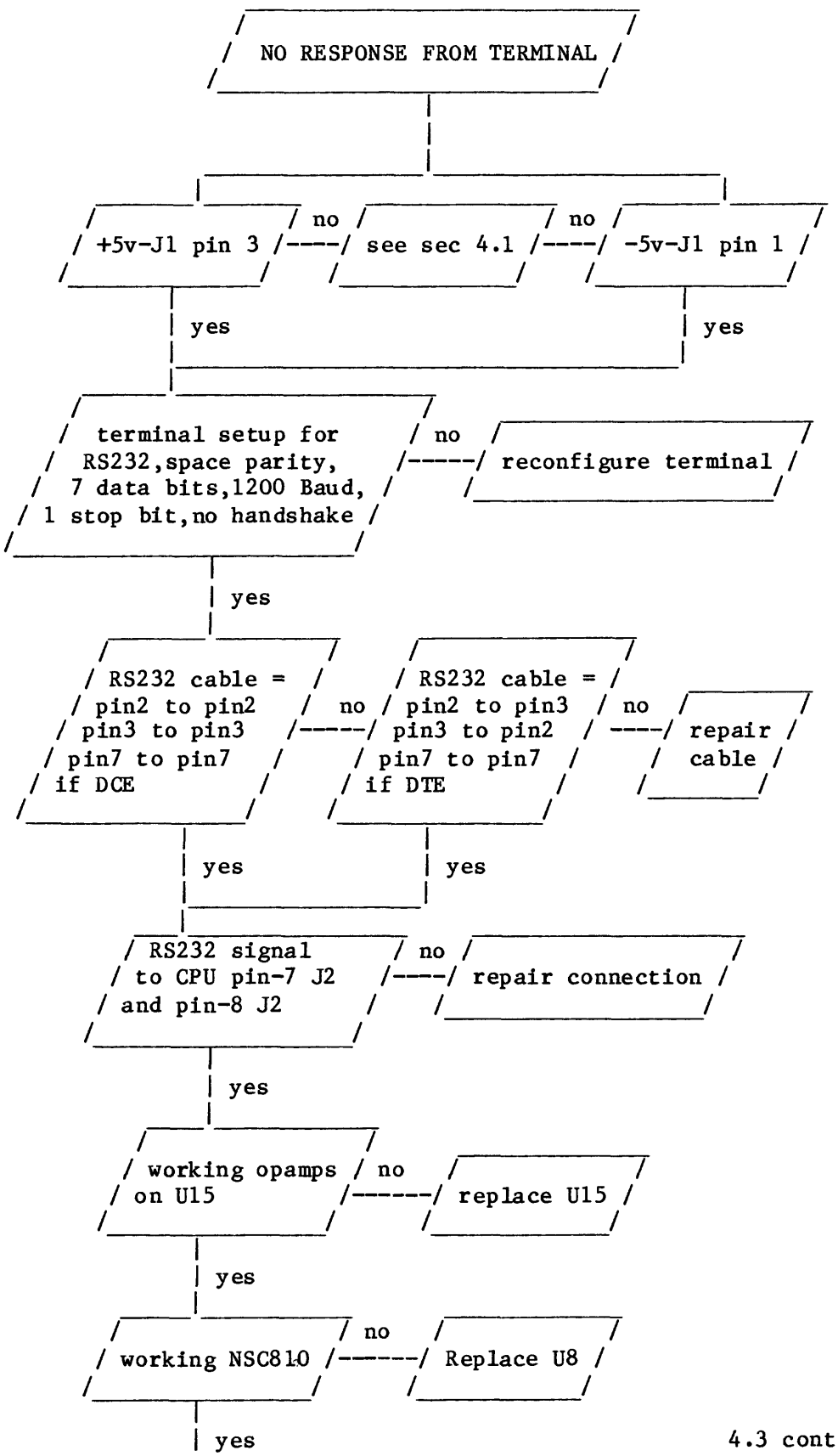


## 4.2 TROUBLESHOOTING HINTS FOR THE CARTRIDGE DRIVE



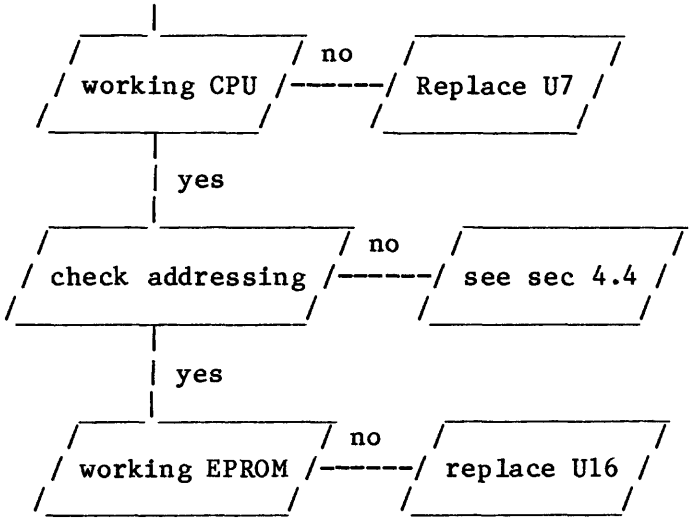

4.2 cont'd
working U1
no
yes
working U2
no
replace IC
yes
replace relay
check EPROM
good connector to drive
no
repair conn.
no
good connector to controller board
yes
check drive see drive manual
yes
check controller board see controller manual

## 4.3 TROUBLESHOOTING HINTS FOR THE CONTROLLER BOARD

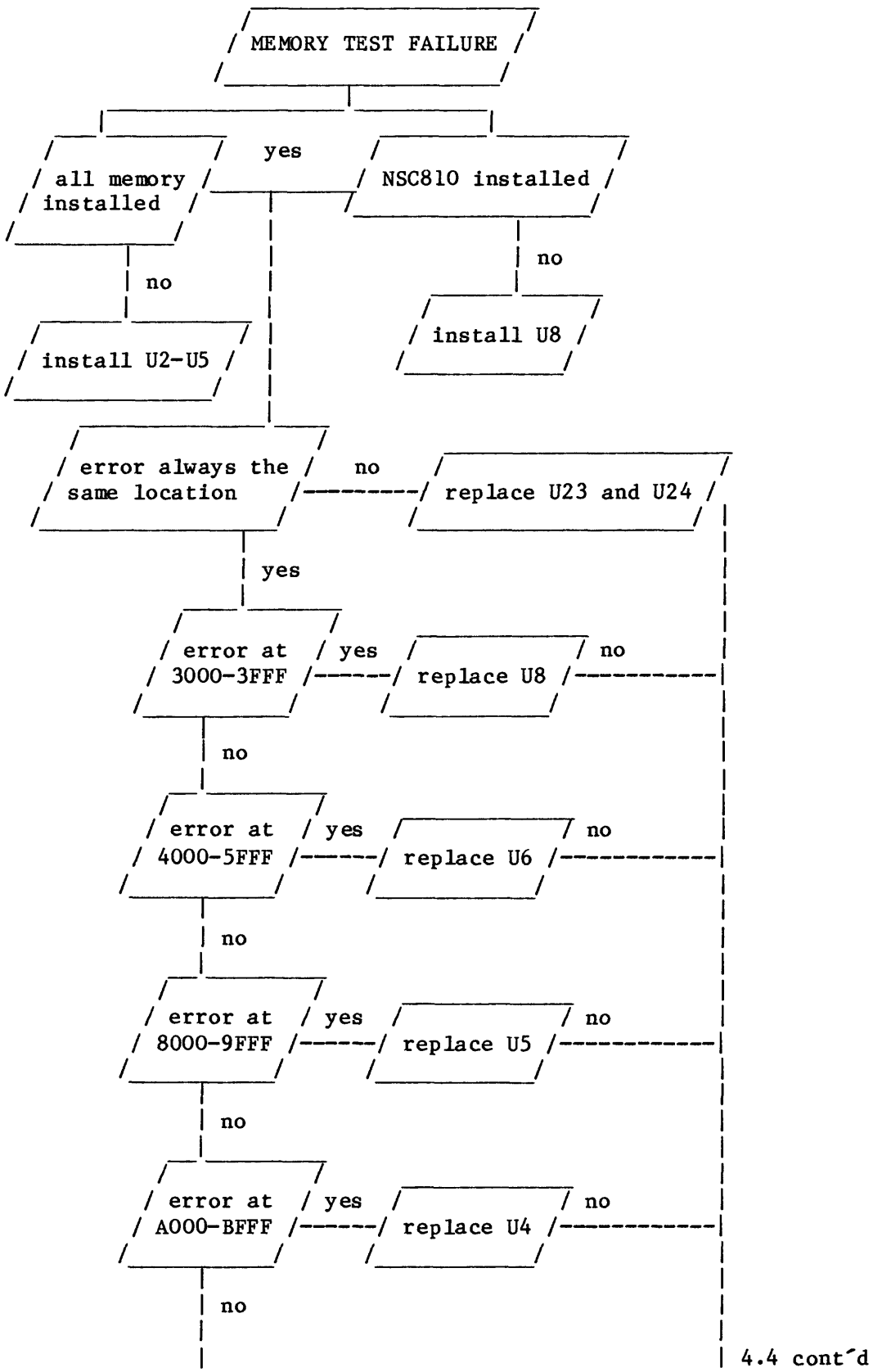



4.3 cont'd

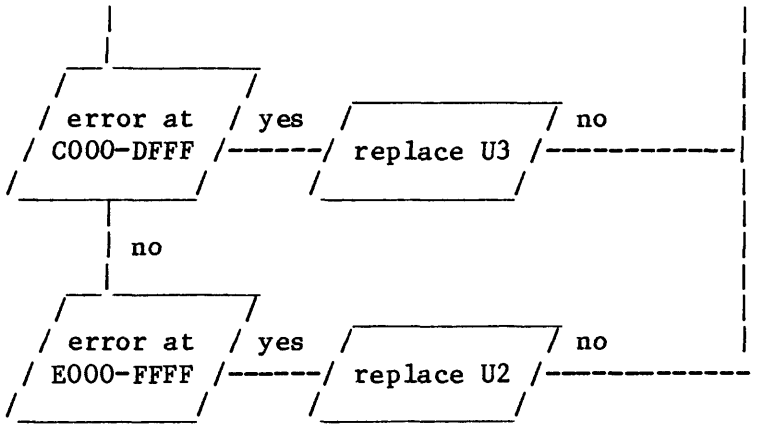
4.3 cont'd


working CPU
no
Replace U7
yes
check addressing
no
see sec 4.4
yes
working EPROM
no
replace U16

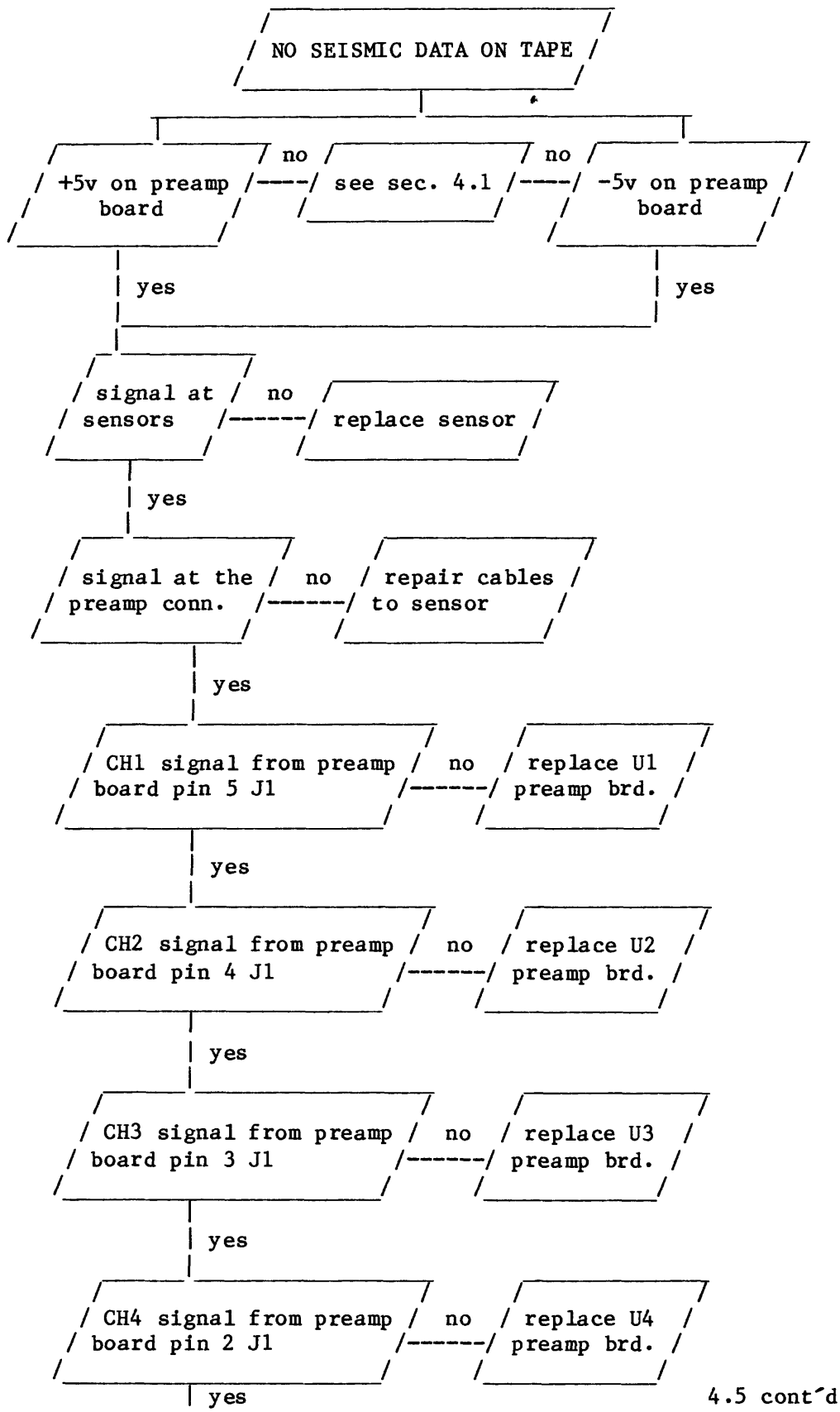
## 4.4 TROUBLESHOOTING HINTS FOR SYSTEM MEMORY



4.4 cont'd

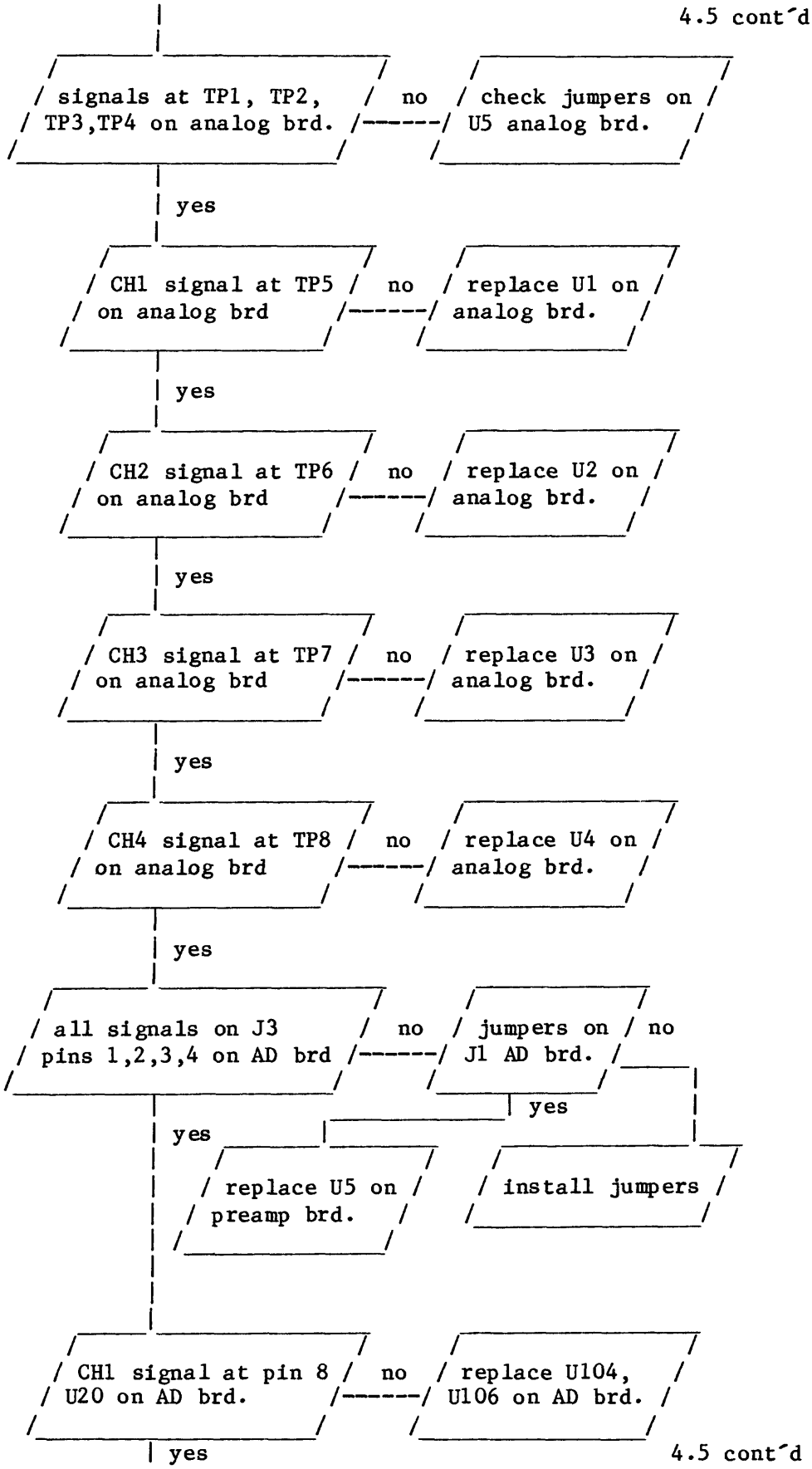

error at C000-DFFF
yes
replace U3
no
error at E000-FFFF
yes
replace U2
no

## 4.5 TROUBLESHOOTING HINTS FOR THE ANALOG SIGNAL



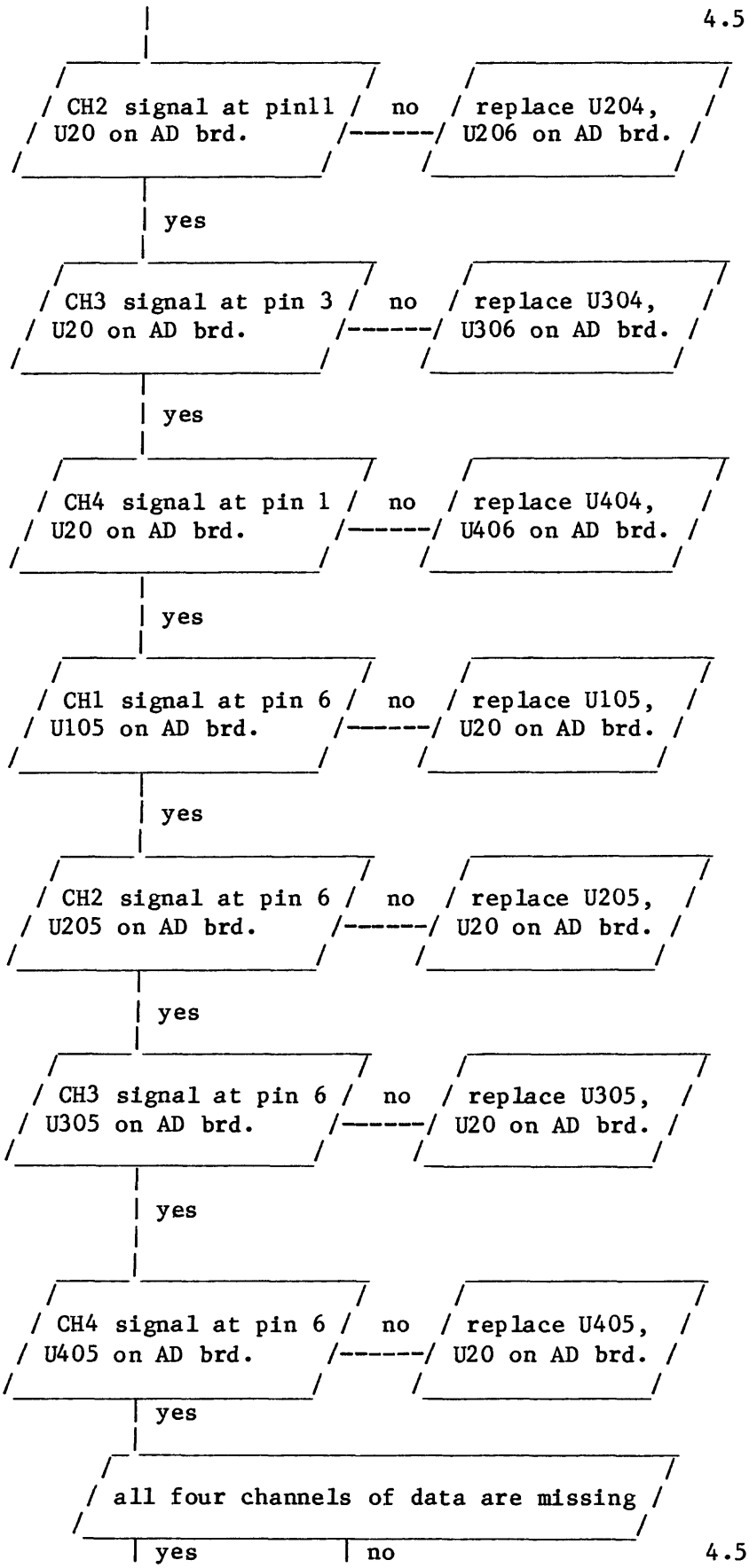

4.5 cont'd

4.5 cont'd

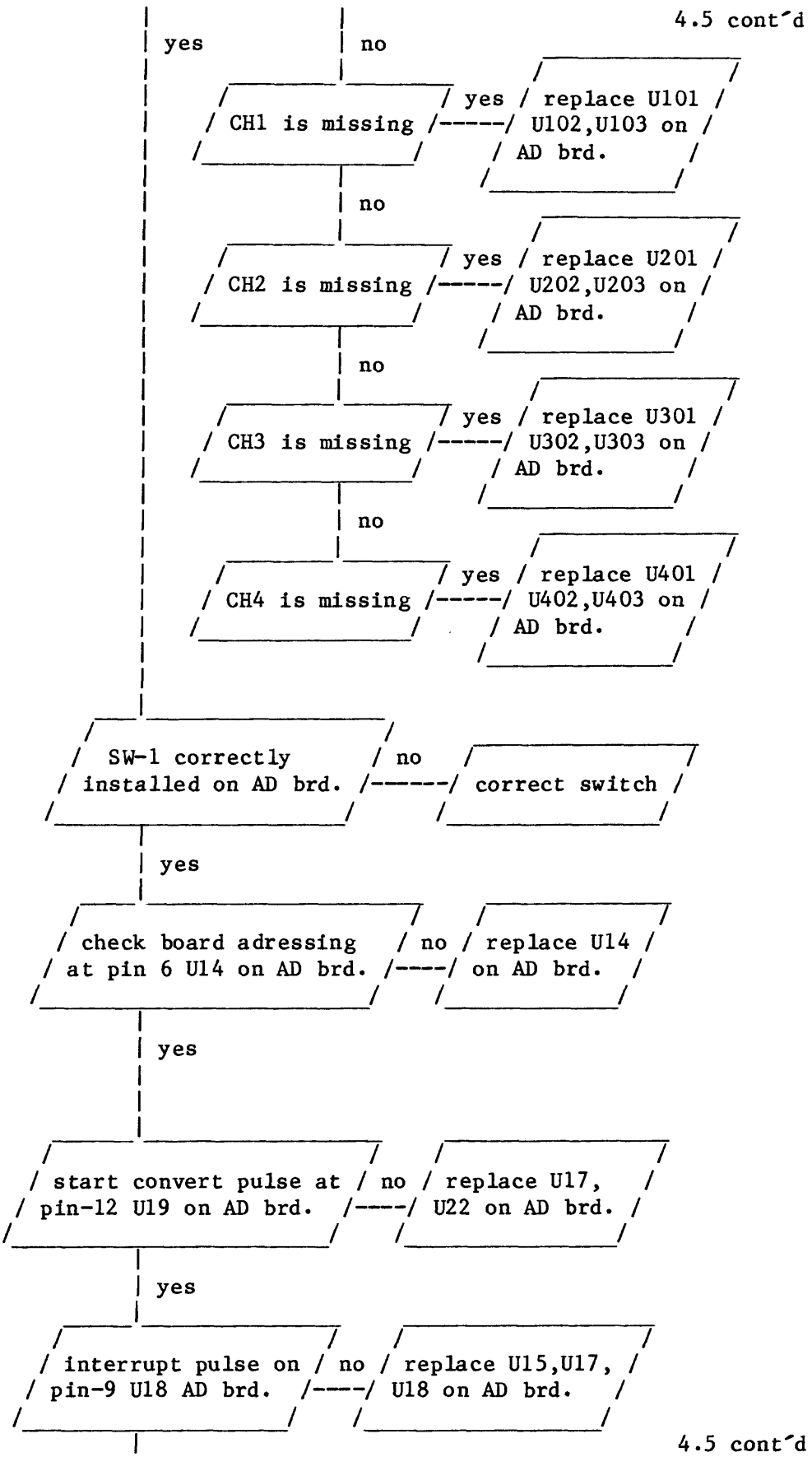


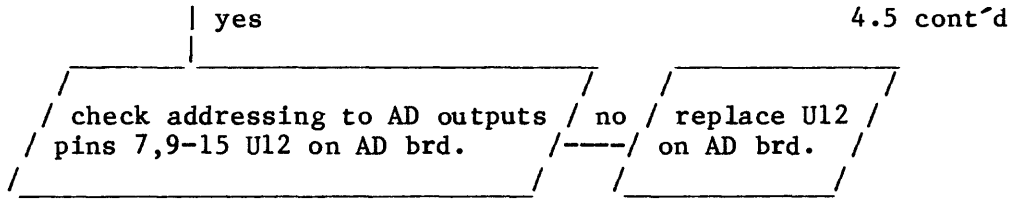

4.5 cont'd

4.5 cont'd




4.5 cont'd


yes
no
CH1 is missing
yes
replace U101 U102,U103 on AD brd.
no
CH2 is missing
yes
replace U201 U202,U203 on AD brd.
no
CH3 is missing
yes
replace U301 U302,U303 on AD brd.
no
CH4 is missing
yes
replace U401 U402,U403 on AD brd.
SW-1 correctly installed on AD brd.
no
correct switch
yes
check board adressing at pin 6 U14 on AD brd.
no
replace U14 on AD brd.
yes
start convert pulse at pin-12 U19 on AD brd.
no
replace U17, U22 on AD brd.
yes
interrupt pulse on pin-9 U18 AD brd.
no
replace U15,U17, U18 on AD brd.


yes
4.5 cont'd
check addressing to AD outputs pins 7,9-15 U12 on AD brd.
no
replace U12 on AD brd.

# 5. BUS LIST

The following pages list the bus connections made to the bus by each board. Although the listings may lead to the impression that that this is an S-100 bus, it is not. Careful attention must be made to the mother-board layout (section 5.1) in order to correctly trace connections. Slot #1 is the power interface board; slot #2 is the analog board; slot #3 is the preamplifier board; slot #4 is the analog-to-digital board, slot #6 is the controller board, and slot #7 is the cartridge controller board.

## 5.1 BUS CONNECTIONS FOR THE MOTHER-BOARD

| | BRD#1 PIN# | BRD#2 PIN# | BRD#3 PIN# | BRD#4 PIN# | BRD#5 PIN# | BRD#6 PIN# | BRD#7 PIN# | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 51 | 1 | 51 | 1 | 51 | 1 | +5v |
| | 2 | 2 | 2 | 2 | 2 | 2 | 2 | +12v |
| | 52 | 52 | 52 | 52 | 52 | 52 | 52 | -12v |
| | 3 | 3 | 3 | 3 | 3 | 3 | 3 | NU |
| | 53 | 53 | 53 | 53 | 53 | 53 | 53 | NU |
| | 4 | 4 | 4 | 4 | 4 | 4 | 4 | VIO |
| +5v | \| | 54 | 54 | 54 | 54 | 54 | 54 | -5v |
| CART. | 5 | 55 | 5 | 55 | 5 | 5 | 5 | *CHAanalog |
| | \| | | | | 55 | 55 | 55 | NU |
| | 6 | 56 | 6 | 56 | 6 | 6 | 6 | *CHBanalog |
| | | | | | 56 | 56 | 56 | NU |
| | 7 | 57 | 7 | 57 | 7 | 7 | 7 | *CHCanalog |
| +12v | \| | | | | 57 | 57 | 57 | NU |
| CART. | 8 | 58 | 8 | 58 | 8 | 8 | 8 | *CHDanalog |
| | | | | | 58 | 58 | 58 | NU |
| | 9 | 59 | 9 | 59 | 9 | 9 | 9 | *CHEanalog |
| -12v | \| | | | | 59 | 59 | 59 | NU |
| CART. | 10 | 60 | 10 | 60 | 10 | 10 | 10 | *CHFanalog |
| | | | | | 60 | 60 | 60 | NU |
| RCV | 11 | 61 | 11 | 61 | 11 | 11 | 11 | *CHGanalog |
| | | | | | 61 | 61 | 61 | NU |
| XMIT | 12 | 62 | 12 | 62 | 12 | 12 | 12 | *CHHanalog |
| | | | | | 62 | 62 | 62 | NU |
| CLK | 13 | 63 | 13 | 63 | 13 | 13 | 13 | *CHIanalog |
| | | | | | 63 | 63 | 63 | NU |
| RST | 14 | 64 | 14 | 64 | 14 | 14 | 14 | *CHJanalog |
| | | | | | 64 | 64 | 64 | NU |
| EXTST | 15 | 65 | 15 | 65 | 15 | 15 | 15 | *CHKanalog |
| | | | | | 65 | 65 | 65 | RST CART. |
| INT* | 16 | 66 | 16 | 66 | 16 | 16 | 16 | *CHLanalog |
| | | | | | 66 | 66 | 66 | NU |
| RST* | 17 | 67 | 17 | 67 | 17 | 17 | 17 | *CHManalog |
| | | | | | 67 | 67 | 67 | NU |
| | 18 | 18 | 18 | 18 | 18 | 18 | 18 | NU |
| | 68 | 68 | 68 | 68 | 68 | 68 | 68 | NU |
| | 19 | 19 | 19 | 19 | 19 | 19 | 19 | NU |
| | 69 | 69 | 69 | 69 | 69 | 69 | 69 | EXTST |
| | 20 | 20 | 20 | 20 | 20 | 20 | 20 | GND |
| | 70 | 70 | 70 | 70 | 70 | 70 | 70 | GND |
| | 21 | 21 | 21 | 21 | 21 | 21 | 21 | -5v |
| | 71 | 71 | 71 | 71 | 71 | 71 | 71 | NU |
| | 22 | 22 | 22 | 22 | 22 | 22 | 22 | NU |
| | 72 | 72 | 72 | 72 | 72 | 72 | 72 | RDY* |
| | 23 | 23 | 23 | 23 | 23 | 23 | 23 | NU |
| | 73 | 73 | 73 | 73 | 73 | 73 | 73 | INT* |
| | 24 | 24 | 24 | 24 | 24 | 24 | 24 | NU |
| | 74 | 74 | 74 | 74 | 74 | 74 | 74 | NU |
| | 25 | 25 | 25 | 25 | 25 | 25 | 25 | NU |
| | 75 | 75 | 75 | 75 | 75 | 75 | 75 | RESET* |

Continued on next page.

NU = Not used

5.1 Continued

| BRD#1 PIN# | BRD#2 PIN# | BRD#3 PIN# | BRD#4 PIN# | BRD#5 PIN# | BRD#6 PIN# | BRD#7 PIN# | |
|---|---|---|---|---|---|---|---|
| 26 | 26 | 26 | 26 | 26 | 26 | 26 | NU |
| 76 | 76 | 76 | 76 | 76 | 76 | 76 | NU |
| 27 | 27 | 27 | 27 | 27 | 27 | 27 | RCV |
| 77 | 77 | 77 | 77 | 77 | 77 | 77 | PWR* |
| 28 | 28 | 28 | 28 | 28 | 28 | 28 | XMIT |
| 78 | 78 | 78 | 78 | 78 | 78 | 78 | pDBIN |
| 29 | 29 | 29 | 29 | 29 | 29 | 29 | A5 |
| 79 | 79 | 79 | 79 | 79 | 79 | 79 | A0 |
| 30 | 30 | 30 | 30 | 30 | 30 | 30 | A4 |
| 80 | 80 | 80 | 80 | 80 | 80 | 80 | A1 |
| 31 | 31 | 31 | 31 | 31 | 31 | 31 | A3 |
| 81 | 81 | 81 | 81 | 81 | 81 | 81 | A2 |
| 32 | 32 | 32 | 32 | 32 | 32 | 32 | NU |
| 82 | 82 | 82 | 82 | 82 | 82 | 82 | A6 |
| 33 | 33 | 33 | 33 | 33 | 33 | 33 | NU |
| 83 | 83 | 83 | 83 | 83 | 83 | 83 | A7 |
| 34 | 34 | 34 | 34 | 34 | 34 | 34 | NU |
| 84 | 84 | 84 | 84 | 84 | 84 | 84 | NU |
| 35 | 35 | 35 | 35 | 35 | 35 | 35 | DO1 |
| 85 | 85 | 85 | 85 | 85 | 85 | 85 | NU |
| 36 | 36 | 36 | 36 | 36 | 36 | 36 | DO0 |
| 86 | 86 | 86 | 86 | 86 | 86 | 86 | NU |
| 37 | 37 | 37 | 37 | 37 | 37 | 37 | NU |
| 87 | 87 | 87 | 87 | 87 | 87 | 87 | NU |
| 38 | 38 | 38 | 38 | 38 | 38 | 38 | DO4 |
| 88 | 88 | 88 | 88 | 88 | 88 | 88 | DO2 |
| 39 | 39 | 39 | 39 | 39 | 39 | 39 | DO5 |
| 89 | 89 | 89 | 89 | 89 | 89 | 89 | DO3 |
| 40 | 40 | 40 | 40 | 40 | 40 | 40 | DO6 |
| 90 | 90 | 90 | 90 | 90 | 90 | 90 | DO7 |
| 41 | 41 | 41 | 41 | 41 | 41 | 41 | DI2 |
| 91 | 91 | 91 | 91 | 91 | 91 | 91 | DI4 |
| 42 | 42 | 42 | 42 | 42 | 42 | 42 | DI3 |
| 92 | 92 | 92 | 92 | 92 | 92 | 92 | DI5 |
| 43 | 43 | 43 | 43 | 43 | 43 | 43 | DI7 |
| 93 | 93 | 93 | 93 | 93 | 93 | 93 | DI6 |
| 44 | 44 | 44 | 44 | 44 | 44 | 44 | NU |
| 94 | 94 | 94 | 94 | 94 | 94 | 94 | DI1 |
| 45 | 45 | 45 | 45 | 45 | 45 | 45 | sOUT |
| 95 | 95 | 95 | 95 | 95 | 95 | 95 | DI0 |
| 46 | 46 | 46 | 46 | 46 | 46 | 46 | sINP |
| 96 | 96 | 96 | 96 | 96 | 96 | 96 | INTA |
| 47 | 47 | 47 | 47 | 47 | 47 | 47 | NU |
| 97 | 97 | 97 | 97 | 97 | 97 | 97 | NU |
| 48 | 48 | 48 | 48 | 48 | 48 | 48 | NU |
| 98 | 98 | 98 | 98 | 98 | 98 | 98 | NU |
| 49 | 49 | 49 | 49 | 49 | 49 | 49 | CLOCK |
| 99 | 99 | 99 | 99 | 99 | 99 | 99 | POC* |
| 50-100 | 50-100 | 50-100 | 50-100 | 50-100 | 50-100 | 50-100 | GND |

NU = Not used

## 5.2 BUS CONNECTIONS FOR THE POWER INTERFACE BOARD

| PIN# | FUNCTION | PIN# | FUNCTION |
|---|---|---|---|
| 1 | +5v | 51 | +5v |
| 2 | +12v | 52 | -12v |
| 3 | NC | 53 | NU |
| 4 | +5v CART | 54 | -5v |
| 5 | +5v CART | 55 | CH1 ANALOG |
| 6 | +5v CART | 56 | NU |
| 7 | +12v CART | 57 | NU |
| 8 | +12v CART | 58 | CH2 ANALOG |
| 9 | -12v CART | 59 | NU |
| 10 | -12v CART | 60 | NU |
| 11 | RCV RS232 | 61 | CH3 ANALOG |
| 12 | XMIT RS232 | 62 | NU |
| 13 | CLK LCD | 63 | NU |
| 14 | RST LCD | 64 | CH4 ANALOG |
| 15 | EXTST | 65 | NU |
| 16 | INT* TERM | 66 | NU |
| 17 | RESET* EXTRST | 67 | GND |
| 18 | NC | 68 | NC |
| 19 | NC | 69 | EXTST |
| 20 | GND | 70 | GND |
| 21 | -5v | 71 | NC |
| 22 | NC | 72 | NC |
| 23 | NC | 73 | INT* |
| 24 | NC | 74 | NC |
| 25 | NC | 75 | RESET* |
| 26 | NC | 76 | NC |
| 27 | RCV RS232 | 77 | PWR* |
| 28 | XMIT RS232 | 78 | NC |
| 29 | A5 | 79 | A0 |
| 30 | A4 | 80 | A1 |
| 31 | A3 | 81 | A2 |
| 32 | NC | 82 | A6 |
| 33 | NC | 83 | A7 |
| 34 | NC | 84 | NC |
| 35 | DO1 | 85 | NC |
| 36 | DO0 | 86 | NC |
| 37 | NC | 87 | NC |
| 38 | NC | 88 | NC |
| 39 | NC | 89 | NC |
| 40 | NC | 90 | DO7 |
| 41 | NC | 91 | NC |
| 42 | NC | 92 | NC |
| 43 | NC | 93 | NC |
| 44 | NC | 94 | NC |
| 45 | sOUT | 95 | NC |
| 46 | NC | 96 | NC |
| 47 | NC | 97 | NC |
| 48 | NC | 98 | NC |
| 49 | CLOCK | 99 | NC |
| 50 | GND | 100 | GND |

NC= not connected NU= not used

## 5.3 BUS CONNECTIONS FOR ANALOG BOARD

| PIN# | FUNCTION | PIN# | FUNCTION |
|---|---|---|---|
| 1 | +5v | 51 | +5v |
| 2 | NC | 52 | NC |
| 3 | NC | 53 | NC |
| 4 | NC | 54 | -5v |
| 5 | NU | 55 | CH1 out ANALOG |
| 6 | NU | 56 | NU |
| 7 | NU | 57 | NU |
| 8 | NU | 58 | CH2 out ANALOG |
| 9 | NU | 59 | NU |
| 10 | NU | 60 | NU |
| 11 | NU | 61 | CH3 out ANALOG |
| 12 | NU | 62 | NU |
| 13 | NU | 63 | NU |
| 14 | NU | 64 | CH4 out ANALOG |
| 15 | NU | 65 | NU |
| 16 | NU | 66 | NU |
| 17 | GND | 67 | GND |
| 18 | NC | 68 | NC |
| 19 | NC | 69 | NC |
| 20 | NC | 70 | NC |
| 21 | -5v | 71 | NC |
| 22 | NC | 72 | NC |
| 23 | NC | 73 | INT* |
| 24 | NC | 74 | NC |
| 25 | NC | 75 | NC |
| 26 | NC | 76 | NC |
| 27 | NC | 77 | PWR* |
| 28 | NC | 78 | pDBIN |
| 29 | A5 | 79 | A0 |
| 30 | A4 | 80 | NC |
| 31 | A3 | 81 | NC |
| 32 | NC | 82 | A6 |
| 33 | NC | 83 | A7 |
| 34 | NC | 84 | NC |
| 35 | DO1 | 85 | NC |
| 36 | DO0 | 86 | NC |
| 37 | NC | 87 | NC |
| 38 | DO4 | 88 | DO2 |
| 39 | DO5 | 89 | DO3 |
| 40 | DO6 | 90 | DO7 |
| 41 | DI2 | 91 | DI4 |
| 42 | DI3 | 92 | DI5 |
| 43 | DI7 | 93 | DI6 |
| 44 | NC | 94 | DI1 |
| 45 | sOUT | 95 | DI0 |
| 46 | sINP | 96 | NC |
| 47 | NC | 97 | NC |
| 48 | NC | 98 | NC |
| 49 | CLOCK | 99 | POC* |
| 50 | GND | 100 | GND |

NC= not connected NU= not used

## 5.4 BUS CONNECTIONS FOR THE PREAMPLIFIER BOARD

| PIN# | FUNCTION | PIN# | FUNCTION |
|---|---|---|---|
| 1 | +5v | 51 | +5v |
| 2 | NC | 52 | NC |
| 3 | NC | 53 | NC |
| 4 | NC | 54 | -5v |
| 5 | CH1 in ANALOG | 55 | NC |
| 6 | NC | 56 | CH1 out ANALOG |
| 7 | NC | 57 | NC |
| 8 | CH2 in ANALOG | 58 | NC |
| 9 | NC | 59 | CH2 out ANALOG |
| 10 | NC | 60 | NC |
| 11 | CH3 in ANALOG | 61 | NC |
| 12 | NC | 62 | CH3 out ANALOG |
| 13 | NC | 63 | NC |
| 14 | CH4 in ANALOG | 64 | NC |
| 15 | NC | 65 | CH4 out ANALOG |
| 16 | NC | 66 | NC |
| 17 | NC | 67 | NC |
| 18 | NC | 68 | NC |
| 19 | NC | 69 | NC |
| 20 | NC | 70 | NC |
| 21 | NC | 71 | NC |
| 22 | NC | 72 | NC |
| 23 | NC | 73 | NC |
| 24 | NC | 74 | NC |
| 25 | NC | 75 | NC |
| 26 | NC | 76 | NC |
| 27 | NC | 77 | NC |
| 28 | NC | 78 | NC |
| 29 | NC | 79 | NC |
| 30 | NC | 80 | NC |
| 31 | NC | 81 | NC |
| 32 | NC | 82 | NC |
| 33 | NC | 83 | NC |
| 34 | NC | 84 | NC |
| 35 | NC | 85 | NC |
| 36 | NC | 86 | NC |
| 37 | NC | 87 | NC |
| 38 | NC | 88 | NC |
| 39 | NC | 89 | NC |
| 40 | NC | 90 | NC |
| 41 | NC | 91 | NC |
| 42 | NC | 92 | NC |
| 43 | NC | 93 | NC |
| 44 | NC | 94 | NC |
| 45 | NC | 95 | NC |
| 46 | NC | 96 | NC |
| 47 | NC | 97 | NC |
| 48 | NC | 98 | NC |
| 49 | NC | 99 | NC |
| 50 | GND | 100 | GND |

NC= not connected NU= not used

## 5.5 BUS CONNECTIONS FOR THE ANALOG-TO DIGITAL BOARD

| PIN# | FUNCTION | PIN# | FUNCTION |
|---|---|---|---|
| 1 | +5v | 51 | +5v |
| 2 | NC | 52 | NC |
| 3 | NC | 53 | NC |
| 4 | VIO* | 54 | -5v |
| 5 | NU | 55 | NU |
| 6 | CH1 in ANALOG | 56 | CH1 in ANALOG |
| 7 | NU | 57 | NU |
| 8 | NU | 58 | NU |
| 9 | CH2 in ANALOG | 59 | CH2 in ANALOG |
| 10 | NU | 60 | NU |
| 11 | NU | 61 | NU |
| 12 | CH3 in ANALOG | 62 | CH3 in ANALOG |
| 13 | NU | 63 | NU |
| 14 | NU | 64 | NU |
| 15 | CH4 in ANALOG | 65 | CH4 in ANALOG |
| 16 | NU | 66 | NU |
| 17 | GND | 67 | GND |
| 18 | NC | 68 | NC |
| 19 | NC | 69 | NC |
| 20 | NC | 70 | NC |
| 21 | NC | 71 | NC |
| 22 | NC | 72 | NC |
| 23 | NC | 73 | INT* |
| 24 | NC | 74 | NC |
| 25 | NC | 75 | NC |
| 26 | NC | 76 | NC |
| 27 | NC | 77 | PWR* |
| 28 | NC | 78 | pDBIN |
| 29 | A5 | 79 | A0 |
| 30 | A4 | 80 | NC |
| 31 | A3 | 81 | NC |
| 32 | NC | 82 | A6 |
| 33 | NC | 83 | A7 |
| 34 | NC | 84 | NC |
| 35 | DO1 | 85 | NC |
| 36 | DO0 | 86 | NC |
| 37 | NC | 87 | NC |
| 38 | DO4 | 88 | DO2 |
| 39 | DO5 | 89 | DO3 |
| 40 | DO6 | 90 | DO7 |
| 41 | DI2 | 91 | DI4 |
| 42 | DI3 | 92 | DI5 |
| 43 | DI7 | 93 | DI6 |
| 44 | NC | 94 | DI1 |
| 45 | sOUT | 95 | DI0 |
| 46 | sINP | 96 | NC |
| 47 | NC | 97 | NC |
| 48 | NC | 98 | NC |
| 49 | CLOCK | 99 | NC |
| 50 | GND | 100 | GND |

NC= not connected NU= not used

## 5.6 BUS CONNECTIONS FOR THE CONTROLLER BOARD

| PIN# | FUNCTION | PIN# | FUNCTION |
|---|---|---|---|
| 1 | +5v | 51 | +5v |
| 2 | +12v | 52 | NC |
| 3 | NC | 53 | NC |
| 4 | VIO* | 54 | -5v |
| 5 | NC | 55 | NC |
| 6 | NC | 56 | NC |
| 7 | NC | 57 | NC |
| 8 | NC | 58 | NC |
| 9 | NC | 59 | NC |
| 10 | NC | 60 | NC |
| 11 | NC | 61 | NC |
| 12 | NC | 62 | NC |
| 13 | NC | 63 | NC |
| 14 | NC | 64 | NC |
| 15 | NC | 65 | RST CART |
| 16 | NC | 66 | NC |
| 17 | NC | 67 | NC |
| 18 | NC | 68 | NC |
| 19 | NC | 69 | EXTST |
| 20 | GND | 70 | GND |
| 21 | -5v | 71 | NC |
| 22 | NC | 72 | RDY |
| 23 | NC | 73 | INT* |
| 24 | NC | 74 | NC |
| 25 | NC | 75 | RESET* |
| 26 | NC | 76 | NC |
| 27 | RCV RS232 | 77 | PWR* |
| 28 | XMIT RS232 | 78 | pDBIN |
| 29 | A5 | 79 | A0 |
| 30 | A4 | 80 | A1 |
| 31 | A3 | 81 | A2 |
| 32 | NC | 82 | A6 |
| 33 | NC | 83 | A7 |
| 34 | NC | 84 | NC |
| 35 | DO1 | 85 | NC |
| 36 | DO0 | 86 | NC |
| 37 | NC | 87 | NC |
| 38 | DO4 | 88 | DO2 |
| 39 | DO5 | 89 | DO3 |
| 40 | DO6 | 90 | DO7 |
| 41 | DI2 | 91 | DI4 |
| 42 | DI3 | 92 | DI5 |
| 43 | DI7 | 93 | DI6 |
| 44 | NC | 94 | DI1 |
| 45 | sOUT | 95 | DI0 |
| 46 | sINP | 96 | INTA |
| 47 | NC | 97 | NC |
| 48 | NC | 98 | NC |
| 49 | CLOCK | 99 | POC* |
| 50 | GND | 100 | GND |

NC= not connected NU= not used

## 5.7 BUS CONNECTIONS FOR THE CARTRIDGE CONTROLLER BOARD

| PIN# | FUNCTION | PIN# | FUNCTION |
|---|---|---|---|
| 1 | +5v | 51 | +5v |
| 2 | NC | 52 | NC |
| 3 | NC | 53 | NC |
| 4 | NC | 54 | NC |
| 5 | NC | 55 | NC |
| 6 | NC | 56 | NC |
| 7 | NC | 57 | NC |
| 8 | NC | 58 | NC |
| 9 | NC | 59 | NC |
| 10 | NC | 60 | NC |
| 11 | NC | 61 | NC |
| 12 | NC | 62 | NC |
| 13 | NC | 63 | NC |
| 14 | NC | 64 | NC |
| 15 | NC | 65 | RST CART |
| 16 | NC | 66 | NC |
| 17 | NC | 67 | NC |
| 18 | NC | 68 | NC |
| 19 | NC | 69 | NC |
| 20 | NC | 70 | NC |
| 21 | NC | 71 | NC |
| 22 | NC | 72 | NC |
| 23 | NC | 73 | NC |
| 24 | NC | 74 | NC |
| 25 | NC | 75 | RESET* |
| 26 | NC | 76 | NC |
| 27 | NC | 77 | PWR* |
| 28 | NC | 78 | pDBIN |
| 29 | A5 | 79 | A0 |
| 30 | A4 | 80 | A1 |
| 31 | A3 | 81 | A2 |
| 32 | NC | 82 | A6 |
| 33 | NC | 83 | A7 |
| 34 | NC | 84 | NC |
| 35 | DO1 | 85 | NC |
| 36 | DO0 | 86 | NC |
| 37 | NC | 87 | NC |
| 38 | DO4 | 88 | DO2 |
| 39 | DO5 | 89 | DO3 |
| 40 | DO6 | 90 | DO7 |
| 41 | DI2 | 91 | DI4 |
| 42 | DI3 | 92 | DI5 |
| 43 | DI7 | 93 | DI6 |
| 44 | NC | 94 | DI1 |
| 45 | sOUT | 95 | DI0 |
| 46 | sINP | 96 | NC |
| 47 | NC | 97 | NC |
| 48 | NC | 98 | NC |
| 49 | NC | 99 | NC |
| 50 | GND | 100 | GND |

NC= not connected NU= not used

# 6. PARTS LIST

## 6.1 POWER INTERFACE BOARD

| value/part# | board # | qty. | notes |
|---|---|---|---|
| **Capacitors** | | | |
| 0.1uf,50v,ceramic | C7 | 1 | Centralab CY20C104M |
| 0.22uf,50v,ceramic | C8,C9 | 2 | Centralab CY20C224M |
| 2.2uf,50v,ceramic | C3,C4 | 2 | Centralab CY30C225M |
| 10.0uf,20v,tantalum | C1,C2,C6 | 3 | Sprague CSR13E106KL |
| 100.0uf,20v,tantalum | C5 | 1 | Sprague CSR13E107KL |
| **Resistors** | | | |
| 274 ohm* | R3 | 1 | 1/4 watt, 1% |
| 1.00k ohm | R4 | 1 | " " " |
| 3.32k ohm | R1,R2 | 2 | " " " |
| 4.72k ohm | R5,R6 | 2 | " " " |
| **Semiconductors** | | | |
| LT1038Ksteel, 12v adj. reg. | Q1 | 1 | Linear Tech |
| UA78M05,+5v reg. | Q2 | 1 | Fairchild |
| UA79M05,-5v reg. | Q3 | 1 | Fairchild |
| 2N2222 | Q4,Q5 | 2 | Motorola |
| 1N4001,50v,1a | CR1-CR12 | 11 | Motorola |
| 74C10, 3-input nand gate | U1 | 1 | National Semiconductor |
| 74C30, 8-input nand gate | U2 | 1 | National Semiconductor |
| CD4724, 8-bit latch | U3 | 1 | National Semiconductor |
| **Fuses** | | | |
| 2A Micro | F1,F3-F5 | 5 | Littlefuse |
| 3A Micro | F2 | 1 | Littlefuse |
| **Relay** | | | |
| S4E-12V | K1,K2 | 2 | Aromat |

| value/part# | board # | qty. | notes |
|---|---|---|---|
| **Oscillator** | | | |
| 251-5907, 2.097152Mhz | Y1 | 1 | Vectron |
| **Switches** | | | |
| TP11, MOM,SPST | SW1 | 1 | C&K |
| T203HMCBE, DPDT | SW2 | 1 | C&K |
| **Hardware** | | | |
| 8 pin, rt. angle,PC | P1 | 1 | Molex 2391 series |
| 26pin conn., rt. angle header | P2 | 1 | Berg 65823-073 |
| 26 pin .01c, header | P3 | 1 | AMP 1-87543-3 |
| 13 pin .01, header | P4 | 1 | AMP 1-87348-3 |
| 14 pin IC socket | | 2 | Augat 314-AG40D |
| 16 pin IC socket | | 1 | Augat 316-AG40D |
| Front mount MTD jack(coax) | | 4 | Selectro 50-045-0000 |
| Battery holder | | 2 | Keystone 856 |
| Fuse holder | | 5 | Littlefuse 281-007 |
| Heat sink | | 1 | Ahamtor 401-T03 |
| Battery | | 2 | GE GC9B |
| 6-32x1/2" Binder hd | | 2 | screw |
| 4-40x3/8" Binder hd | | 6 | screw |
| #6 lock | | 2 | washer |
| 6-32 hex | | 2 | nut |
| 4-40 hex | | 6 | nut |

* R3 adjusted for output of Q1 = 5.2volts under load.

## 6.2 ANALOG BOARD

| value/part# | board # | qty. | notes |
|---|---|---|---|
| **Capacitors** | | | |
| 0.00627 uf,1%, polycarb. | C8,C17, C26,C35 | 4 | Elpac C5B6271F |
| 0.0178 uf,1%, polycarb. | C6,C15, C24,C33 | 4 | Elpac C5B1782F |
| 0.0267 uf,1%, polycarb. | C4,C13, C22,C31 | 4 | Elpac C5B2672F |
| 0.0315 uf,1%, polycarb. | C2,C11, C20,C29 | 4 | Elpac C5B3152F |
| 0.0328 uf,1%, polycarb. | C1,C10, C19,C28 | 4 | Elpac C5B3282F |
| 0.0387 uf,1%, polycarb. | C3,C12, C21,C30 | 4 | Elpac C5B3872F |
| 0.0581 uf,1%, polycarb. | C5,C14, C23,C32 | 4 | Elpac C5B5812F |
| 0.1690 uf,1%, polycarb. | C7,C16, C25,C34 | 4 | Elpac C5B1693F |
| 470 pf,50v,ceramic | C54,C56 | 2 | Centralab CW15C471K |
| 0.0015 uf,50v,ceramic | C53 | 1 | Centralab CW30C153K |
| 0.0047 uf,50v,ceramic | C52 | 1 | Centralab CW20C472K |
| 0.018 uf,50v,ceramic | C51 | 1 | Centralab CW20C183K |
| 0.1 uf,50v,ceramic | C65 | 1 | Centralab CW30C104M |
| 0.22 uf,50v,ceramic | C66-C90 | 25 | Centralab CY20C224M |
| 0.33 uf,50v,ceramic | C64 | 1 | Centralab CY20C334M |
| 0.68 uf,50v,ceramic | C63 | 1 | Centralab CY20C684M |
| 1.5 uf,50v,ceramic | C62 | 1 | Centralab CY30C155M |
| 2.2 uf,50v,ceramic | C9,C18, C27,C50, C55,C57 | 6 | Centralab CY30C225M |
| 3.3 uf,50v,ceramic | C61 | 1 | Centralab CY30C335M |
| 39.0 uf,10v, tantalum | C60 | 1 | Sprague CSR13E396KL |
| 100 uf,10v, tantalum | C58,C59, C92,C93 | 4 | Sprague CSR13E107KL |

| value/part# | board # | qty. | notes |
|---|---|---|---|
| **Resistors** | | | |
| 1.00K, 1/4 watt, 1% | R1,R12, R23,R34, R85 | 5 | |
| 4.70K, 1/4 watt, 1% | R108 | 1 | |
| 5.11K, 1/4 watt, 1% | R87 | 1 | |
| 10.0K, 1/4 watt, 1% | R84 | 1 | |
| 22.1K, 1/4 watt, 1% | R83 | 1 | |
| 33.2K, 1/4 watt, 1% | R64 | 1 | |
| 47.5K, 1/4 watt, 1% | R70,R72, R75 | 3 | |
| 56.2K, 1/4 watt, 1% | R81,R94 | 2 | |
| 82.5K, 1/4 watt, 1% | R77,R80, R90,R93, R96 | 5 | |
| 100.0K, 1/4 watt, 1% | R62,R63, R65-R67, R74,R86, R104,R105, R109-R112 | 13 | |
| 165k, 1/ watt, 5% | R76,R78, R79,R82, R89,R91, R92,R95 | 8 | |
| 200k, 1/4 watt, 5% | R107 | 1 | |
| 2m, 1/4 watt, 5% | R71,R73 | 2 | |
| 6.8m, 1/4 watt, 5% | R88 | 1 | |
| on header CM-8: | | | |
| 5.49k, 1/4 watt, 1% | R102 | 1 | |
| 11.3k, 1/4 watt, 1% | R101 | 1 | |
| 26.7k, 1/4 watt, 1% | R100 | 1 | |
| 100K sip network | RP1 | 1 | Bourne 10-1-104 |
| XXK dip network | CM1-CM4 | 4 | Bourne 16-1-XX4 value determined by freq. cutoff |

| value/part# | board # | qty. | notes |
|---|---|---|---|
| **Semiconductors** | | | |
| 2N2222 | Q1 | 1 | Motorola |
| 1N914 | D3-D6 | 4 | Motorola |
| AD7110, audio attenuator | U22 | 1 | Analog Devices |
| OP421HY, quad op-amp | U1-U4, U6,U7, U13,U15, U19 | 7 | PMI |
| L161CJ, comparator | U12 | 1 | Siliconix |
| 74C04N, hex inverter | U9 | 1 | National Semiconductor |
| 74C10, 3input AND gate | U8 | 1 | National Semiconductor |
| 74C32, 2input OR gate | U10 | 1 | National Semiconductor |
| 74C74, dual D flip/flop | U24 | 1 | National Semiconductor |
| 74C244, octal buffer | U20 | 1 | National Semiconductor |
| 74C374,octal D flip/flop | U14 | 1 | National Semiconductor |
| 4012B, 4input NAND gate | U27 | 1 | National Semiconductor |
| 4029B, U/D binary cntr. | U21,U25 | 1 | National Semiconductor |
| 4063B, 4bit comparator | U11 | 1 | Toshiba |
| 4066B, quad switch | U16,U17, U18 | 3 | National Semiconductor |
| 4071B, quad NOR gate | U23 | 1 | National Semiconductor |
| 4521B, 24stage bin. cntr | U26 | 1 | RCA |
| **Switches** | | | |
| SPST momentary | SW1 | 1 | C&K # TP11 |
| 4-Position Dip | SW2 | 1 | Grayhill #76RSB04S |
| 8-Position Dip | SW3 | 1 | Grayhill #76RSB08S |
| **Hardware** | | | |
| 2x13 .1", header, PC | J6,J7 | 2 | Amp 1-87543-3 |
| 2x3 .1", header, PC | J3,J5 | 2 | Amp |
| 1x3 .1", header, PC | J4,J8 | 2 | Amp |
| 3 pin rt. ang. header | J9 | 1 | Amp |
| 5 pin rt.ang. header | J1,J2 | 2 | Amp |
| **Sockets** | | | |
| 8 pin IC socket | | 1 | Augat 308-AG40D |
| 14 pin IC socket | | 19 | Augat 314-AG40D |
| 16 pin IC socket | | 16 | Augat 316-AG40D |
| 20 pin IC socket | | 2 | Augat 320-AG40D |

## 6.3 PREAMPLIFIER BOARD

| value/part# | board # | qty. | notes |
|---|---|---|---|
| **Capacitors** | | | |
| 0.047uf,35v,tantalum | C2-C9 | 8 | Sprague 150D473X9035A |
| 10.0uf,20v,tantalum | C1,C10 | 2 | Sprague CSR13E106KL |
| **Resistors** | | | |
| 124 ohm | R5,R10, R15,R17 | 4 | 1/4 watt, 1% |
| 272 ohm | R4,R9, R14, | 3 | " " " |
| 332 ohm | R20 | 1 | " " " |
| 825 ohm | R2,R7, R12 | 3 | " " " |
| 5.49k ohm | R3,R8 R13 | 3 | " " " |
| 67.5k ohm | R16 | 1 | " " " |
| 100k ohm | R18 | 1 | " " " |
| 331k ohm | R1,R6, R11 | 3 | " " " |
| 1.00 megohm | R19 | 1 | " " " |
| 150K dip network | RM1 | 1 | Bourne 16-1-154 |
| **Semiconductors** | | | |
| AMP 01 | U1-U4 | 4 | PMI |
| OP421HY | U5 | 1 | PMI |
| **Hardware** | | | |
| 5 pin conn., rt. angle header | P1 | 1 | AMP |
| 14 pin IC socket | | 2 | CA CA-14SPV-103WW |
| 16 pin IC socket | | 1 | CA CA-16SPV-103WW |
| 18 pin IC socket | | 4 | CA CA-18SPV-103WW |
| Front mount MTD jack(coax) | J2-J5 | 4 | Selectro 50-045-0000 |

## 6.4 ANALOG-TO-DIGITAL BOARD

| value/part# | board # | qty. | notes |
|---|---|---|---|
| **Capacitors** | | | |
| 100 pf,100v,ceramic | C1,C4, C20,C33 | 4 | Centralab CN15A101K |
| 0.001uf,100v,ceramic | C29 | 1 | Centralab CN20A102K |
| 0.22 uf,50v,ceramic | C3, C5-C15, C19, C21-C28, C30,C32, C34-C44, C46-C55, C60-C62 | 44 | Centralab CY20C224M |
| 2.2 uf,50v,ceramic | C2,C18, C31,C45 | 4 | Centralab CY30C225M |
| 0.01 uf,1% polycarb. | C56-C59 | 4 | Elpac PD5A103K |
| 100.0 uf,10v,tantalum | C16,C17 | 2 | Sprague CSR13E107KL |
| **Resistors** | | | |
| 332, 1/4 watt, 1% | R18,R19 | 2 | |
| 1.00k, 1/4 watt, 5% | R101,R201, R301, R401 | 4 | |
| 3.32k, 1/4 watt, 1% | R17,R20 | 2 | |
| 4.42k, 1/4 watt, 1% | R16,R21 | 2 | |
| 10.0k, 1/4 watt, 5% | R11,R104, R204,R304, R404 | 5 | |
| 20.0k, 1/4 watt, 1% | R103,R203, R303, R403 | 4 | |
| 100k, 1/4 watt, 1% | R12-R15, R22,R23, R105-R108, R205-R208, R305-R308, R405-R408 | 22 | |
| 200k, 1/4 watt, 1% | R102,R202, R302,R402, R109,R209, R309, R409 | 8 | |

| value/part# | board # | qty. | notes |
|---|---|---|---|
| **Semiconductors** | | | |
| 2N2907 | Q1 | 1 | Motorola |
| 1N914 | D1 | 1 | Motorola |
| OP21EP,Op-amp | U104,U105, U204,U205, U304,U305, U404, U405 | 8 | Precision Monolithics |
| ADC1210HCD, A-D convert | U101,U201, U301, U401 | 4 | National Semiconductor |
| 7541KN, 12bit D-A | U106,U206, U306 U406 | 4 | Datel |
| L161CJ, comparator | U111,U211, U311, U411 | 4 | Siliconix |
| CD4016BE, analog switch | U20 | 1 | RCA |
| CD4017BE, counter | U17 | 1 | RCA |
| CD4028B,lof10 decode | U107,U207, U307 U407 | 4 | Fairchild |
| CD4029, counter | U108,U208, U308 U408 | 4 | Fairchild |
| CD4040, counter | U22 | 1 | Fairchild |
| CD4043, latch | U18 | 1 | Toshiba |
| CD4063, 4-bit compare | U14 | 1 | Toshiba |
| CD4536, timer | U15 | 1 | RCA |
| 74C00, NAND gate | U110,U210, U320, U410 | 4 | National Semiconductor |
| 74C04, hex inverter | U19 | 1 | National Semiconductor |
| 74C08, AND gate | U21,U109, U209,U309, U409 | 5 | National Semiconductor |
| 74C10, NAND gate | U16 | 1 | National Semiconductor |
| 74C138, lof8 decode | U12 | 1 | National Semiconductor |
| 74C374, latch | U13,U102, U103,U202, U203,U302, U303,U402, U403 | 9 | Motorola |
| **Switches** | | | |
| 4-Position Dip | SW1 | 1 | Grayhill 76RSB04S |

| value/part# | board # | qty. | notes |
|---|---|---|---|
| **Connectors** | | | |
| 2x13 .1", header,pc | J1 | 1 | Amp 1-87543-3 |
| 5pin rt. ang. header | J2,J3 | 2 | Amp |
| **Sockets** | | | |
| 8 pin | | 9 | Augat 308-AG40D |
| 14 pin | | 13 | Augat 314-AG40D |
| 16 pin | | 18 | Augat 316-AG40D |
| 18 pin | | 4 | Augat 318-AG40D |
| 20 pin | | 9 | Augat 320-AG40D |
| 24 pin | | 4 | Augat 324-AG40D |

## 6.5 CONTROLLER BOARD

| value/part# | board # | qty. | notes |
|---|---|---|---|
| **Capacitors** | | | |
| 0.22 uf,50v,ceramic | C4-C31 | 28 | Centralab CY20C224M |
| 39.0 uf,10v,tantalum | C1 | 1 | Sprague CSR13E396KL |
| 100.0 uf,10v,tantalum | C2,C3 | 2 | Sprague CSR13E107KL |
| **Resistors** | | | |
| 1.00k, 1/4 watt, 5% | R5 | 1 | |
| 10.0k, 1/4 watt, 5% | R1,R6,R7, R12,R13 | 5 | |
| 27.4k, 1/4 watt, 5% | R8,R9 | 2 | |
| 50.0k, 1/4 watt, 5% | R10 | 1 | |
| 68.1k, 1/4 watt, 1% | R11 | 1 | |
| 100k network | RP1 | 1 | Bournes 10-1-104 |
| **Semiconductors** | | | |
| 1N914 | D1-D4 | 4 | GE |
| 74C00, NAND gate | U20 | 1 | National Semiconductor |
| 74C02, NOR gate | U12 | 1 | National Semiconductor |
| 74C08, AND gate | U13 | 1 | National Semiconductor |
| 74C30, NAND gate | U28 | 1 | National Semiconductor |
| 74C32, OR gate | U22,U27 | 2 | National Semiconductor |
| 74C74*, flip/flop | U26 | 1 | National Semiconductor |
| 74C86*, XOR gate | U25 | 1 | National Semiconductor |
| 74C138, 1of8 decode | U23,U24 | 2 | National Semiconductor |
| 74C240, octal buffer | U21 | 1 | National Semiconductor |
| 74C244, octal buffer | U18,U19 | 2 | National Semiconductor |
| 74HC373, latch | U17 | 1 | National Semiconductor |
| 58167A, RTC | U10 | 1 | National Semiconductor |
| NSC800N, CPU | U7 | 1 | National Semiconductor |
| NSC810AN,I/O ram timer | U8 | 1 | National Semiconductor |
| CD4040, counter | U14 | 1 | Fairchild |
| HM5-6564, ram | U2-U6 | 5 | Harris |
| MBM27C64-30,EPROM | U16 | 1 | Fujitsu |
| OP220HZ, op-amp | U15 | 1 | PMI |

* not needed for some Software. Use 14 pin dip header with pins 2&3, 5&6 tied together in place of U25.

| value/part# | board # | qty. | notes |
|---|---|---|---|
| **Sockets** | | | |
| 8 pin | | 1 | Augat 308-AG40D |
| 14 pin | | 8 | Augat 314-AG40D |
| 16 pin | | 4 | Augat 316-AG40D |
| 20 pin | | 4 | Augat 320-AG40D |
| 28 pin | | 1 | Augat 328-AG40D |
| 40 pin | | 2 | Augat 340-AG40D |
| 20 pin sip | | 10 | Augat |

## 6.6 CARTRIDGE CONTROLLER BOARD

| value/part# | board # | qty. | notes |
|---|---|---|---|
| **Capacitors** | | | |
| 100.0 pf,100v,mica | C20,C21, C23 | 3 | CT1000PF |
| 0.10 uf,100v,ceramic | C4-C19, C22 | 17 | CF.1@100 |
| 47.0 uf,16v,electrolytic | C1-C3 | 3 | Maram CFTE-113 |
| **Resistors** | | | |
| 100, 1/4 watt, 5% | R4,R5 | 2 | |
| 2.0k, 1/4 watt, 5% | R1-R3 | 3 | |
| 2.0k network | M1,M24 | 2 | Bournes 10-1-202 |
| 220/330 network | M3,M8 | 2 | Beckman 785-5-R220/330 |
| **Crystal** | | | |
| QC6.144MHZ | CL1 | 1 | |
| **Semiconductors** | | | |
| 74LS04, hex inverter | M34 | 1 | Texas Instruments |
| 7406, hex inverter | M10 | 1 | Fairchild |
| 74LS10, NAND gate | M21,M22 | 2 | Fairchild |
| 74LS11, AND gate | M20,M35, M36 | 3 | Fairchild |
| 74LS74, flip/flop | M15,M23, M31 | 3 | Texas Instruments |
| 74LS138, lof8 decode | M18,M19 | 2 | Texas Instruments |
| 74LS155, dual 2/4 decode | M26 | 1 | Fairchild |
| 74LS240, octal inverter | M4,M9 | 2 | Texas Instruments |
| 74LS244, octal buffer | M11-M13 | 3 | Texas Instruments |
| 74LS287, CODEC rom | M25 | 1 | Signetics |
| 74LS368, hex buffer | M30 | 1 | Texas Instruments |
| 74LS373, latch | M2 | 1 | Texas Instruments |
| 74LS374, octal flip-flop | M5,M6, M32,M33 | 4 | Texas Instruments |
| 2114-2, ram 1Kx4 | M16,M17 | 2 | NEC |
| 2651, prog. interface | M7 | 1 | Signetics |
| 2716, EPROM 2Kx8 | M29 | 1 | Hatachi |
| 6132-6WB, ram 4Kx8 | M27,M28 | 2 | Ziglog |
| 8085, CPU | M14 | 1 | NEC |

| value/part# | board # | qty. | notes |
|---|---|---|---|
| **Sockets** | | | |
| 14 pin | | 10 | Augat 314-AG40D |
| 16 pin | | 8 | Augat 316-AG40D |
| 18 pin | | 2 | Augat 318-AG40D |
| 20 pin | | 10 | Augat 320-AG40D |
| 24 pin | | 1 | Augat 324-AG40D |
| 28 pin | | 2 | Augat 328-AG40D |
| 40 pin | | 1 | Augat 340-AG40D |
| **Switches** | | | |
| 4-Position Dip | SW1 | 1 | Grayhill 76RSB04S |
| **Connectors** | | | |
| 40 pin header | P2 | 1 | |
| 50 pin header | P1 | 1 | |
| 2x3 pin header | | 1 | |

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# APPENDIX I

## Electrical Specifications

| | |
|---|---|
| Data channels | 1 to 4 |
| Time channels | 1 |
| Dynamic range | |
| Main converter | 72dB (12bits) |
| Gain ranging | 60dB (10bits) |
| Total | 132dB |
| analog-to-digital noise | 150 millivolts |
| Total useful | 90dB (15bits) |
| Gain range rate | |
| Type | floating |
| Increment | 6dB/step |
| Rate | 7 microseconds |
| Sample rate | 1, 2, 4, 8 milliseconds software selectable |
| Filters | |
| Type | butterworth |
| Frequency | 30, 60, 125, 250, 500 Hz |
| Roll off | 48dB/octave |
| Memory | |
| Main | 8 kilobytes |
| Buffer | 32 kilobytes |
| Program memory | 8 kilobytes |
| Power requirements | |
| | +12 volts, 85 milliamps |
| | -12 volts, 1 milliamp |

## Functional Specifications

| | |
|---|---|
| Event recording | |
| Criteria | long term vs short term |
| LTA time constant | 5 minutes |
| STA time constant | 50 milliseconds to 0.5 seconds software selectable |
| Threshold | 6 to 24dB software selectable |
| Operational range | 70dB |
| Program window | |
| Number of windows | 9 |
| Turn-on delay | software selectable |
| Number experiments/window | 1 to 9999 software selectable |
| Window spacing | 1 to 99minutes software selectable |
| Offset | 0 to 99 seconds software selectable |

| Cartridge Recorder Specifications | |
|---|---|
| Data capacity | 17.5 Megabytes |
| Density | 6400 BPI |
| Number of tracks | 4 |
| Power Requirement (maximum values) | +12 volts, 0.5 amps<br>-12 volts, 0.5 amps<br>+5 volts, 2.25 amps |

FIGURES

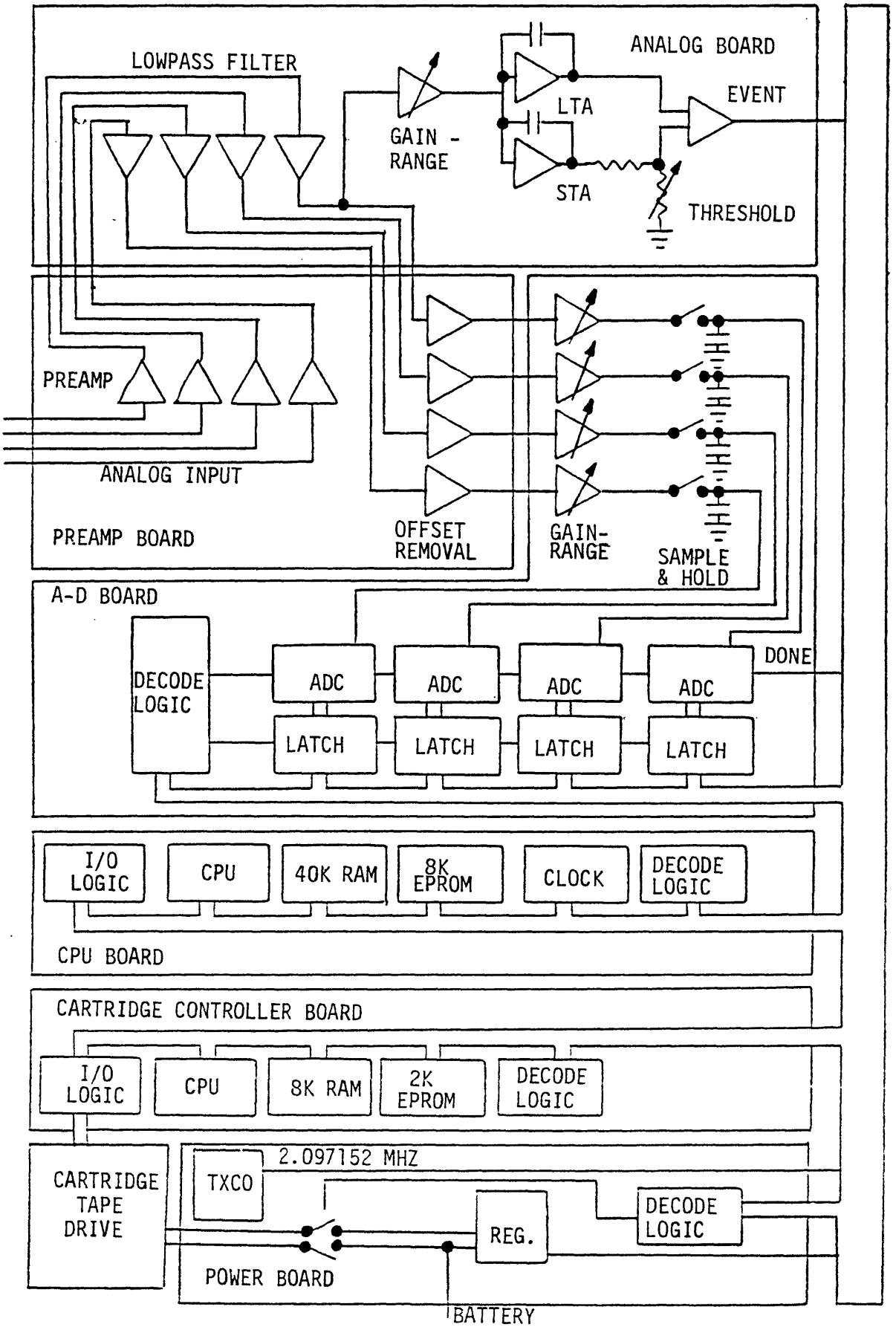



FIGURE 1. Block Diagram of the Geophysical Data-Acquisition System

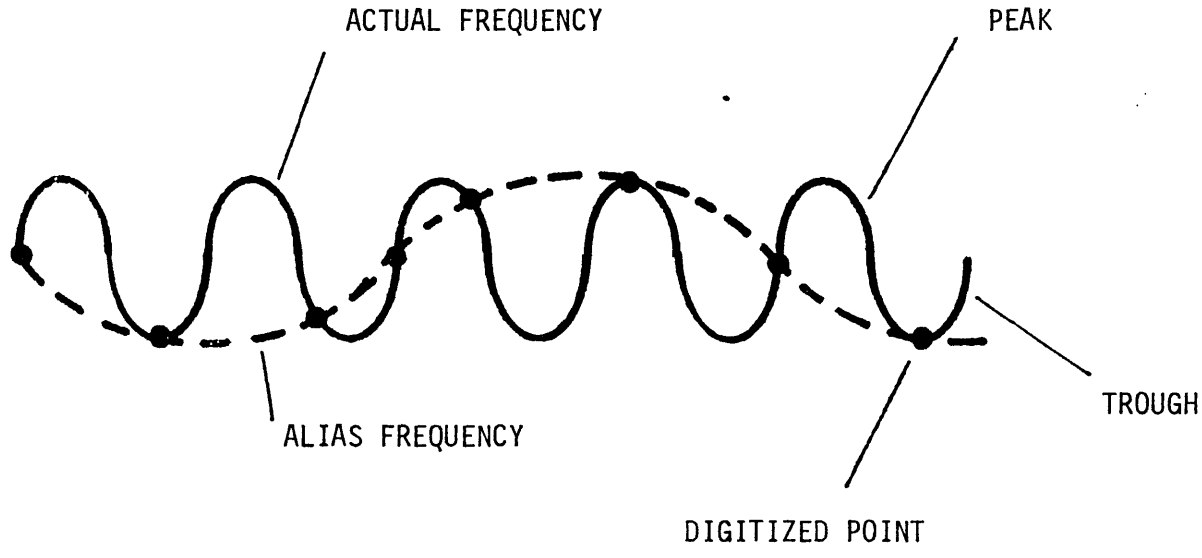



FIGURE 2. Aliasing of Analog Signals

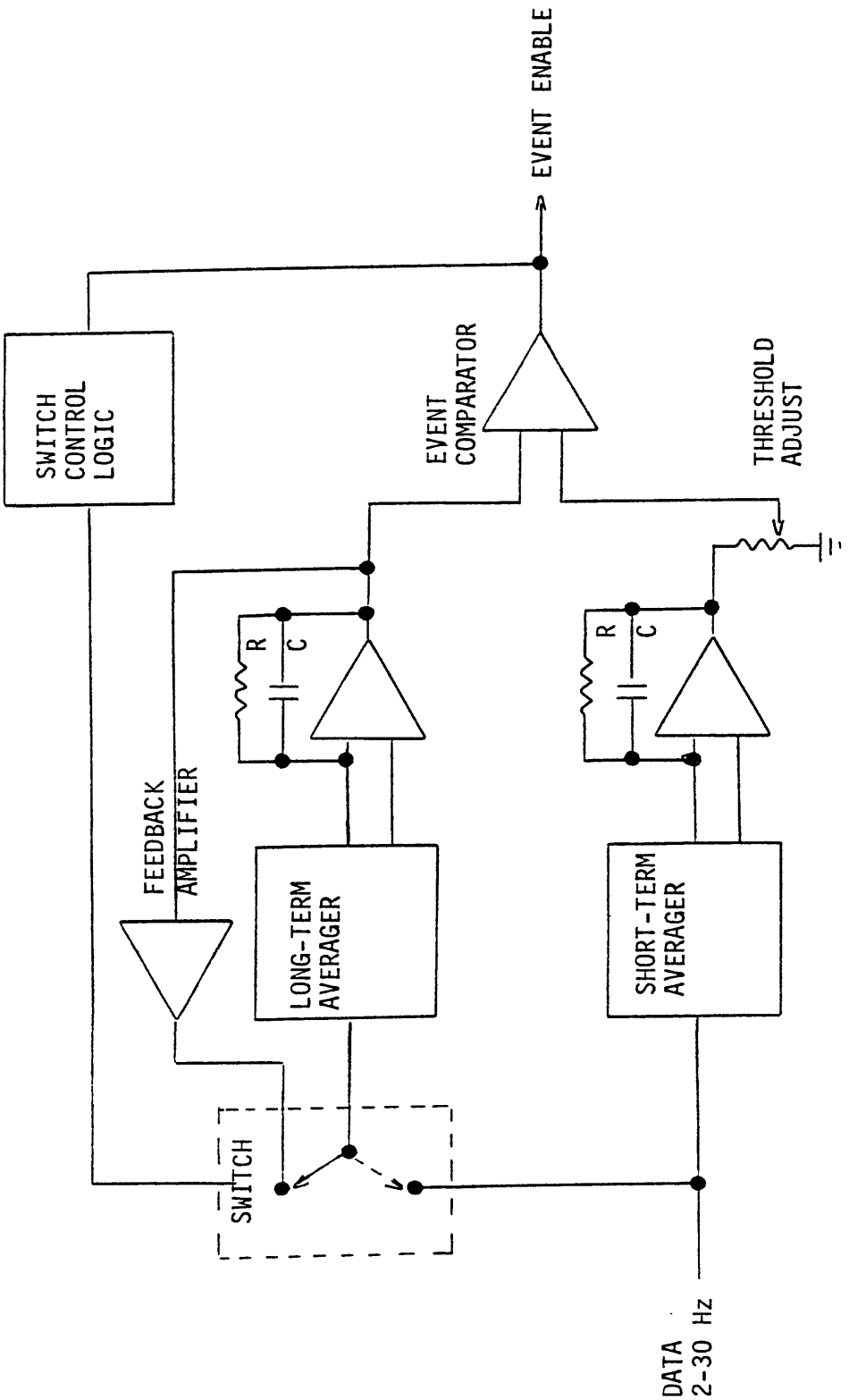



FIGURE 3. Block Diagram of Event-Detection Circuitry

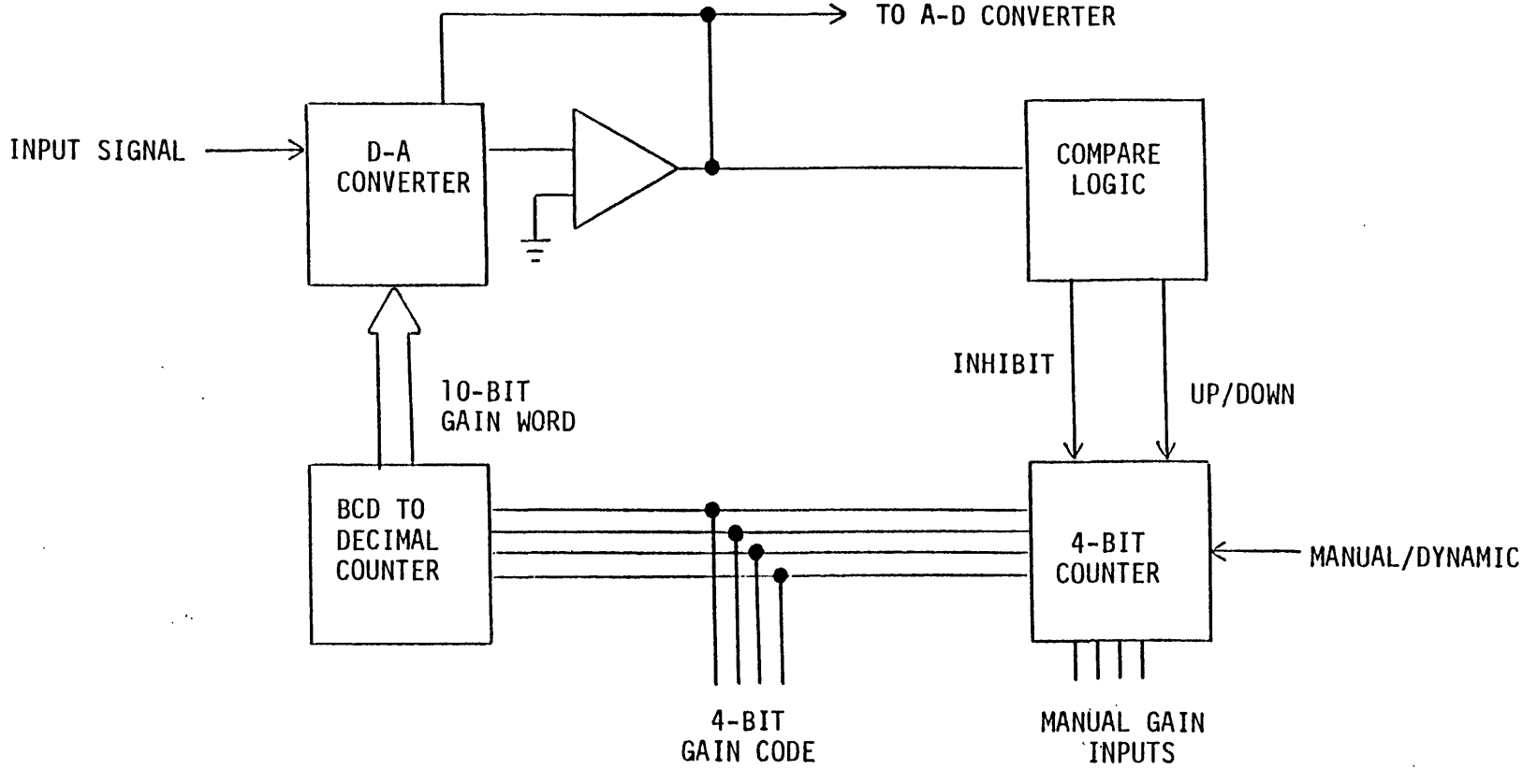



FIGURE 4. Block Diagram of Gain-Ranging Circuitry

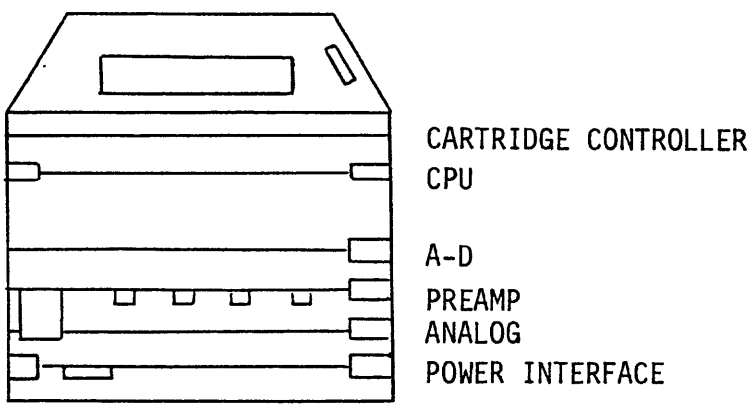



FIGURE 5. Location of Circuit Boards on the Bus

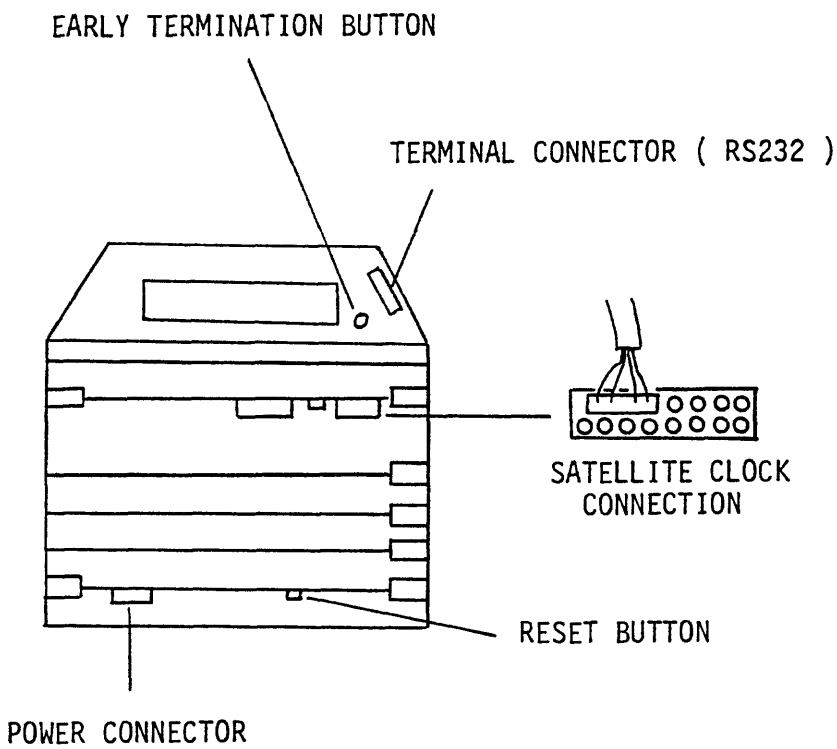



FIGURE 6. User Connections and Controls

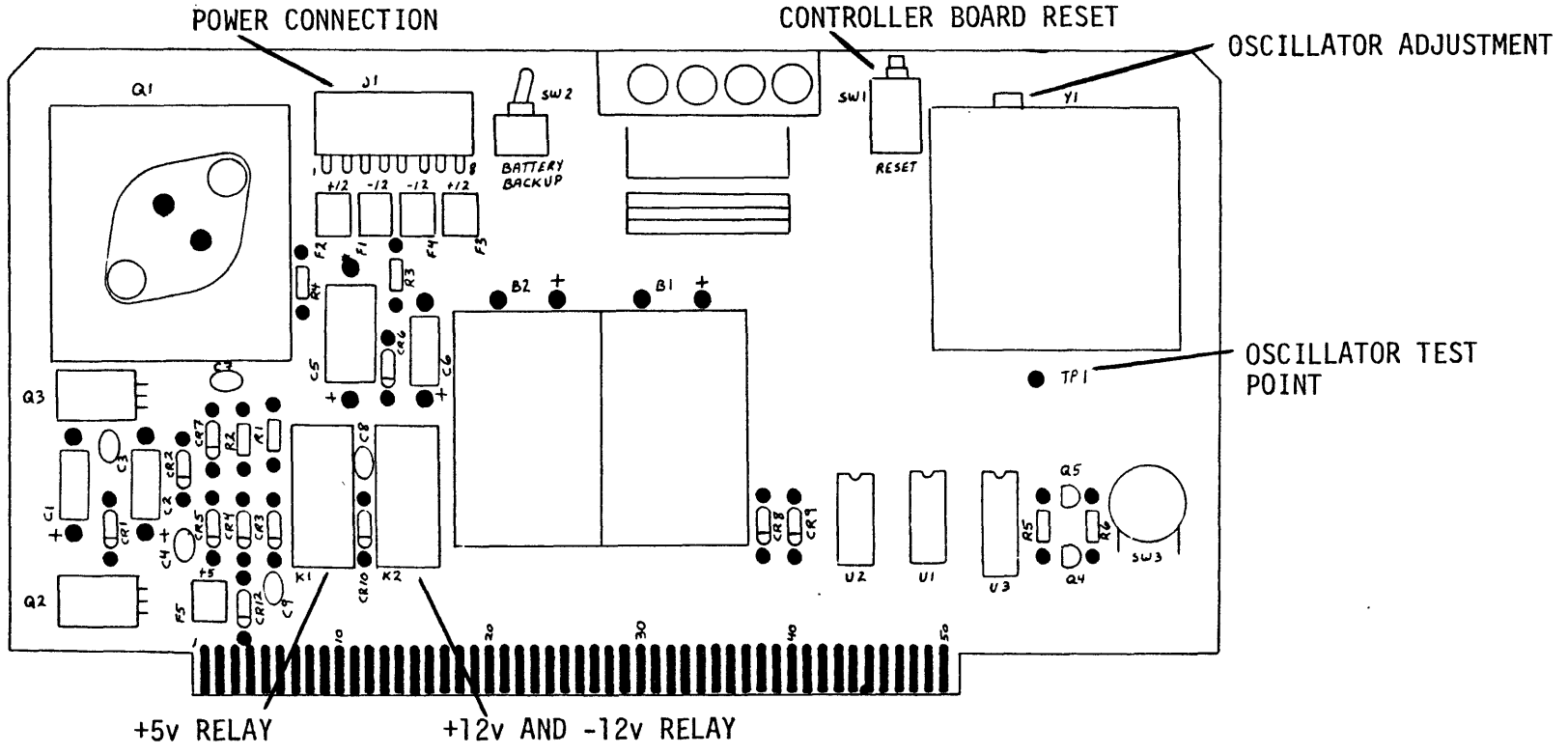



FIGURE 7. Component Layout of the Power Interface Board

| | | |
|---|---|---|
| POWER INTERFACE BOARD - COMPONENT LAYOUT | | |
| SCALE: 1:1 | APPROVED BY | DRAWN BY GKM |
| DATE: 6 MAY 86 | | |
| | | |
| MOD 3 | | DRAWING NUMBER |

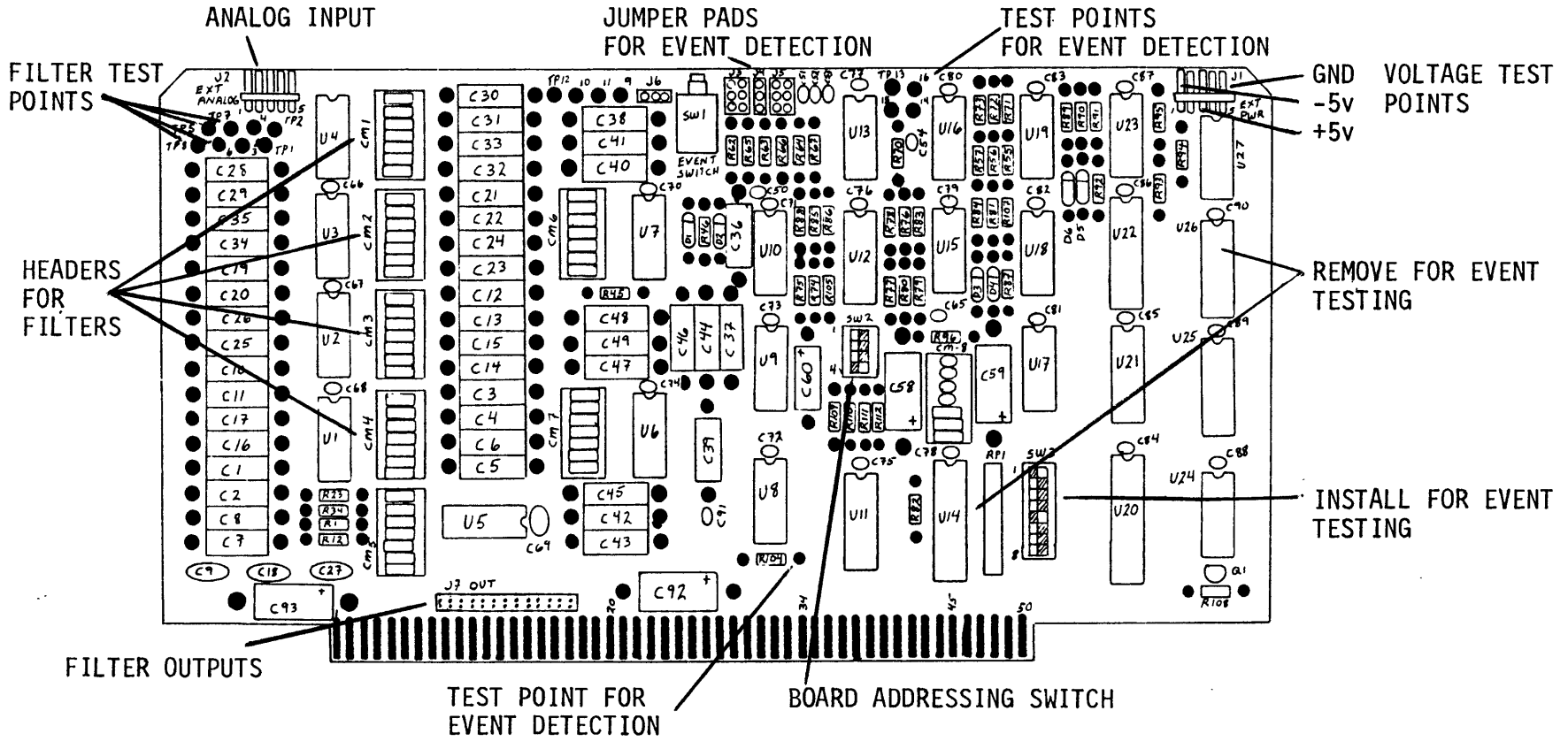



FIGURE 8. Component Layout of the Analog Board

| | | |
|---|---|---|
| ANALOG BOARD - COMPONENT LAYOUT | | |
| SCALE: 1:1 | APPROVED BY | DRAWN BY |
| DATE: 6 MAY 86 | | GKM |
| | | |
| MOD5 | | DRAWING NUMBER |

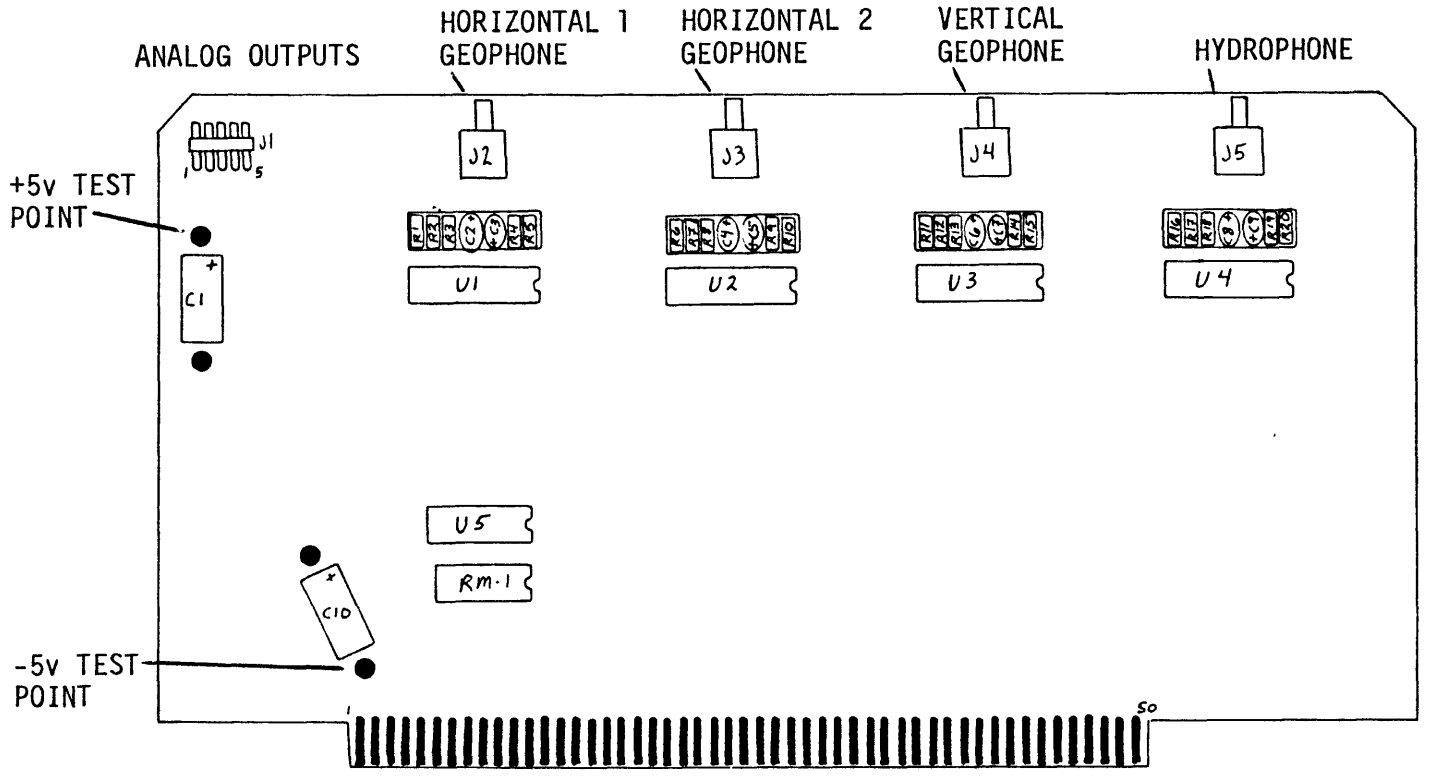



FIGURE 9. Component Layout of the Preamplifier Board

| | | |
|---|---|---|
| PREAMPLIFIER BOARD - COMPONENT LAYOUT | | |
| SCALE: 1:1 | APPROVED BY | DRAWN BY GKM |
| DATE: 9 MAY 86 | | |
| | | DRAWING NUMBER |
| MOD 1 | | |

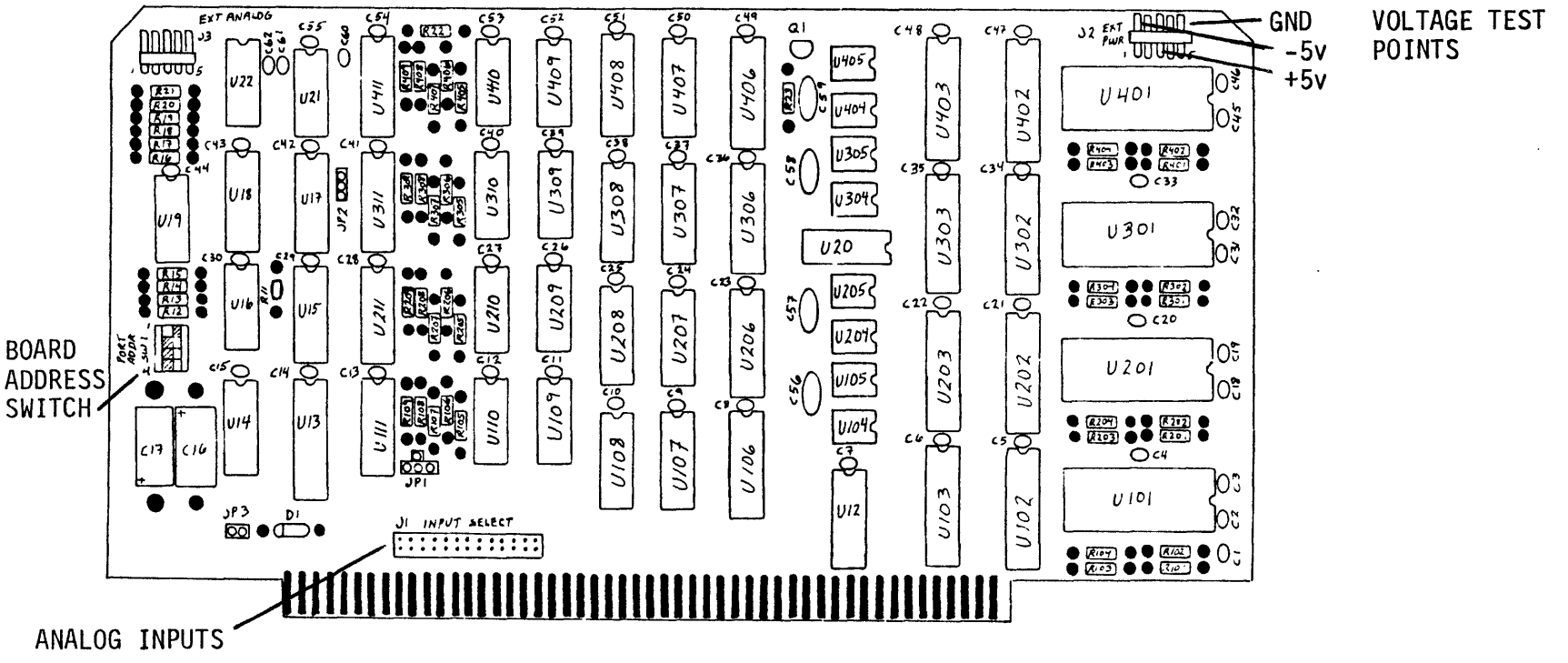



FIGURE 10. Component Layout of the Analog-to-Digital Board

| | | |
|---|---|---|
| ANALOG-TO-DIGITAL BOARD - COMPONENT LAYOUT | | |
| SCALE: 1:1 | APPROVED BY | DRAWN BY GKM |
| DATE: 7 MAY 86 | | |
| | | DRAWING NUMBER |
| mod 2 | | |

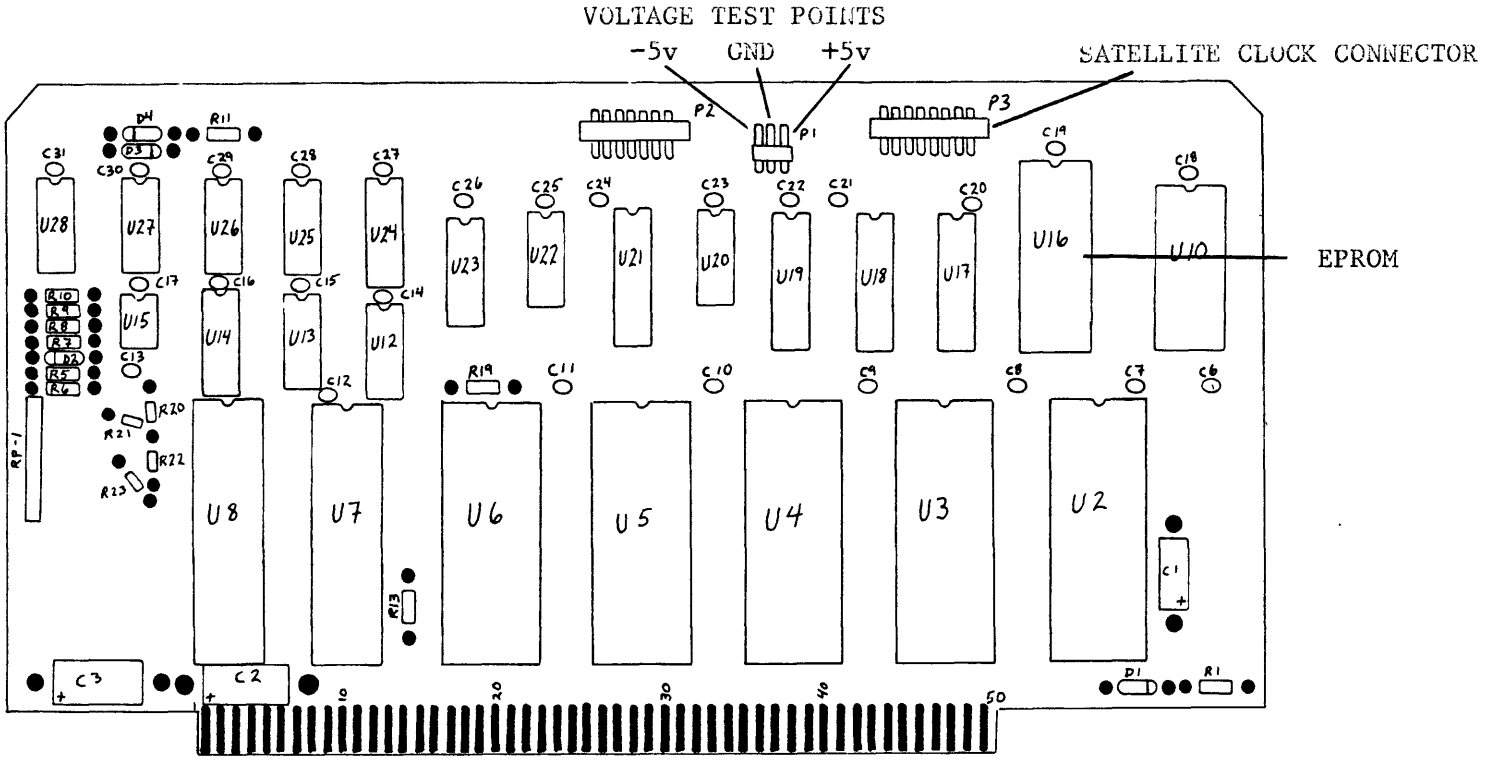



FIGURE 11. Component Layout of the Controller Board

| | | |
|---|---|---|
| CONTROLLER BOARD - COMPONENT LAYOUT | | |
| SCALE: 1:1 | APPROVED BY | DRAWN BY |
| DATE: 8 MAY 86 | | GKM |
| | | |
| MOD 4 | | DRAWING NUMBER |

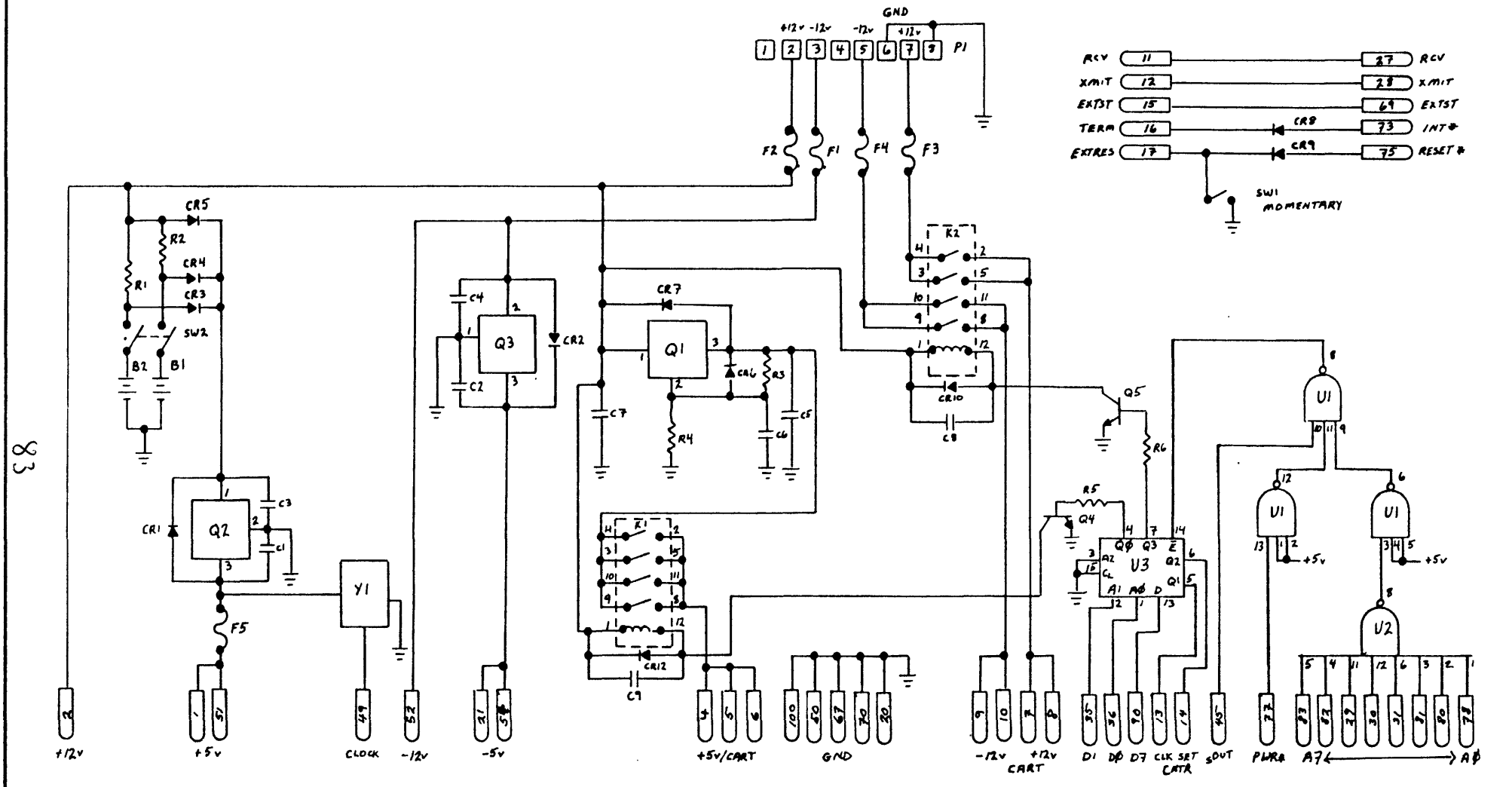



Figure 12. Schematic of the Power Interface Board

BUS CONNECTOR

| TITLE | POWER INTERFACE BOARD mod 3 |
|---|---|
| | SHEET 1 |

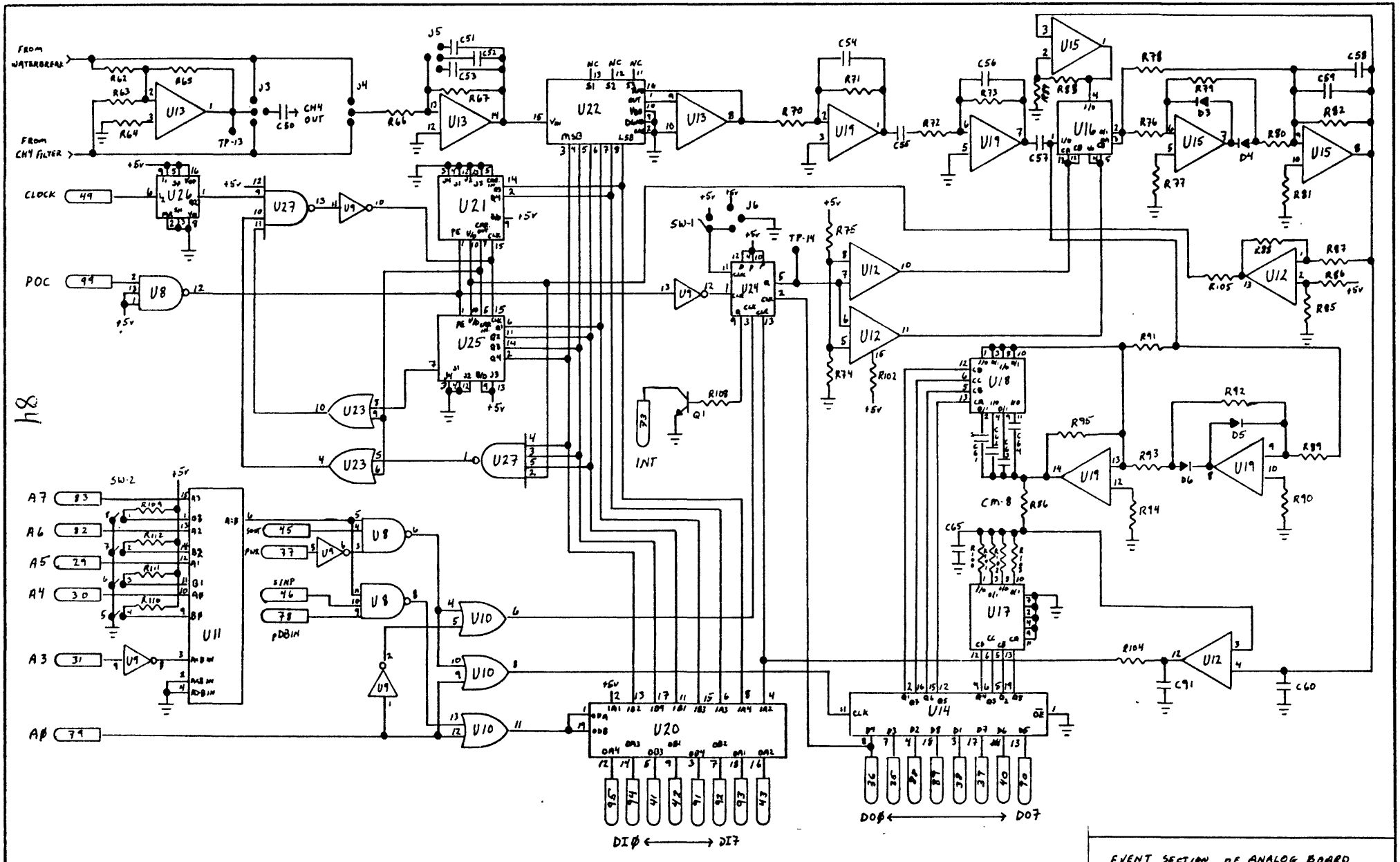



FIGURE 13. Schematic of the Event-Detection Circuits

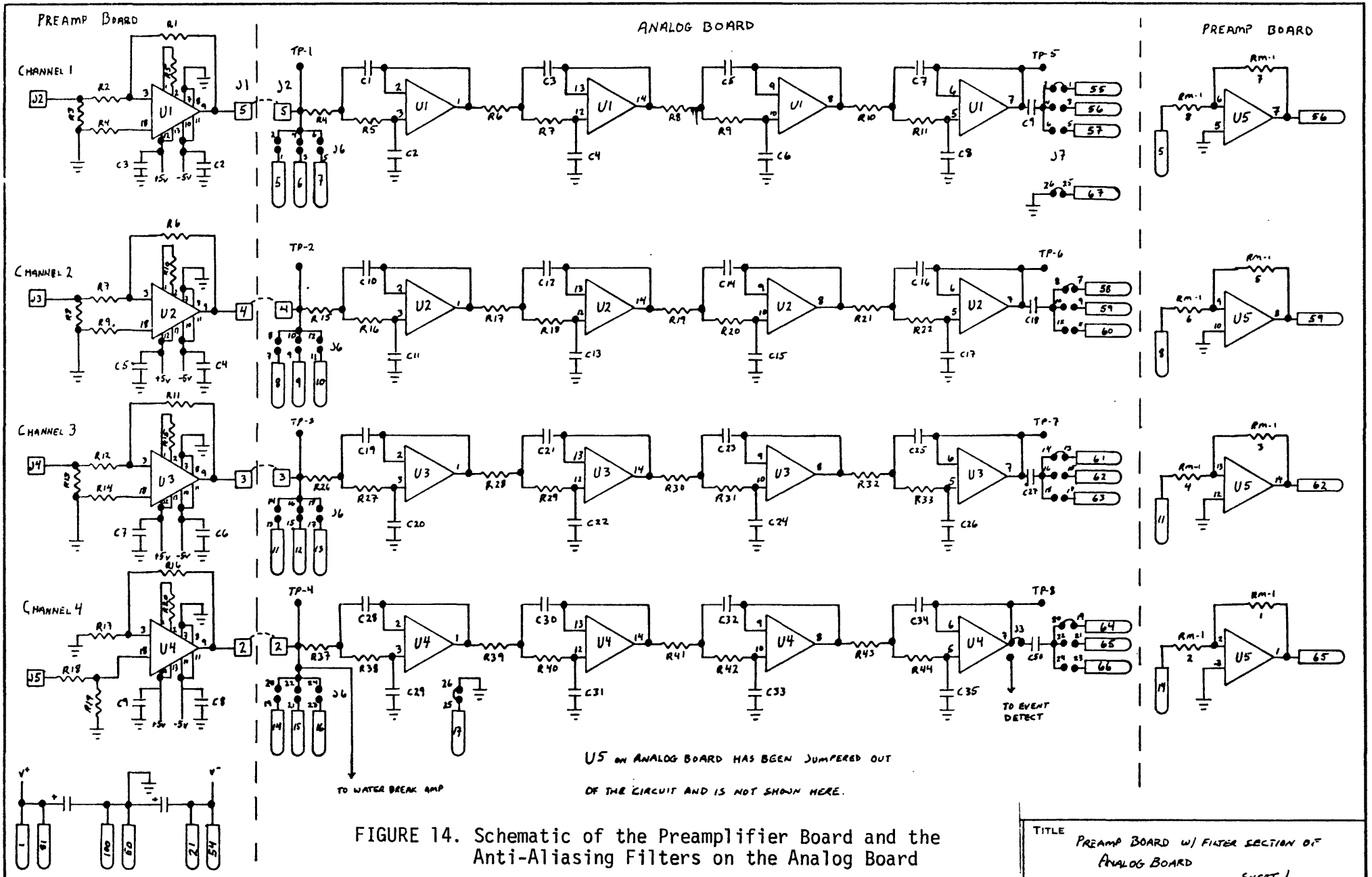



FIGURE 14. Schematic of the Preamplifier Board and the Anti-Aliasing Filters on the Analog Board

| TITLE | |
|---|---|
| | PREAMP BOARD W/ FILTER SECTION OF ANALOG BOARD |
| | SHEET 1 |

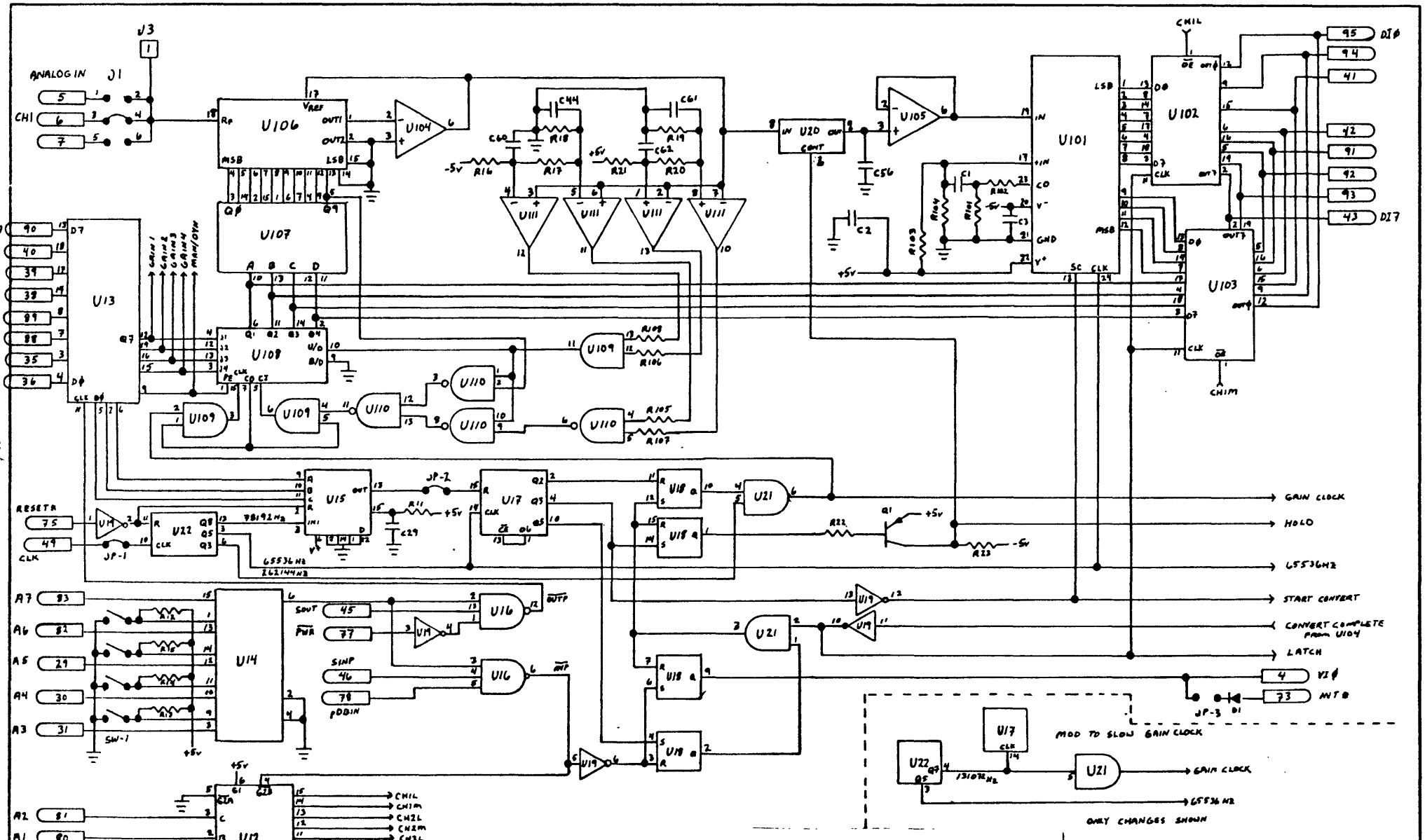



FIGURE 15. Schematic of the Analog-to-Digital Board Channel 1 and Timing Circuits

| | |
|---|---|
| TITLE | A-D BOARD MOD 3 |
| | CHANNEL 1 + TIMING |
| | SHEET 1 OF 3 |

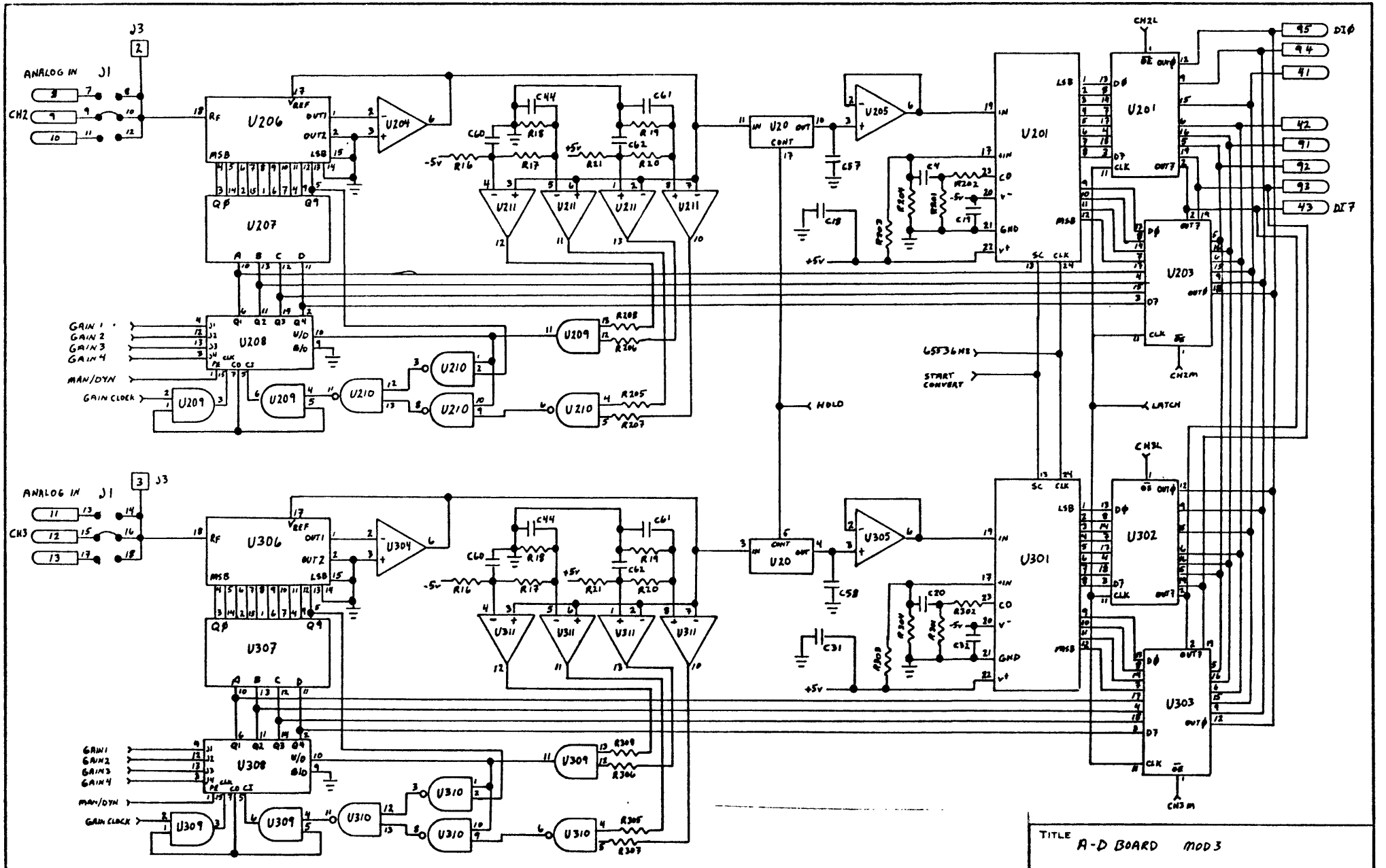
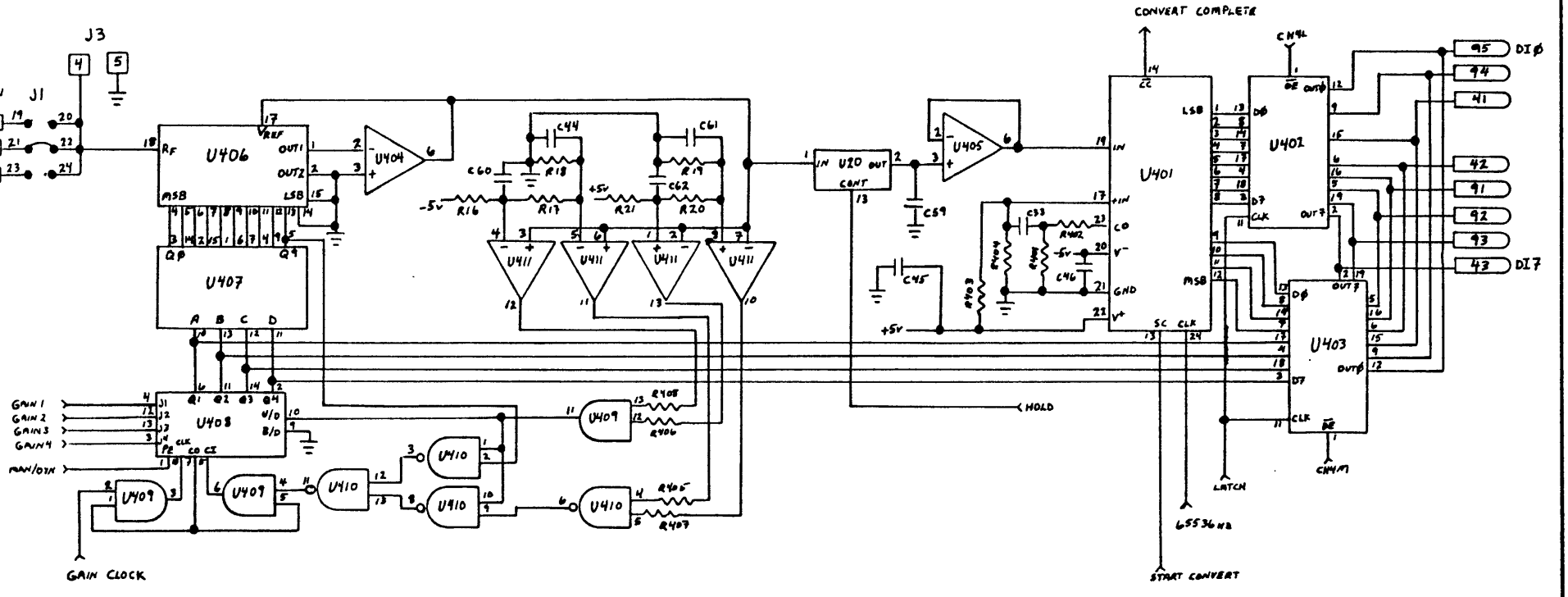



FIGURE 16. Schematic of the Analog-to-Digital Board Channels 2+3



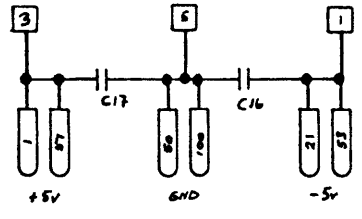




FIGURE 17. Schematic of the Analog-to-Digital Board Channel 4 Circuits

| | |
|---|---|
| TITLE | A-D BOARD MOD 3 |
| CHANNEL 4 | SHEET 3 of 3 |

88

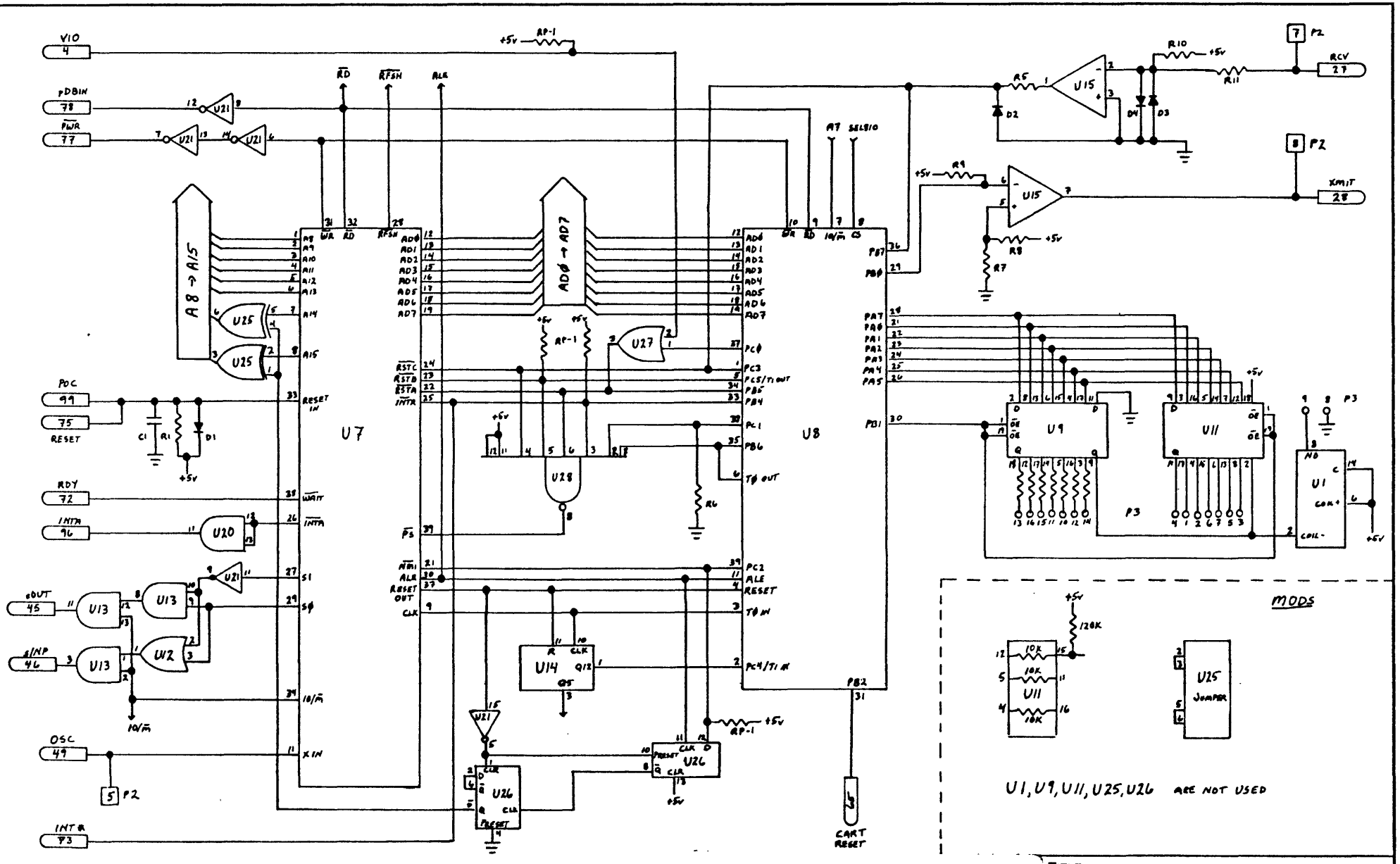



FIGURE 18. Schematic of the Controller Board Address and Input/Output Circuits

TITLE CPU BOARD MOD 4

CPU & I/O SHEET 1 of 2

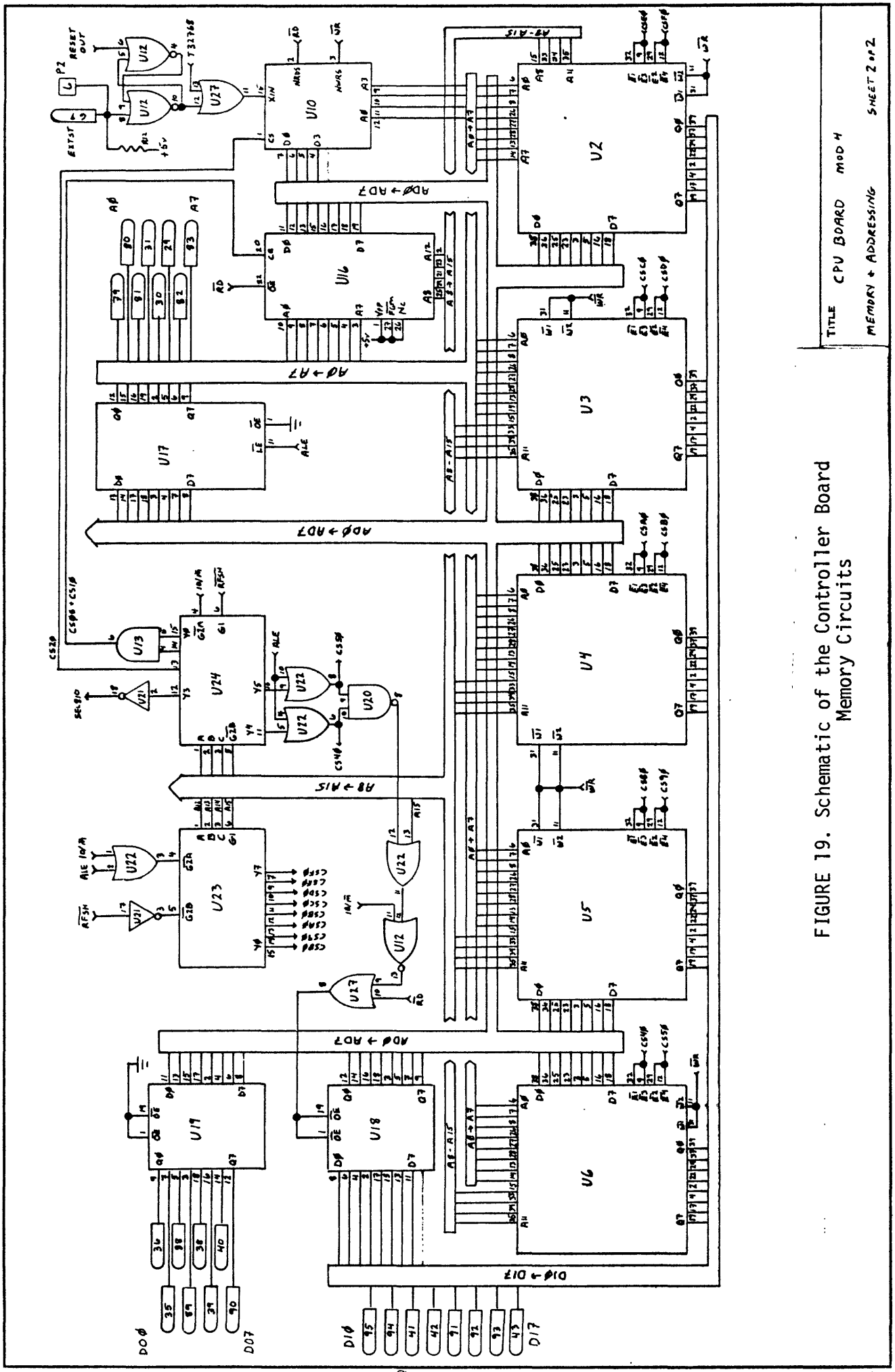



FIGURE 19. Schematic of the Controller Board
Memory Circuits