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EXPANDING THE INPUT MULTIPLEXER FOR THE DATA TRANSLATION, INC. MODEL DT2821 ANALOG-TO-DIGITAL CONVERTER

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1. INTRODUCTION

W.H.K. Lee, et. al., (1988) have developed a computer data acquisition and processing system based upon the I.B.M. PC-AT technology. The system was designed to monitor local seismograph networks. This system uses a model DT2821 Analog-to-Digital Converter (ADC) manufactured by Data Translation, Inc. (DTI) of Marlboro, MA.

This ADC will digitize from one to sixteen channels, sufficient for only the smallest of networks. This report describes how to expand the number of input channels from sixteen to sixty-four in sixteen channel increments.

2. DESIGN PRINCIPLES

The ADC card uses a 74F161 four bit synchronous counter to generate the address bits for the internal multiplexer. Fortunately, this counter is designed to be cascadeable, i.e., counter packages can be connected serially to produce counters of arbitrary length. Control signals connected among the counter packages in a chain maintain synchronism among the packages in the chain. Synchronism, in this case, means that all functions and output changes occur at some constant interval after the clock signal becomes active.

This is in contrast to "ripple" counters in which an output from a counter early in the chain is the input to the next counter in the chain, etc. causing the changes in the state of the counters to "ripple" down from the earlier counters to the later ones. If a designer needs to decode the state of a counter chain to control another function, ripple counters can cause "glitches", spurious signals of short (10-20 nanosecond) duration, to appear at the output of the decoder circuit. These "glitches" occur because the outputs of the counter assume many spurious states as the count ripples down the chain.

In a synchronous counter chain, the clock (CK) input of every counter package in the chain is driven by the same signal. A ripple carry out (RCO) signal from the first counter in the chain is connected to an enable (EN) input of the next counter in the chain and so on down the chain of counter packages. The RCO signal goes active when its counter reaches its terminal state. This active signal on the EN pin of the second counter allows that counter to increment at the next active CK signal.

Consider an eight bit synchronous binary counter consisting of two four bit counter packages. Both counters have been cleared so the contents of the two counters are 0000 0000 binary. After the

CK has gone active 15 times, the contents are 0000 1111. The first counter has reached its terminal count and its RCO has gone active, ENabling the second counter. At the next active clock, the first counter increments to 0000 and the second counter increments to 0001, making the contents of the two package eight-bit counter 0001 0000. Since the first counter is no longer at its terminal count, its RCO has gone inactive, disabling the second counter from responding to the CK signal. This sequence continues until the counters are "full", i.e. 1111 1111, at which point they both increment to 0000 0000, or the sequence continues until it is interrupted by making the clear (CLR) pin active, thereby setting all the outputs to zero, or by making the load (LD) pin active, thereby causing the counters outputs to assume the state of the signals at the counter input pins.

The point of this exercise is to generate a set of signals suitable for controlling the switching action of a set of multiplexer circuits.

3. 64 CHANNEL MULTIPLEXER

A. Construction

Refer to Figure 1.

Signals to control the synchronous counter U1 plus Vcc and digital ground are obtained by soldering wires to the circuit side of U27, a 74161 synchronous counter on the ADC board. Flat ribbon cable is appropriate. After soldering five conductors in the ribbon cable to the bottom of U27, a suitable connector should be attached to the free end of the cable to make connection to the multiplexer board. An appropriately sized slot can be cut in the ADC mounting bracket to allow the newly added cable to pass to the outside of the computer. When the multiplexer board is not being used with the computer, the cable can be neatly rolled up and secured out of the way at the rear of the computer.

All other interconnections between the ADC and the multiplexer are made at the 50 pin ribbon cable connector at the rear of the ADC. A like connector should be mounted on the Multiplexer with a 50 conductor flat cable between the two.

B. Theory of operation

This circuit has few enough components that one may "steal" power from the ADC. The ADC has a DC-to-DC converter which

converts the +5 VDC logic power to ±15 VDC for the analog circuits. This converter is rated at 150 mA for each output. The analog circuits on the ADC draw a maximum of 55 mA from the +15 V and 95 mA from the -15 V. Each multiplexer I.C. draws a maximum current of 2.4 mA from the positive supply and a maximum of 1.5 mA from the negative supply for a total of 19.2 mA and 12 mA, respectively, from the two sides of the converter. One can use straight 7400 TTL I.C.s for the logic circuit but it would be best to use Complementary Metal Oxide Semiconductor (CMOS), 74C00 or Low-power Schottky (LS) 74LS00 logic devices.

The sixty four channel multiplexer circuit consists of eight dual four-to-one multiplexer integrated circuits, a synchronous counter and decoding logic. This circuit will multiplex 16, 32, 48 or 64 channels. The number of channels is program controlled.

Analog input signal switching is accomplished in the eight dual four channel multiplexers, U11 through U18. Each four channel multiplexer is the equivalent of a single-pole four position switch with the pole position determined by the two address bit inputs, A0 and A1. The switches S1-S4 are selected by address bit input patterns 00, 01, 10 and 11, respectively. When the Enable pin (EN) is low, all inputs are disconnected from outputs. When EN is high, the input selected by the address bits is connected to the output.

The counter may be either a 74160 BCD counter or a 74161 4-bit binary counter, since, in this application, the counter is never allowed to count past three (0011). The counter uses the same CLR and CLK signal as the multiplexer address counter on the ADC. Using the same CLR signal insures that the counter on the external multiplexer will be initiated at the same time the ADC counter is initiated by the software.

The number of multiplexed channels is controlled by Digital Input/Output (DIO) bits 0, 1 and 2 of DIO byte 0. For 16 channels, all three bits are set low. For 32, 48 or 64 channels, bits 0, 1 or 2 ,respectively, are set high by the controlling program. These three bits are connected to the inputs of the three-input and gates U4, U5, U6 and U7. The first three are high-active input gates while the fourth is a low-active input gate.

If all three control signals are low, for 16 channel operation, at least one input of U4-6 is low causing their outputs to be low. The three low signals at the inputs of U7 cause its output to be high and the output of U10 sends a continuous low signal to the LOAD (LD) input of the counter. When the LD signal is low and the CLK goes active, the signals at the four inputs A, B, C and D are loaded into the

four flip-flops of the counter. Since these inputs are wired low, executing a LD function will have the same effect as clearing the counter. With a continuous low at the LD input, the counter is reset by every clock pulse, the counter outputs never change, the multiplexer outputs are always connected to S1 inputs and the ADC functions as it would with no external multiplexer.

If one wishes to digitize 32 channels, one would raise DIO bit 0 to a high. Now U7 is disabled by the high on one of its inputs so that its output always stays low. U5 and U6 are still disabled by the presence of a continuous low on one of their inputs so their outputs will remain low. However, with its control input now high, U4's output can go high if its other two inputs ever go high at the same time.

At the outset of an ADC sweep, U1 has been cleared and its outputs A0 and A1 are low. All multiplexer S1s are selected and multiplexer channels 1-16 are connected to ADC analog inputs 1-16. With A0 low, U4 is still disabled.

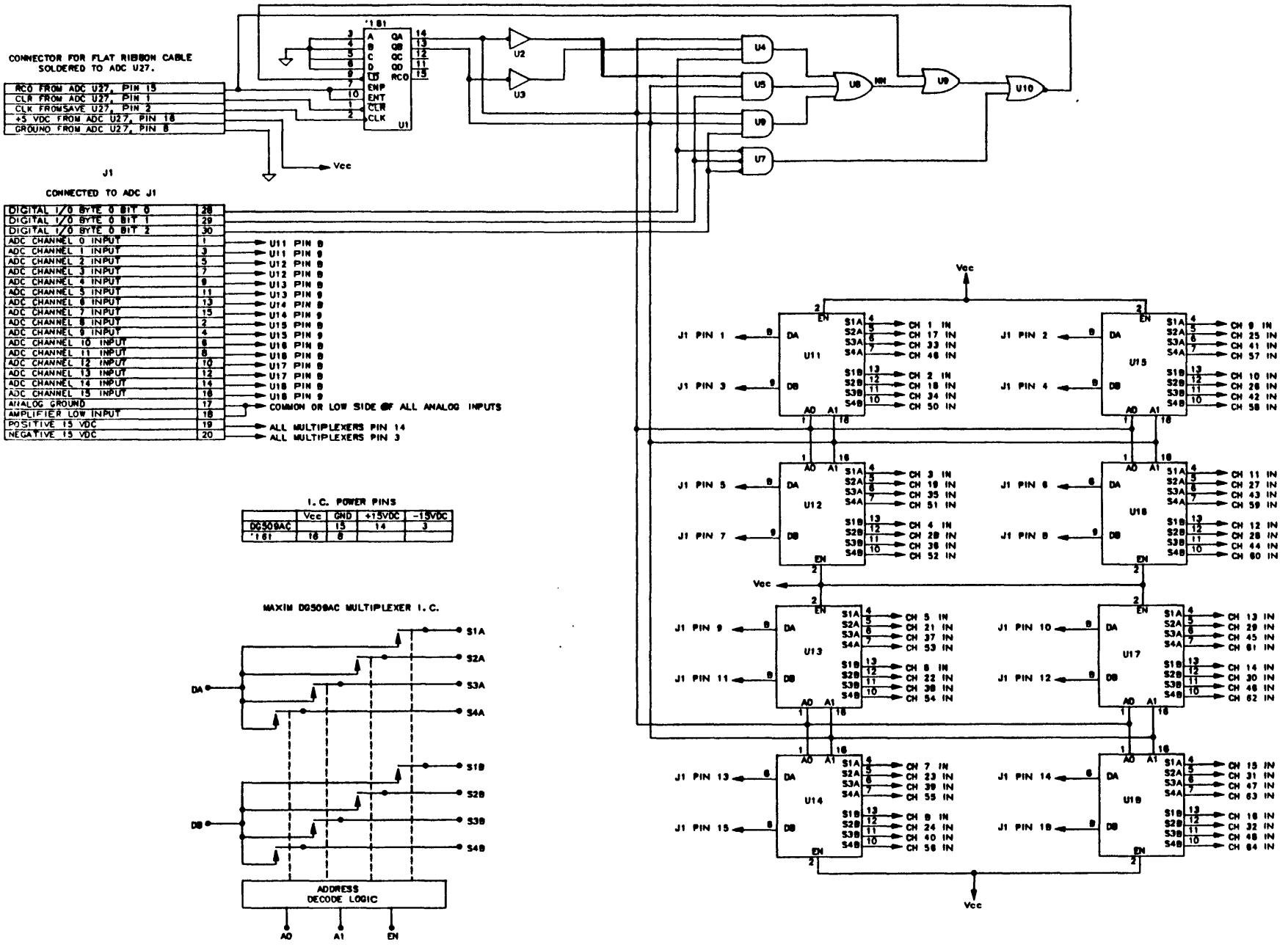
The ADC sequentially digitizes its 16 inputs, during the course of which, its internal counter has incremented from 0000 to 1111. When it reached its terminal count of 1111, its RCO signal goes high. The condition of U1 is that its count enable inputs have been made active by the high level from the ADC's RCO signal and its LD signal is inactive so the next CLK will cause the counter to increment from 00 to 01. The same clock pulse increments the ADC's counter from 1111 to 0000 causing its RCO to go low. Now, A0 is high putting a high at the first input of U4; A1 is low but it is inverted to a high by U3 and sent to U4's second input and U4's third input is already high from DIO bit 0, so U4's output now goes high causing a high at U8's output and at one input of U9. However, the other input to U9 is connected to RCO, which has just gone low, so U9's output stays low, U10's output stays high and the LD input of the counter is not enabled.

The change of the multiplexer address bits from 00 to 01 has caused all of the switches to switch from S1 to S2 so that input channels 17-32 are now connected to ADC inputs 1-16. The ADC now digitizes the new set of 16 inputs exactly as above but this time when the ADC counter reaches 1111 and its RCO goes high, the high from the output of U4 propogates through U8, U9 and U10 and ends up as an enabling low level at U1's LD pin. This time, the very next clock signal will cause the ADC's counter to increment to 0000 and also will load all lows into U1, taking the circuit back to its original condition and the 32 analog inputs are scanned again.

The principle of operation is the same for 48 and 64 channels with a different decoder U5 or U6 enabled by a different DIO bit and decoding a different set of values of A0 and A1.

REFERENCES

Lee, W.H.K., D.M Tottingham and J.O. Ellis, 1988. A PC-based seismic data acquisition and processing system, U.S. Geol. Surv. Open-file Report 88-751, 31 pp.


CONNECTOR FOR FLAT RIBBON CABLE SOLDERED TO ADC U27.
RCO FROM ADC U27, PIN 15
CLR FROM ADC U27, PIN 1
CLK FROMSAVE U27, PIN 2
+5 VDC FROM ADC U27, PIN 16
GROUND FROM ADC U27, PIN 8
'161
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
Vcc
J1
CONNECTED TO ADC J1
DIGITAL I/O BYTE 0 BIT 0 28
DIGITAL I/O BYTE 0 BIT 1 29
DIGITAL I/O BYTE 0 BIT 2 30
ADC CHANNEL 0 INPUT 1 → U11 PIN 8
ADC CHANNEL 1 INPUT 3 → U11 PIN 9
ADC CHANNEL 2 INPUT 5 → U12 PIN 8
ADC CHANNEL 3 INPUT 7 → U12 PIN 9
ADC CHANNEL 4 INPUT 9 → U13 PIN 8
ADC CHANNEL 5 INPUT 11 → U13 PIN 9
ADC CHANNEL 6 INPUT 13 → U14 PIN 8
ADC CHANNEL 7 INPUT 15 → U14 PIN 9
ADC CHANNEL 8 INPUT 2 → U15 PIN 8
ADC CHANNEL 9 INPUT 4 → U15 PIN 9
ADC CHANNEL 10 INPUT 6 → U16 PIN 8
ADC CHANNEL 11 INPUT 8 → U16 PIN 9
ADC CHANNEL 12 INPUT 10 → U17 PIN 8
ADC CHANNEL 13 INPUT 12 → U17 PIN 9
ADC CHANNEL 14 INPUT 14 → U18 PIN 8
ADC CHANNEL 15 INPUT 16 → U18 PIN 9
ANALOG GROUND 17 → COMMON OR LOW SIDE OF ALL ANALOG INPUTS
AMPLIFIER LOW INPUT 18
POSITIVE 15 VDC 19 → ALL MULTIPLEXERS PIN 14
NEGATIVE 15 VDC 20 → ALL MULTIPLEXERS PIN 3
I.C. POWER PINS
DG509AC Vcc 16 GND 8 +15VDC 15 -15VDC 14 3
'161 16 8
MAXIM DG509AC MULTIPLEXER I.C.
DA
DB
S1A
S2A
S3A
S4A
S1B
S2B
S3B
S4B
ADDRESS DECODE LOGIC
A0
A1
EN
U11
U12
U13
U14
U15
U16
U17
U18
U19
J1 PIN 1
J1 PIN 2
J1 PIN 3
J1 PIN 4
J1 PIN 5
J1 PIN 6
J1 PIN 7
J1 PIN 8
J1 PIN 9
J1 PIN 10
J1 PIN 11
J1 PIN 12
J1 PIN 13
J1 PIN 14
J1 PIN 15
J1 PIN 16
CH 1 IN
CH 17 IN
CH 33 IN
CH 49 IN
CH 2 IN
CH 18 IN
CH 34 IN
CH 50 IN
CH 3 IN
CH 19 IN
CH 35 IN
CH 51 IN
CH 4 IN
CH 20 IN
CH 36 IN
CH 52 IN
CH 5 IN
CH 21 IN
CH 37 IN
CH 53 IN
CH 6 IN
CH 22 IN
CH 38 IN
CH 54 IN
CH 7 IN
CH 23 IN
CH 39 IN
CH 55 IN
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CH 10 IN
CH 26 IN
CH 42 IN
CH 58 IN
CH 11 IN
CH 27 IN
CH 43 IN
CH 59 IN
CH 12 IN
CH 28 IN
CH 44 IN
CH 60 IN
CH 13 IN
CH 29 IN
CH 45 IN
CH 61 IN
CH 14 IN
CH 30 IN
CH 46 IN
CH 62 IN
CH 15 IN
CH 31 IN
CH 47 IN
CH 63 IN
CH 16 IN
CH 32 IN
CH 48 IN
CH 64 IN

FIGURE 1

ADDENDUM (June 25, 1990) to USGS Open-File Report 89-201

A printed circuit board for a 128-channel multiplexer was designed by E. G. Jensen and J. R. Rogers based on the proto-type design of USGS Open-File Report 89-201. A list of necessary parts is shown below. Anyone interested in making such a multiplexer may order the "USGS MUX128" printed circuit board via Martex Circuits, Inc., 875 Maude Ave., Mountain View, CA 94043 (Telephone: 415-965-3004), or borrow the circuit board films from the USGS Library in Menlo Park.

Parts list for USGS 128-channel Multiplexer

#	Item	Part No.	Manufacturer	Quantity
1	IC	DG508A	Maxia	16
2	IC	74LS161	Motorola	1
3	IC	74LS85	Motorola	1
4	IC	74LS04	Motorola	1
5	PCB	USGS MUX128	Martex	1
6	Capacitor	15uF, 15v tanalum	Sprague	1
7	Capacitor	.1uF, ceramic	AVX	3
8	Cable, twist flat	843-132-2801-016	Amphenol-spectra strip	100 ft
9	Cable, ribbon flat	135-2801-050	Amphenol-spectra strip	10 ft
10	Connector,PCB,16 pin	65863-061	Dupont	16
11	Connector,PCB,10 pin	65863-091	Dupont	2
12	Connector,PCB,50 pin	85863-091	Dupont	1
13	Connector,PCB,16 pin	66900-216	Dupont	16
14	Connector,PCB,10 pin	66900-210	Dupont	2
15	Connector,PCB,50 pin	66900-250	Dupont	1
16	Enclosure	19" long 10" wide 3" height (open one end) bottom & top cover		
17	IC	MC14538B	Motorola	1
18	IC	MC14175B	Motorola	1
19	IC	MC14081B	Motorola	1
20	16-pin PCB IC socket	16MLP	Jameco	21
21	14-pin PCB IC socket	14MLP	Jameco	2
22	Breadboard	0.1" spacing proto	Vector	1
23	Spacers			6