UNITED STATES DEPARTMENT OF THE INTERIOR
GEOLOGICAL SURVEY

Short Wave Loop-Loop Sounder

by

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Introduction

This report describes a loop-loop sounder operating over a 0.1 MHz to 30 MHz range. It uses single turn transmitter and receiver coils with a center to center spacing of 0.5 meter to 5 meters. The transmitter and receiver are in separate boxes with fiber optic phase reference transmission between them. The readout provides in-phase and quadrature amplitudes of the receiver signal. The equipment is battery powered with a total weight of 40 pounds.

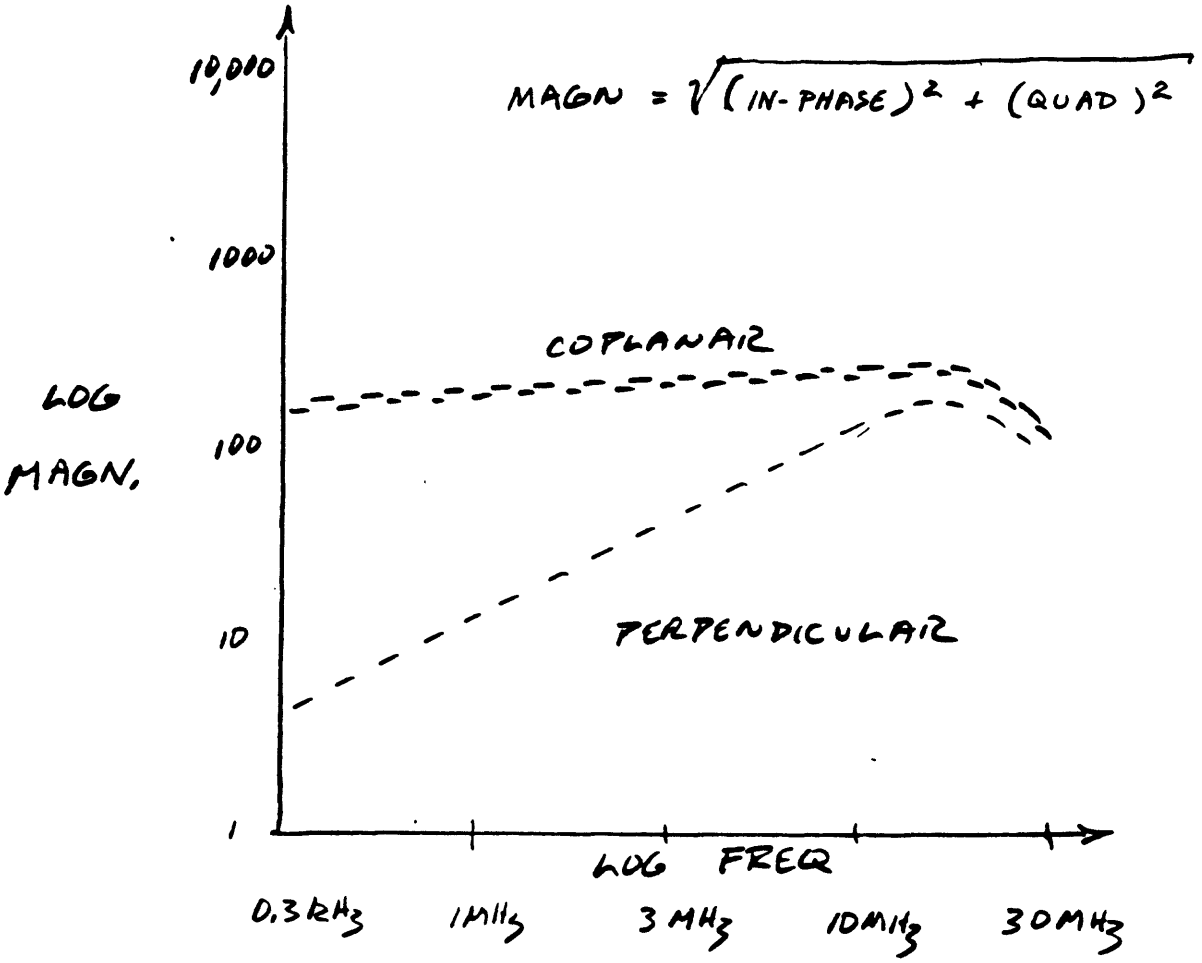
Loop-loop sounders are employed to measure the impedance of the earth between the coils. The penetration depth is proportional to the system dimensions, earth impedance and operating frequency. Prior applications include resistivity profiling near ore bodies and water depth measurement. This system is unique in its high frequency of operation and consequent limited penetration depth. It is more easily portable than most and will be useful in pollution studies, particularly petroleum spills, and shallow mapping in general.

Most loop-loop sounders operate at low frequencies where displacement currents are negligible (Kaufman and Keller, 1983). Above 10 MHz, capacitive effects are as important as resistive ones, and this sounder will respond to the complex impedance yielding information about soil dielectric constant. The low frequency coupling between a pair of coils can be analyzed by considering only the magnetic fields in analogy with a loosely coupled transformer (Wait, 1954). This short wave system has few applicable published solutions. The field situation is complicated by antenna effects in connecting cables and large phase shifts in the electronics and fiber optic cables. The raw field data from a sounding is shown in figure 1, with curves for amplitude and phase. There is no absolute reference for either curve, they must be compared to a calibration sounding. We calibrate in the lab by using a large sheet of aluminum, 8 x 12 feet, and locating the coils 0.5 meters apart and 7 inches above the sheet. This situation is amenable to theoretical calculations using images. The result is a flat amplitude response and constant phase shift versus frequency. This is convenient for analyzing field data; one computes the difference between calibration and field numbers and the difference curve is the the soil response.

There are several features of the amplitude sounding curves that are immediately apparent. There are two coil configurations shown: one has the coils coplanar and the second has the coils oriented at right angles with the axis of one coil aimed at the center of the other horizontal coil. The right angle configuration coupling increases with frequency and approaches the horizontal coplanar coupling at high frequency. This is consistent with theory. Both amplitudes decrease above 20 MHz due to instrumentation artifact: changes in gain in the system. This second feature must be 'subtracted out' by comparing the calibration and field data.

The phase curves have the expected 90^{o} shift between coplanar and right angle loops as well as two types of artifact. There is a two pole rolloff at 16 MHz due to the transmitter output capacitance and the loop inductance. There are two 'wiggles' at 7 and 21 MHz due to phase lock loop errors. Again, the artifacts are consistent during calibration and field tests and can be removed from the data.

FIGURE 1



FIELD DATA

MAGNITUDE + PHASE

System Description

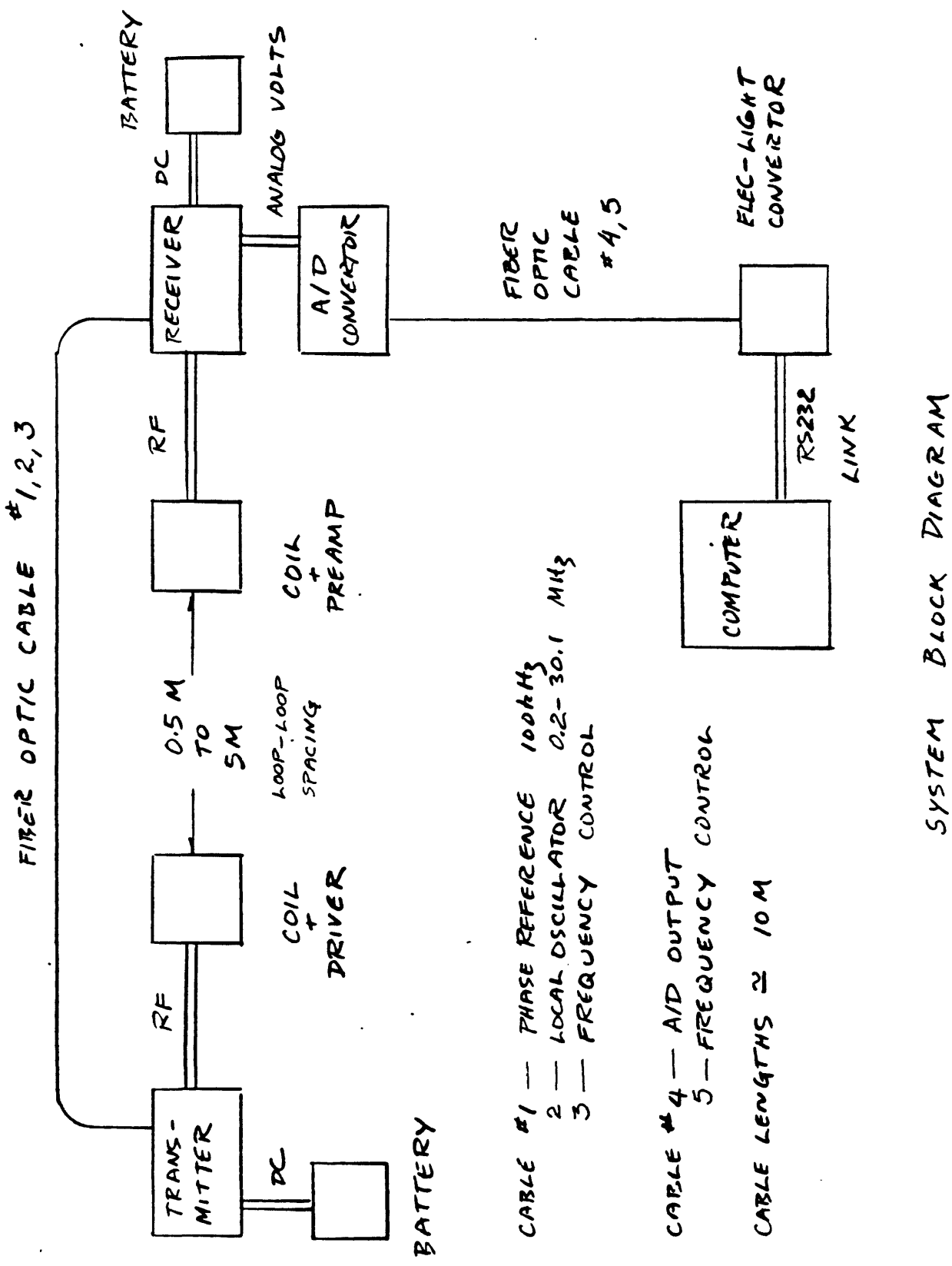
The sounder comprises 8 components: transmitter, receiver, two loops, two battery packs, analog to digital converter and RS 232 interface. The operator controls are located on the receiver. Normally the 6 radio frequency boxes are deployed in a line with the loops in the center and batteries at the ends. There are three fiber optic cables from transmitter to receiver. A sounding is taken by selecting a frequency from 0.1 MHz to 29.8 MHz with thumbwheel switches and writing down the in-phase and quadrature signal amplitudes appearing on a digital panel meter (DPM) on the receiver. The process is repeated until the entire curve of amplitude versus frequency is found. The data can also be taken under computer control.

The system block diagram is shown in figures 2 and 3. A 100 kHz crystal oscillator is the system reference. It drives three phase locked loops (PLL). The minimum frequency spacing is 100 kHz. The reference is sent to the receiver via fiber optic cable #1. The phase lock loops generate local oscillator (LO), radio frequency (RF) output and 50 MHz signals. The final frequencies, 0.1 MHz to 29.8 MHz, are generated by mixing 50.1 MHz through 79.8 MHz signals with the 50 MHz clock. This reduces the percentage tuning range required from the phase lock loops. The local oscillator signal is sent to the receiver via a second fiber optic cable. Its frequency is always 0.1 MHz higher than the RF output frequency. The RF signal is sent through a cable to the transmitter coil. There is an amplifier in the coil assembly. The third fiber optic cable carries frequency control settings from thumbwheels or latch circuits in the receiver to the PLL control circuits in the transmitter. This serial link uses Universal Asynchronous Receiver Transmitter (UART) chips. The control settings of 001 through 298 are converted to 501 through 798 and control the division ratios in the transmitter phase lock loops.

The receiver uses the 100 kHz signal as a phase reference in a synchronous detector. The in-phase and quadrature (SIN and COS) signals are generated by a 400 kHz phase lock loop and frequency divider. The local oscillator signal is mixed with the amplified output of the receiver coil to generate an intermediate frequency of 100 kHz. A narrow band intermediate frequency (IF) amplifier rejects noise and provides most of the receiver gain. The synchronous detector is an Analog Devices IC (AD630) intended for lock-in amplifier applications. The noise bandwidth of 1 Hz is determined by low pass filters at the detector output. These also determine the response speed of the system. Harmonic rejection is provided by the IF amplifier. Two detectors are used to generate in-phase (REAL) and quadrature (QUAD) voltages for display on a digital panel meter (DPM). A separate analog to digital converter (A/D) provides computer data logging via a serial (RS232) link.

The A/D uses UARTs to implement the serial data protocol. The computer sends a frequency control word to the receiver via fiber optic cable #5. A 'local/remote' switch at the receiver selects computer or thumbwheel switch frequency control. The A/D sends eight digitized voltage values back to the computer on fiber optic cable #4. Computer software controls timing and frequency selection. The program records voltage values, averages 10 readings, stores the result on disc or tape and provides a display of the measurements.

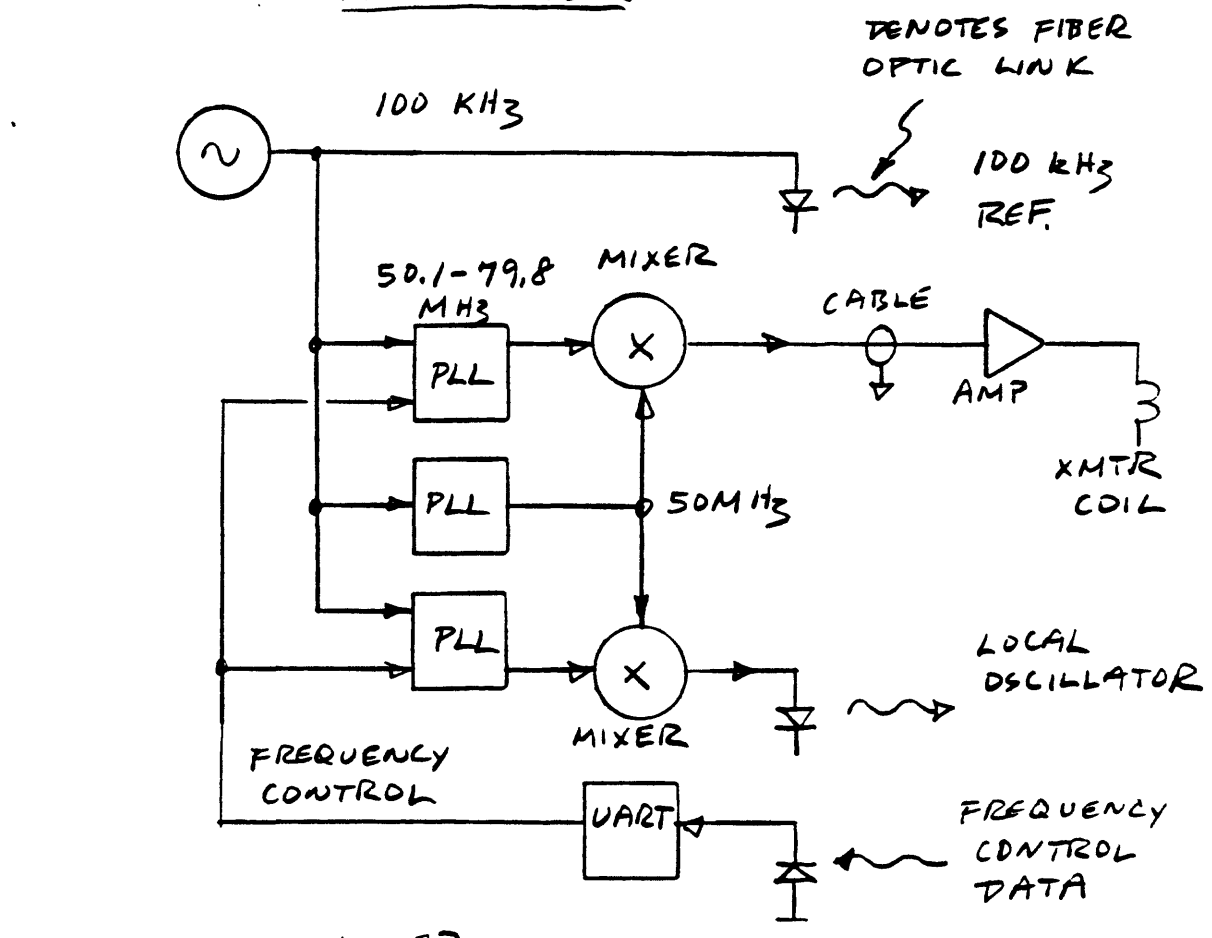
FIGURE 2

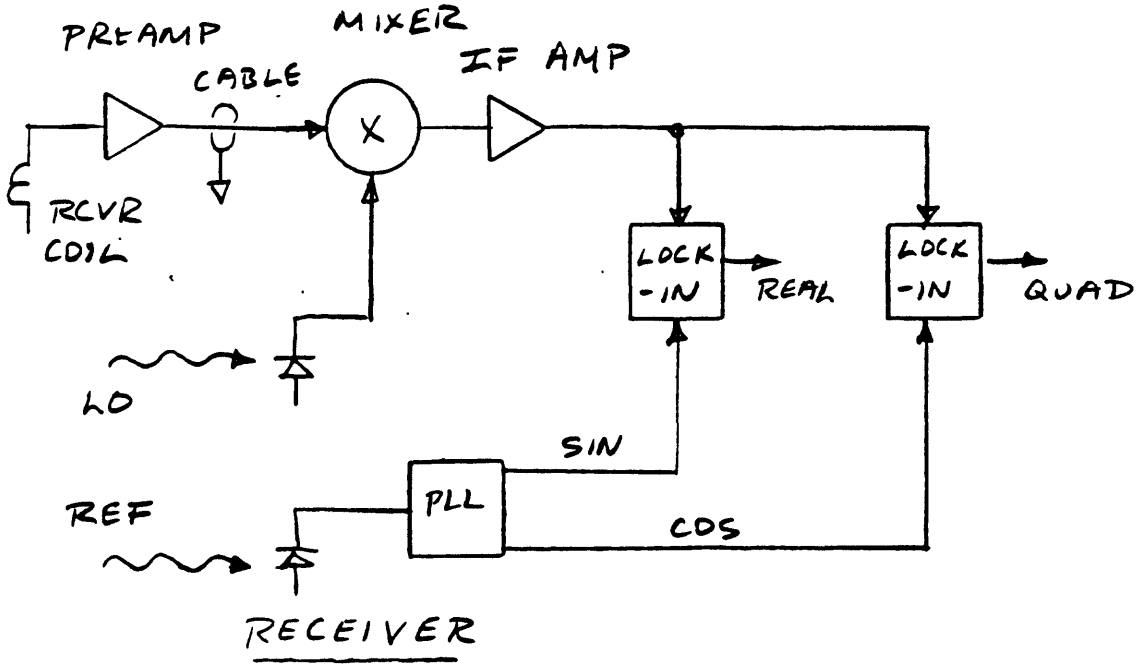


SYSTEM BLOCK DIAGRAM

FIGURE 3

TRANSMITTER





ELECTRONIC BLOCK DIAGRAMS

Results

The sounder has been operated in a variety of test situations in the lab and on two field trips. The aluminum sheet calibration is repeatable with phase changes of two degrees and amplitude variations of about 3%. If the temperature is controlled the variation is reduced. We find that cable orientation and height above the ground must be consistent to avoid large variations. If the receiver coil cable is deployed at right angles to the transmitter coil cable there are 20% changes in amplitude. It is also important to keep the metal equipment boxes off the ground with insulating pads.

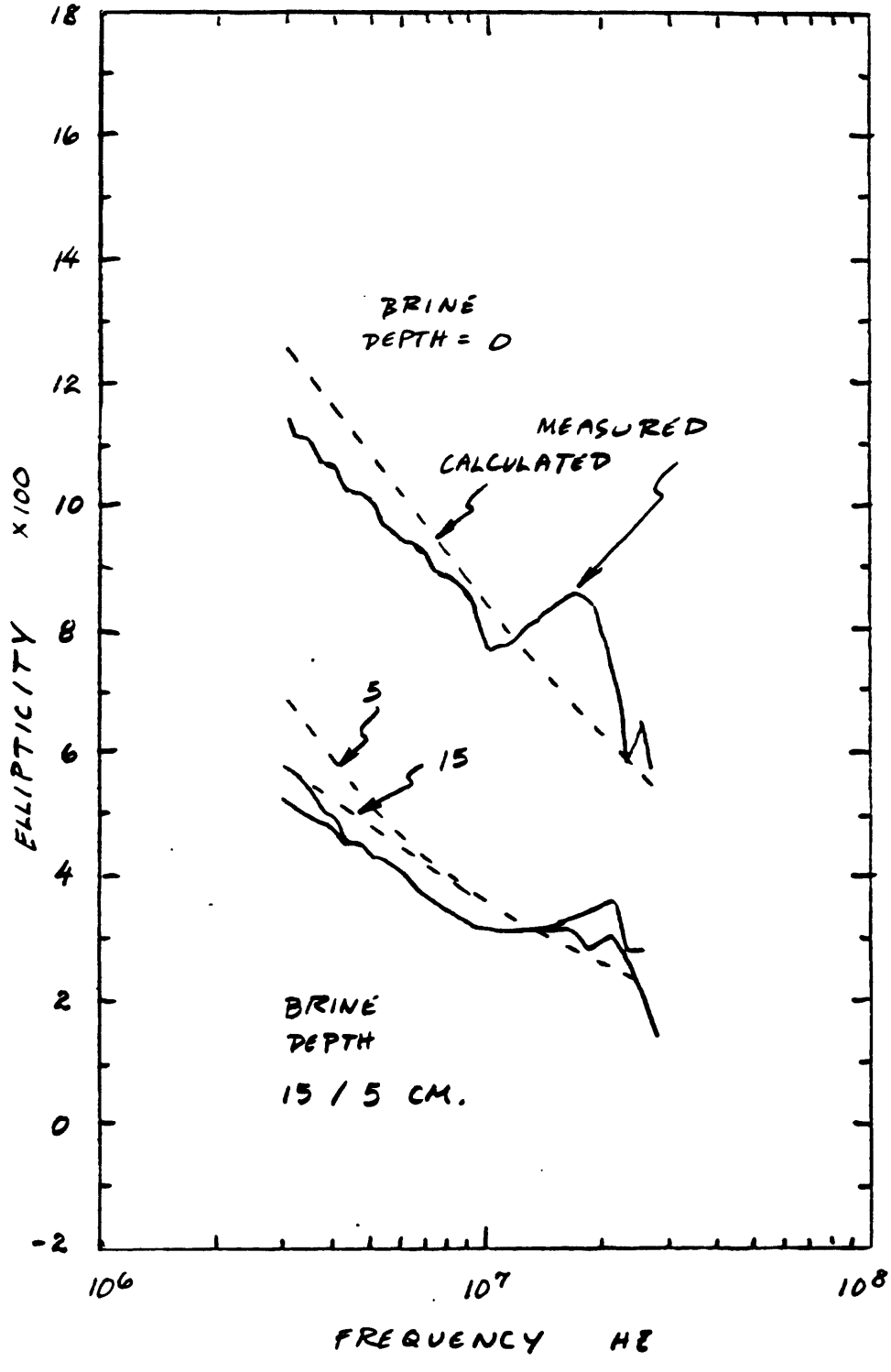
A series of test runs were done in the brine tank in building 5. The brine conductivity is high enough to model the situation with purely conductive current flow. The low frequency field solutions can be used for a comparison of calculated and measured results. The brine was underlain with sand of sufficient depth to be modeled as a half space. The results are shown in figures 4 and 5 for three different brine depths. Coil spacing was 50 cm. The minimum error in ellipticity was 3% at 15 MHz and the worst tilt error was 2 deg at 300 kHz. These correspond to 2% amplitude error and 1 nSec timing error in the RF measurements. This performance approaches laboratory instrument ratings; for instance, the Hewlett Packard HP8495A vector voltmeter has a 0.2 db amplitude accuracy specification and a 1.5 degree phase accuracy specification. The instrument repeatability is about 0.5 degree in tilt and 0.5% in ellipticity. Analog to digital conversion resolution is 12 bits.

The most extensive field test was part of a groundwater contamination study near Cedar Rapids, Iowa. The site was a river bank consisting of silt, clay and sand deposits. Depth to water was about 3.5 meters. There are seven water sampling wells along the survey line. Well logs and water height measurements were available. We did not use the Al sheet calibration.

Soundings were taken at 18 sites with three loop-loop spacings: 1, 2 and 4 meters. The data was inverted using 2 and 3 layer models. Figure 6 shows a comparison of the site cross section as inferred from well logs and that inferred from an inversion of the loop-loop sounding data. In the top cross section the well locations are marked with an x. In the lower section, the sounding locations are shown by arrowheads. The pairs of numbers are resistivity and relative dielectric constant. An inversion was done for the data at each site and the boundaries shown are at resistivities of 10 and 100 ohm meter with the numbers as an average of the inversion values within the boundary. Dielectric constant could not be resolved below the water table.

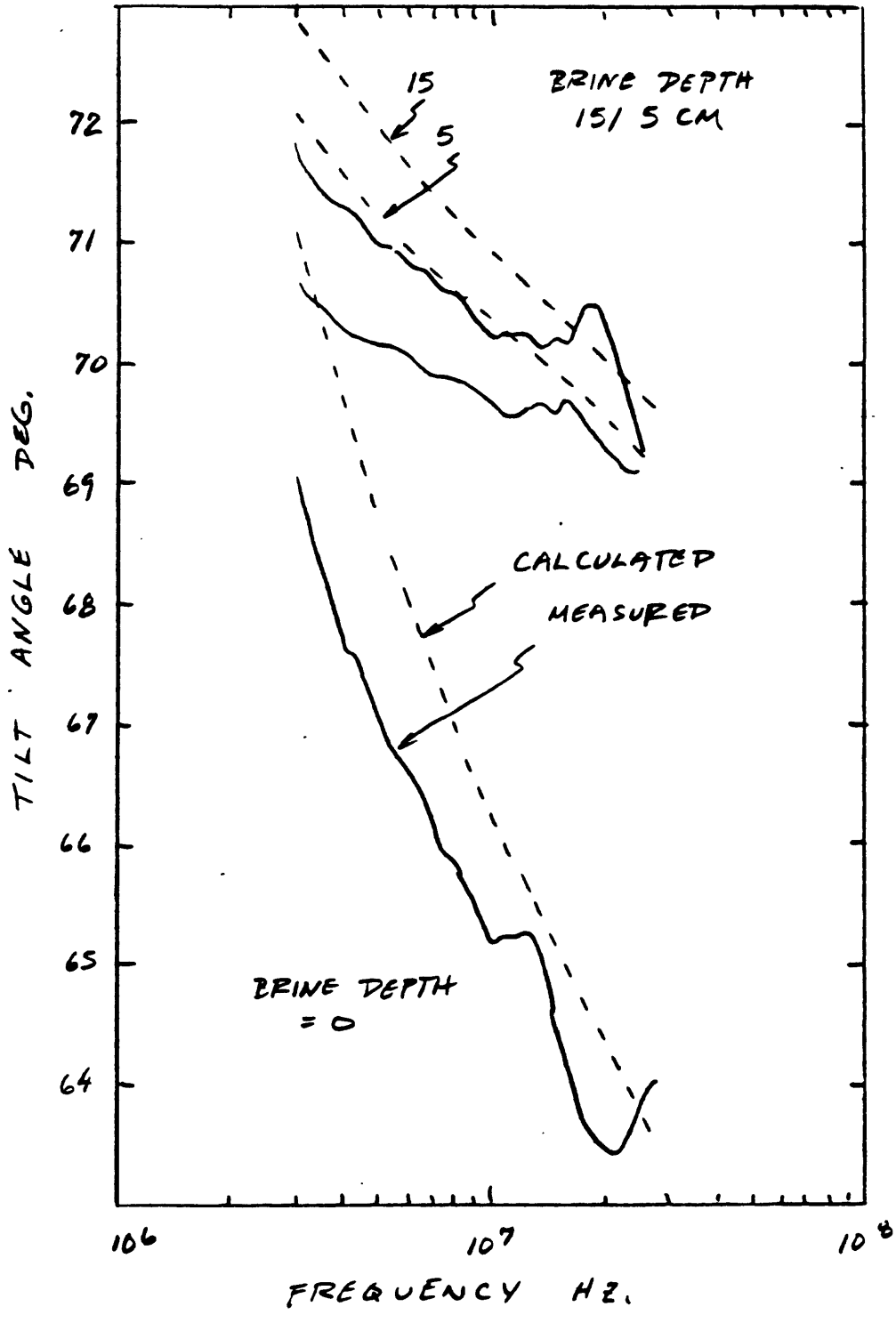
The loop-loop data resolves the shallow sand lenses at the two ends of the survey line. The lowest layer is probably the capillary fringe of the water table. The resistivity and dielectric constant values are reasonable for wet sandy soil.

FIGURE 4



MODEL TEST RESULTS
LOOP SPACING 50 CM

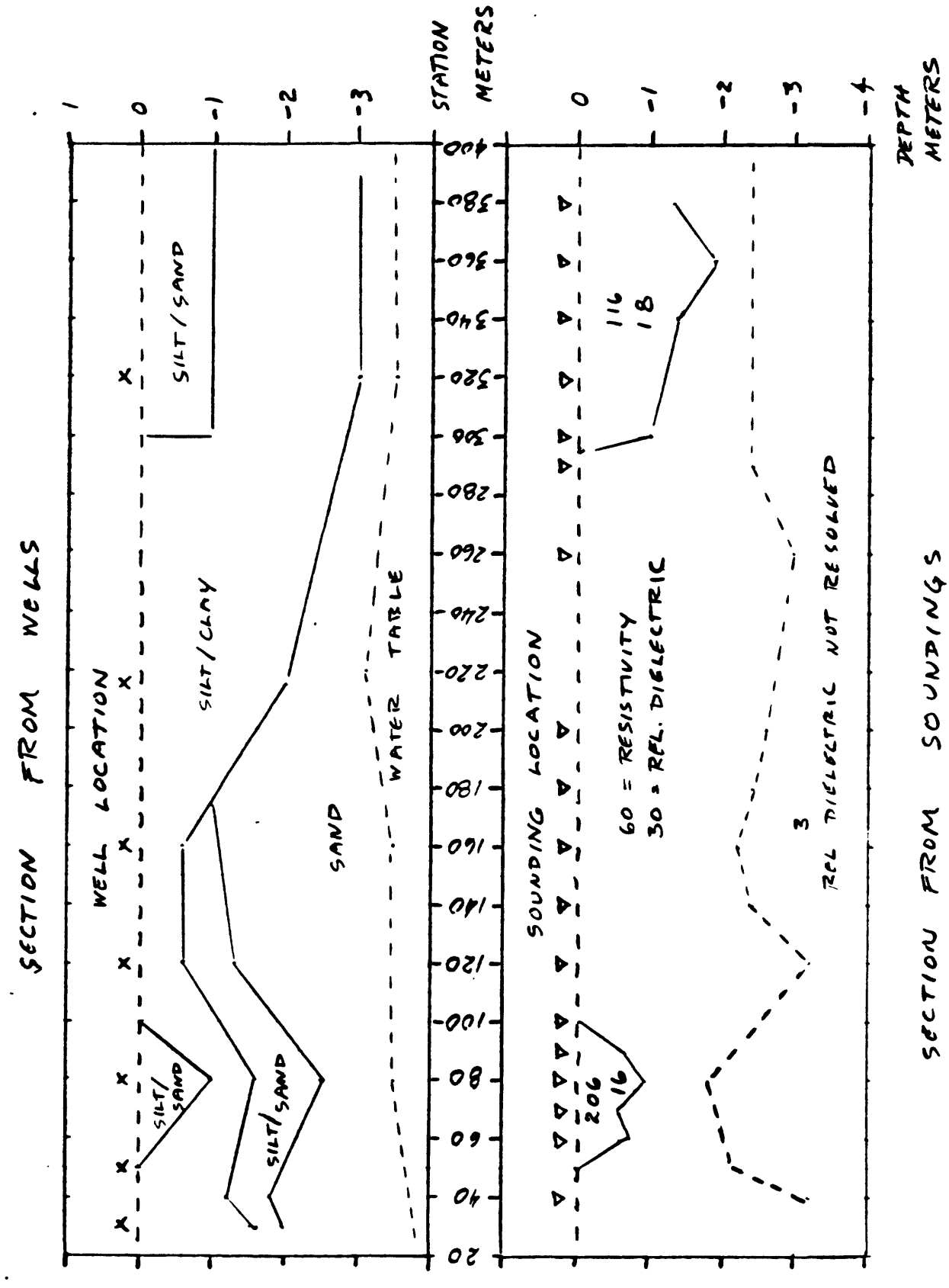
FIGURE 5



MODEL TEST RESULTS

LOOP SPACING 50 CM

FIGURE 6



COMPARISON OF WELL AND SOUNDING DATA

Conclusion

The design and testing of a short wave loop-loop sounder have proven the viability of the concept. It can provide a portable means for near surface electromagnetic exploration. The resolution of 0.5 deg in tilt angle and 1/2% in ellipticity are acceptable for pollution sensing.

Acknowledgments

Walt Anderson initiated the project and recognized the potential of high frequency sounding for pollution monitoring. He wrote the inversion program and extended prior results to the short wave region. Vic Labson encouraged us to try ratio measurements. Dave Wright initiated the use of fiber optics at our lab and supplied test equipment.

References

Kaufman, A.A., and Keller, G.V., 1983, Frequency and transient soundings: Elseview, N.Y., 685 p.

Wait, J.R., 1954, Mutual coupling of loops lying on the Ground: Geophysics, v. 19, p. 290-296.

Appendix - Circuit Description

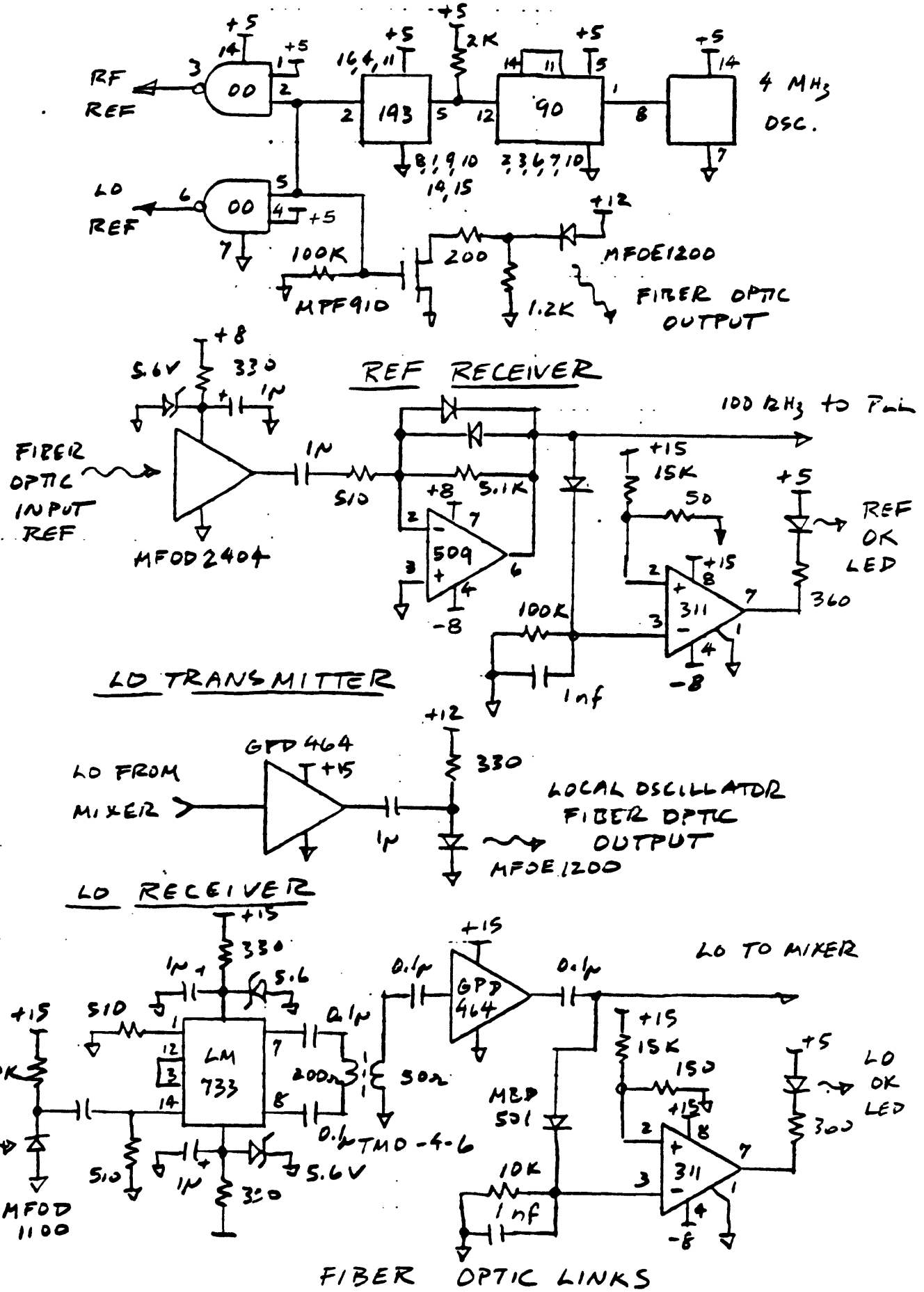
Receiver Circuit Description

The circuitry for the fiber optic links is shown in figure 7. The 100 kHz signal drives a field effect transistor (FET) which operates a light emitting diode (LED), coupled to the fiber optic cable. The cable is 30 ft. long, has a 600 MHz frequency response and a propagation velocity of 60% of the speed of light. A transimpedance amplifier at the receiver boosts a sensor photodiode output and the signal is then amplified by an operational amplifier with a gain of 10 and limiting diodes. A diode senses the peak signal amplitude and a comparator lights an operator LED to indicate that the 100 kHz link is functional.

The local oscillator fiber optic link LED is driven by a cascade of thin film amplifiers for improved frequency response. The amplifiers are manufactured by Avantek. They are fixed gain, typically 14 dB (x5), 50 ohm impedance, 500 MHz bandwidth devices mounted in TO-5 cans. A range of bias currents, 10mA to 100mA, supports signal levels to +24 dBm. The receiver is a photodiode whose output is amplified by a LM733 video amplifier for high input impedance, followed by a GPD amplifier to boost the signal level to the +7 dBm required for optimum mixer performance. The overall frequency response exceeds 100 MHz. A schottky diode peak detector and a comparator drive an operator LED which indicates a functional LO link.

The receiver radio frequency signal path begins with the receiver loop antennas; 12 inch diameter loops mounted in a 14 inch square plywood box. Each loop is centered in the box to allow various coil orientations with no change in distance from the center point to the support surface. The coil is shunted by a 10 ohm resistor for current sensing. The RF signal is amplified ten times by a LM733 video amplifier and transformer coupled to the output

FIGURE 7



FIBER OPTIC LINKS

cable. The transformer breaks a ground loop and lowers the impedance to 50 ohms. The video amp is mounted in the coil box with a 10 foot cable to the receiver console.

The console RF signal path begins with an attenuator to reduce the signal level by 1/10. This selectable attenuator, plus a variable gain amplifier after the IF amplifier, provides 60 dB of gain variation. The dynamic range requirement comes from the 10 to 1 loop spacing range and the cubic relation between distance and magnetic field strength. The mixer is a schottky diode device with 50 ohm port impedances. It has a 50 kHz to 200 MHz frequency response and an insertion loss of 6 dB. The mixer output contains both sum and difference components. Only the 100 kHz difference output is amplified. See figure 8 for a schematic diagram.

The IF amplifier circuitry is shown in figure 9. It has a 6 pole response centered on 100 kHz with a Q of 30 and linear phase response over the center 2 kHz of the passband. The input noise is about 20 nanovolts per root hertz. An input resistor-capacitor network shunts the mixer sum output. An output high pass filter eliminates supply and offset shifts. The main amplifier is a cascade of three FET stages with tuned drain loads. The cascode circuit connection eliminates oscillation. Each tank circuit has a Q of 50 and they are stagger tuned to yield a linear phase response. This tuning reduces phase shifts with temperature. An output operational amplifier boosts the drive capability and provides gain calibration. The nominal setting provides one volt at the DPM for one millivolt at the coil with the attenuator at 1/10 and the variable gain set at 100 on the DPM.

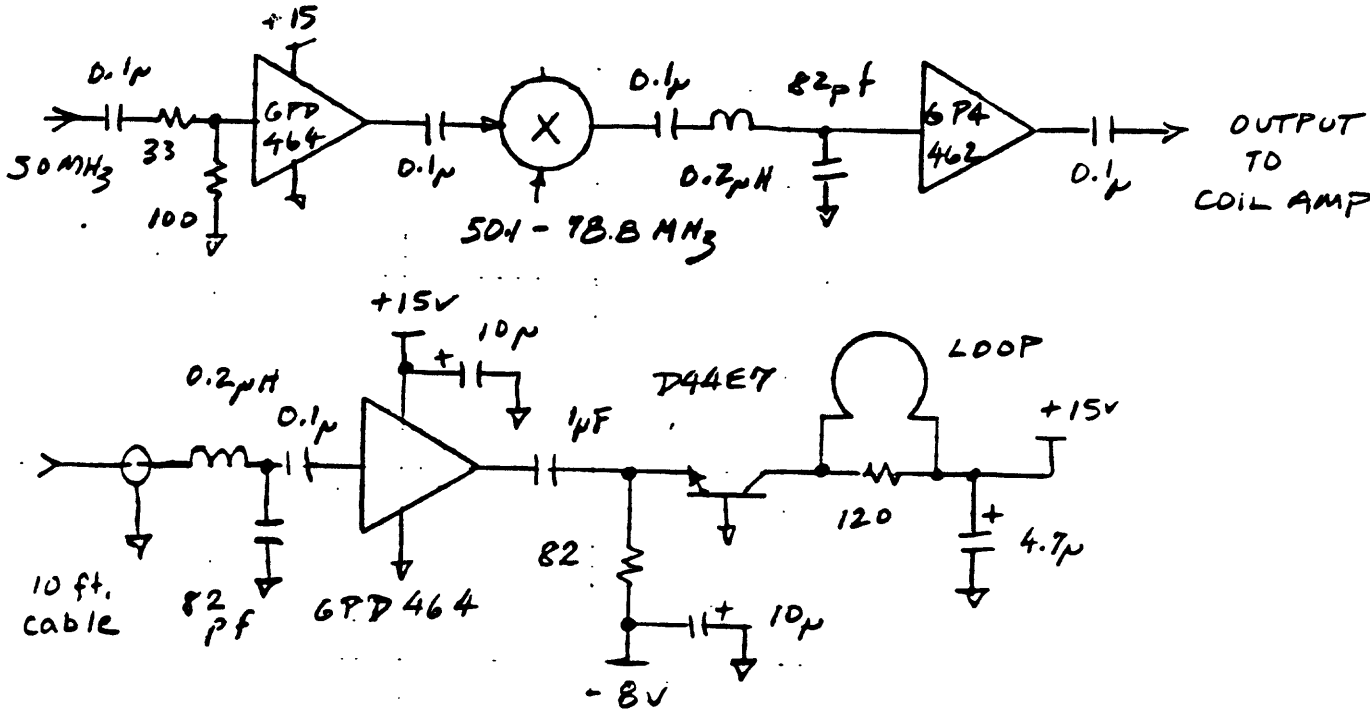
The circuitry of figure 10 is the lock-in portion of the receiver. The 100 kHz reference is input to a comparator with a 0.15 volt threshold and converted to 5 volt logic levels. The '4046 is a phase lock loop operating at 400 kHz. It contains a voltage controlled oscillator and phase sensitive detector. The 400 kHz output is divided by 4 in a '193 counter and compared with the reference. The 100 kHz and 200 kHz signals go to two gates which produce the SIN and COS reference signals. The PLL chip has a lock indicator output which drives an LED to indicate proper operation of the 100 kHz reference to the operator.

The IF output is sent to a AD539 variable gain amplifier. This provides 40 dB of the dynamic range requirement. The gain is proportional to the pin 1 voltage and can be adjusted by the operator and displayed on the DPM.

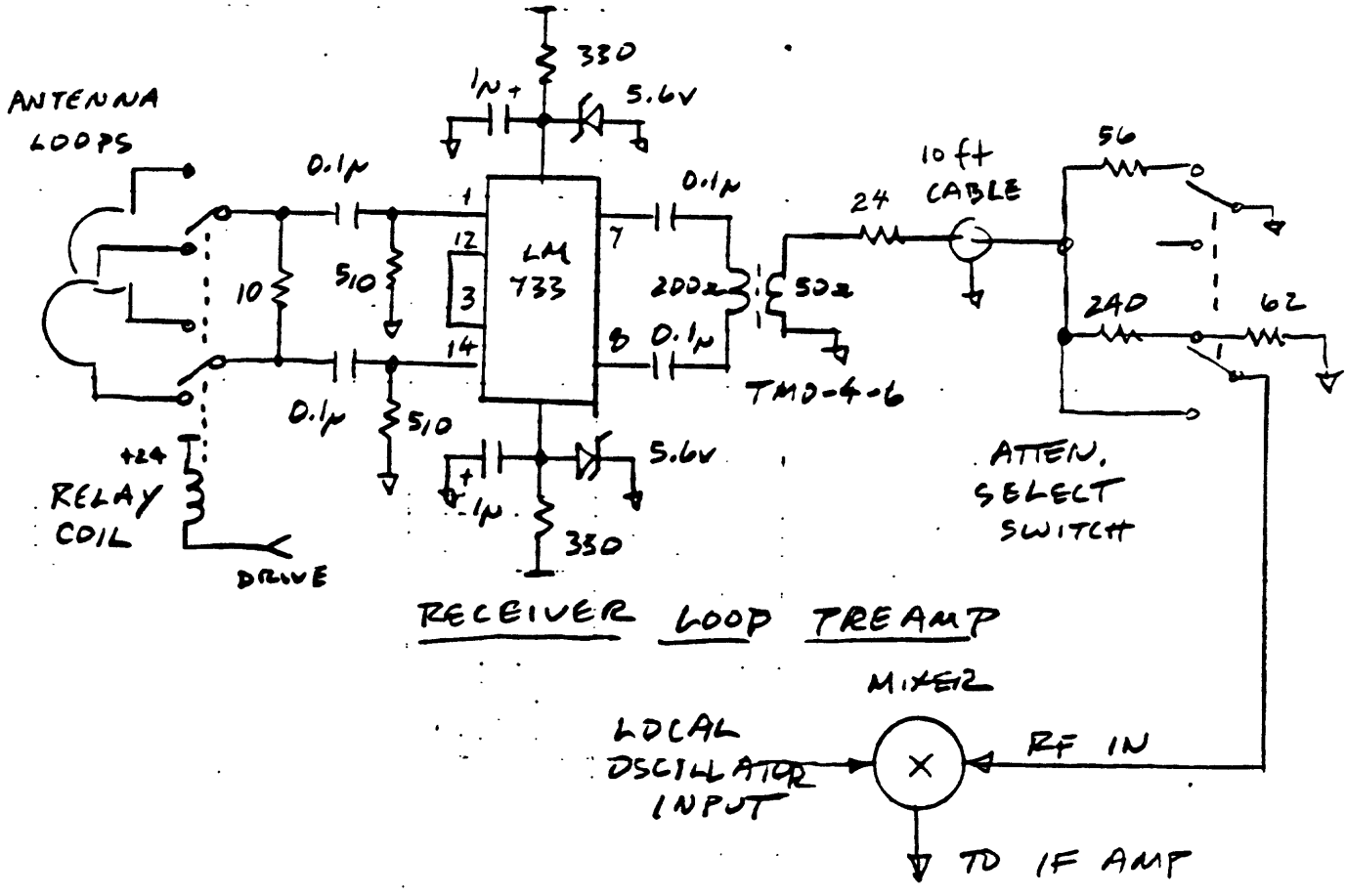
Synchronous detection is performed by two AD630s. These contain switched amplifiers with gains of +1 and -1. The switching is controlled by the SIN and COS reference signals. The detected output is low pass filtered at 1 Hz and sent to the DPM. These devices can recover a signal completely buried in noise and have 0.1% gain accuracy.

Auxiliary circuits in the receiver provide temperature readout, low battery detection, panel meter input and remote frequency control. A third fiber optic link is used to send the frequency control signal from the receiver to the transmitter. See figure 11 and figure 12 for schematic diagrams. There are ten input bits, selected 4 or 6 at a time by '244 tristate buffers. The low and high order words are indicated by the most

FIGURE 8



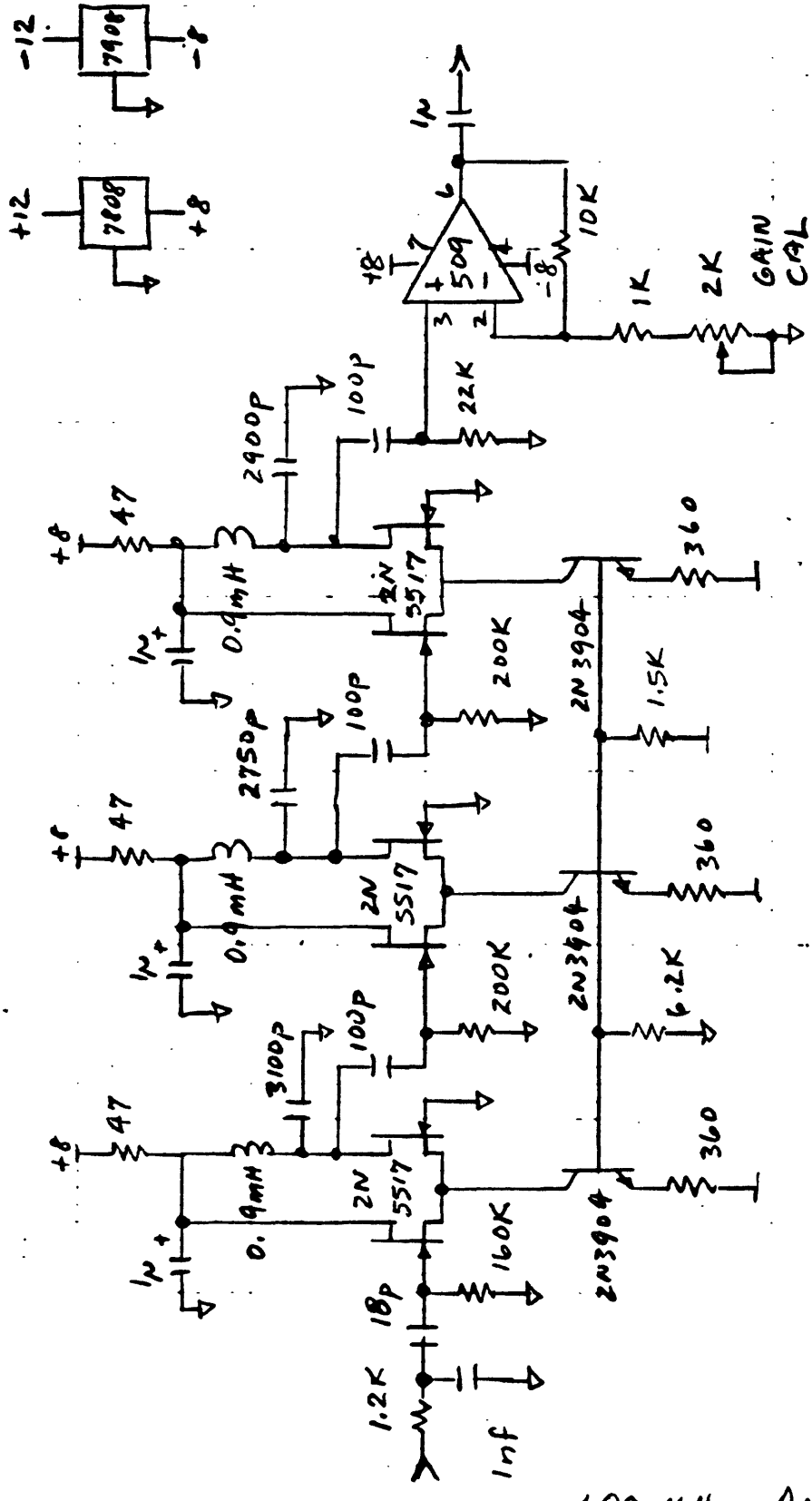
TRANSMITTER LOOP DRIVER



RECEIVER LOOP PREAMP

SCHEMATIC - COIL CIRCUITS

FIGURE 9



CF = 100 kHz
3db ± 3 kHz
GAIN - adj - about 500
e_{IN} ~ 1μV

40 db ± 27 kHz

SCHEMATIC - IF AMPLIFIER

100 KHz AMPLIFIER

FIGURE 10

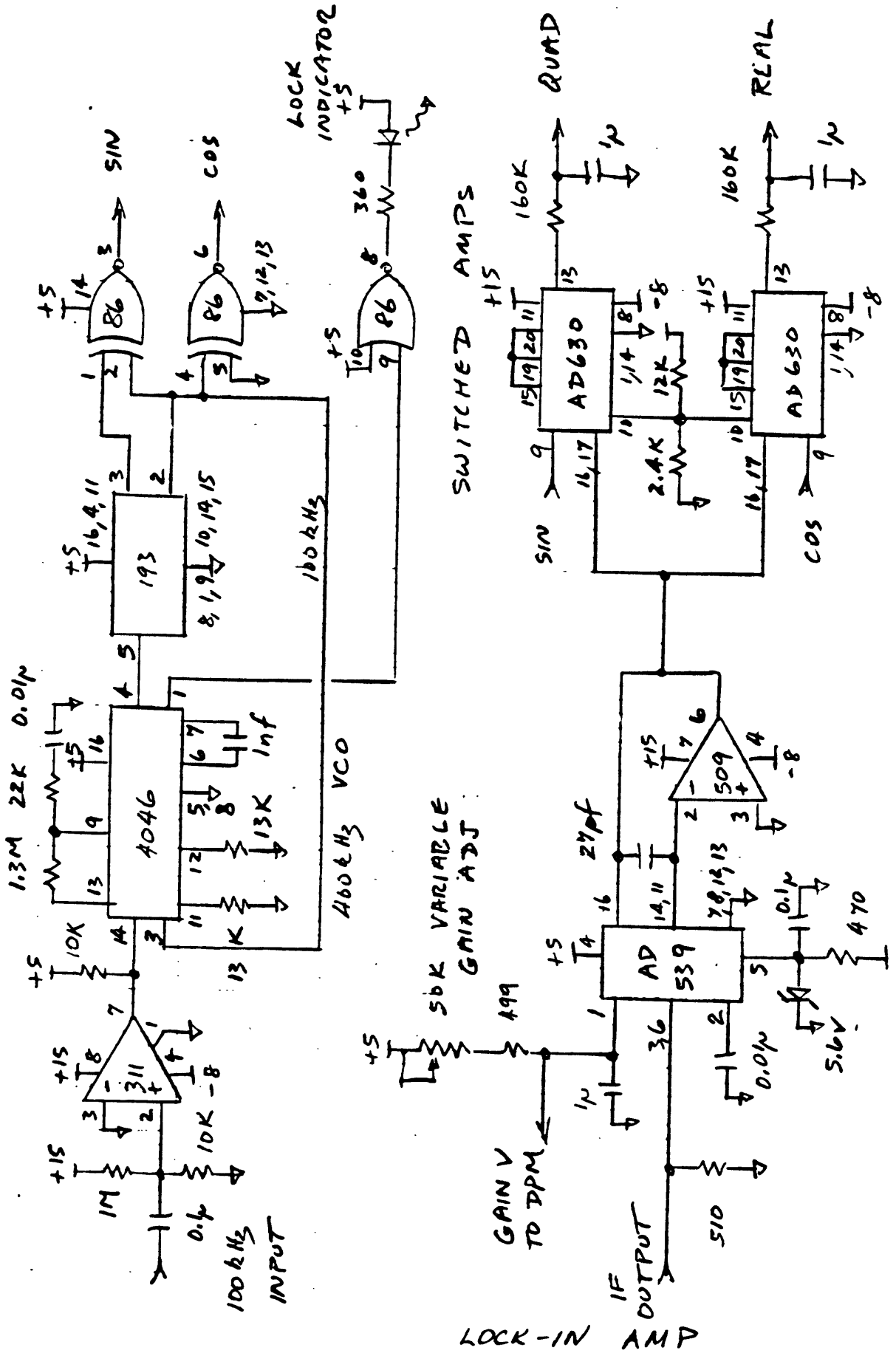

LOCK INDICATOR
SIN
COS
86
193
4046
311
AD630
AD539
509
SWITCHED AMPS
QUAD
REAL
SIN
COS
460 kHz VCO
100 kHz INPUT
GAIN V TO DPM
IF OUTPUT
LOCK-IN AMP
SCHEMATIC - LOCK-IN AMPLIFIER, REF PLL

FIGURE 11

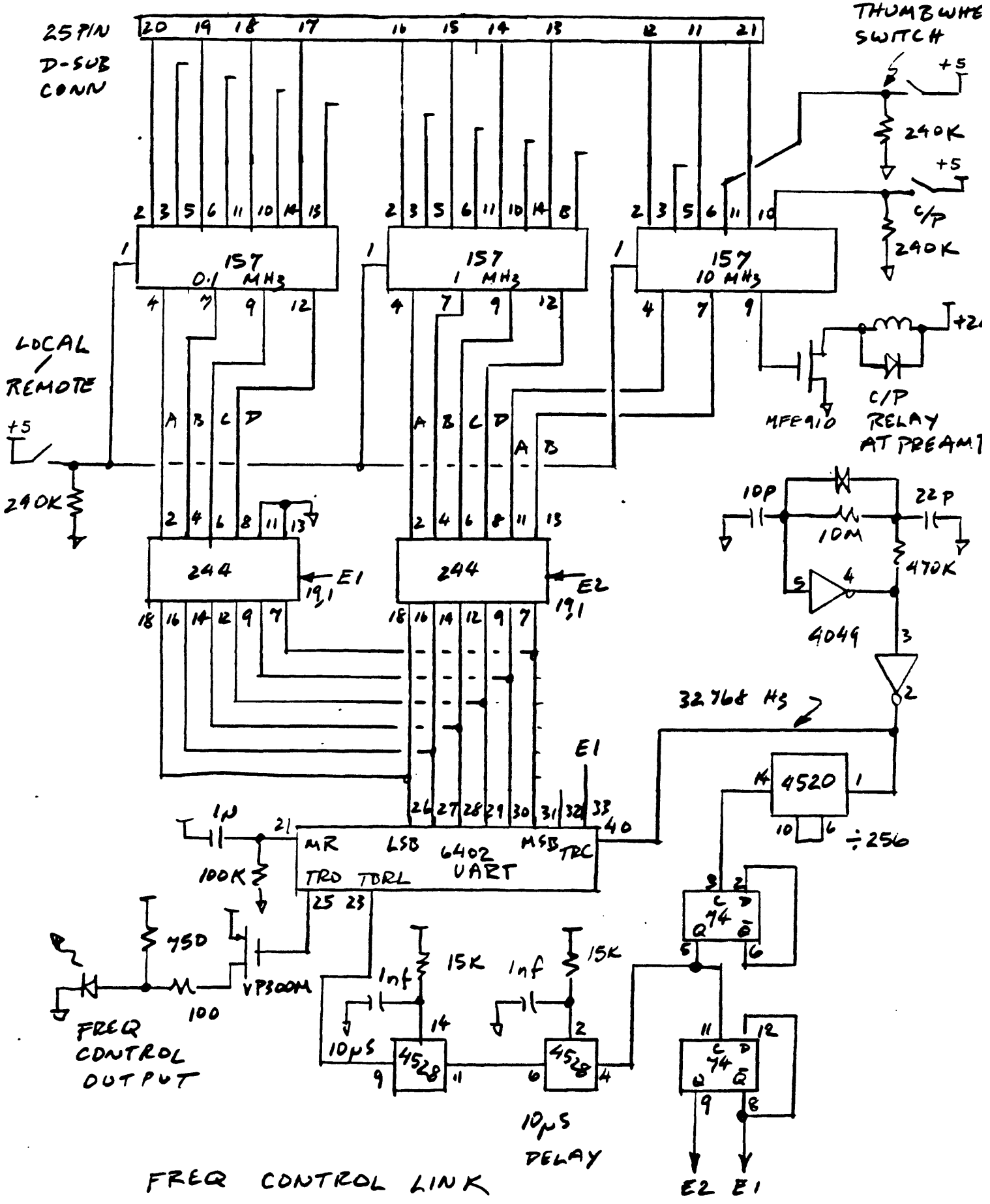
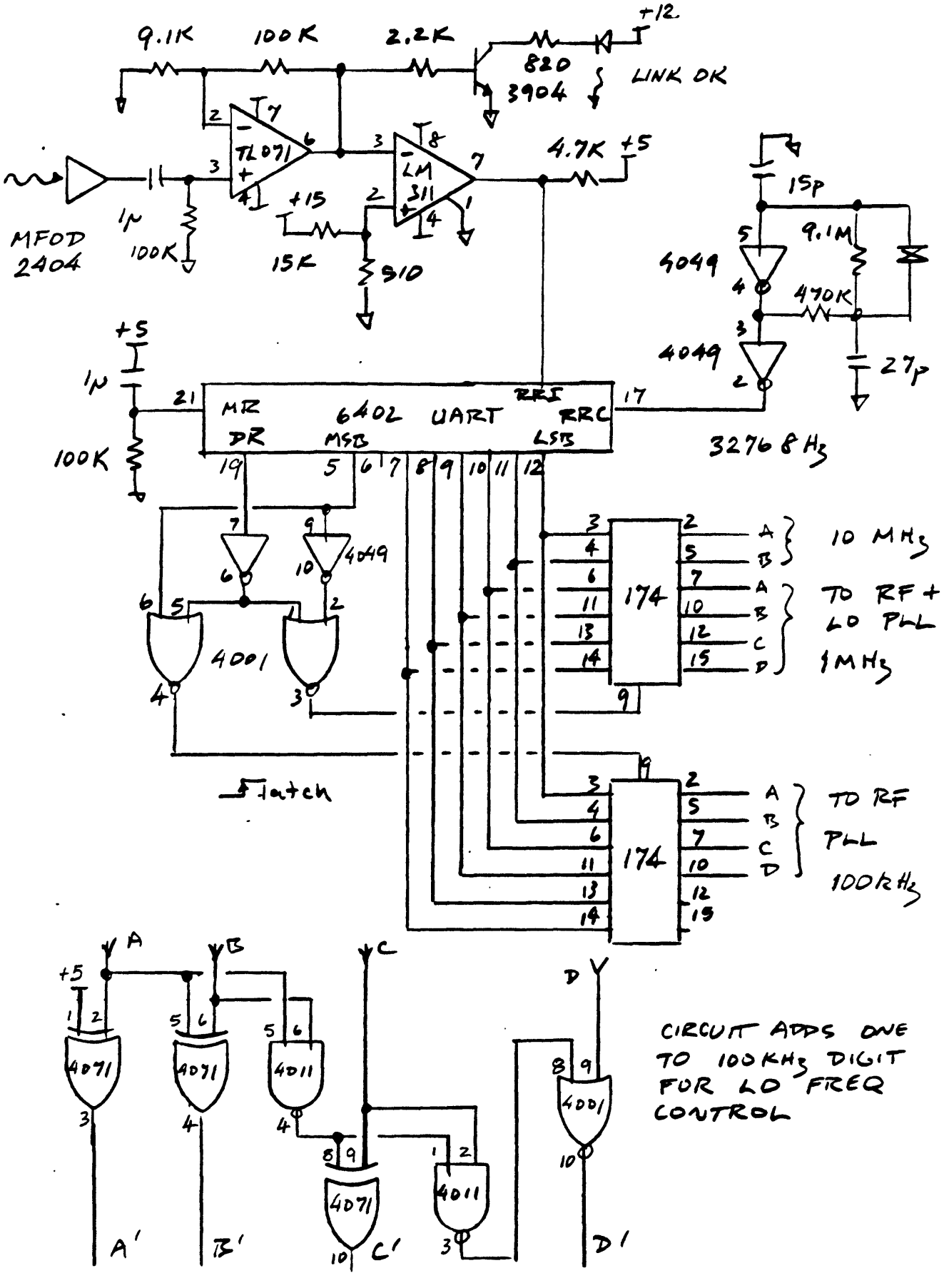

25 PIN D-SUB CONN
20 19 18 17 16 15 14 13 12 11 21
THUMBWHEEL SWITCH
+5
240K
C/P
157 0.1 MHz
157 1 MHz
157 10 MHz
LOCAL / REMOTE
MFE910
C/P RELAY AT PREAMP
244
E1
E2
10P
22P
10M
470K
4049
32.768 KHz
4520
÷256
MR LSB 6402 UART MSB TRC
TRO TDRL
100K
750
VP800M
100
FREQ CONTROL OUTPUT
1nf
15K
10µS
4528
74
10µS DELAY
FREQ CONTROL LINK

FIGURE 12



FREQUENCY CONTROL

significant bit (MSB). The circuit uses a UART clocked at 32768 Hz. A counter string generates the MSB, a transmit pulse and 'enable' control signals for the '244 chips. New frequency control values are sent within 32 milliseconds. The process is reversed at the transmitter where the optical pulses are amplified to logic levels and input to another UART. The 6 data bits are sent to two latches. The MSB of the data word controls which latch is loaded by the 'data ready' output of the UART. The latch contents are updated alternately. The 32768 Hz clock avoids harmonic interference with the 100 kHz reference frequency.

Transmitter circuit description

The system reference is a 4 MHz oscillator with a divider chain to 100 kHz. 100 kHz crystals are large and fragile. The reference accuracy and long term stability are not important, only the short term drift and phase noise. The divider chain improves performance in both these areas. The reference is sent to the receiver and three phase lock loops. One PLL reference is shown in the schematic diagram of figure 13.

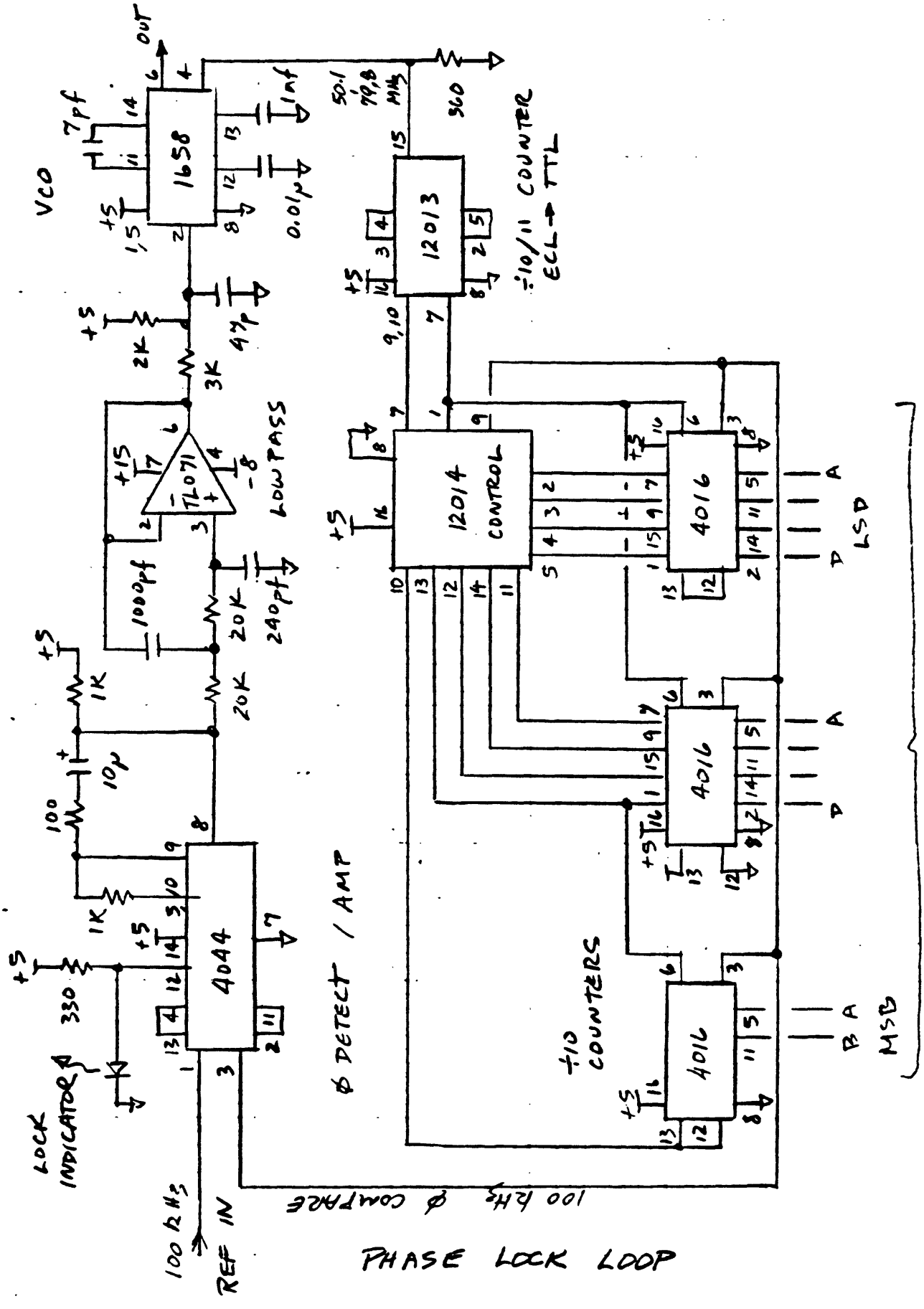
The phase lock loops use '1658 voltage controlled astable multivibrators. These are emitter coupled logic (ECL) circuits which can operate from the audio range to 150 MHz. A 7 pf capacitor sets the tuning range. For our circuit a 3 to 5 volt input provides a 40 MHz to 90 MHz output. The astable output is 0.8 volt peak and can drive 50 ohm lines.

The astable output frequency is divided down by another ECL circuit, the '12013. This IC has 5 volt logic level outputs at 1/10 or 1/11 of the input frequency. This variable modulus division is under the control of a '12014. It permits division by every integer, not just by 110, 120, The controller inserts occasional divisions by 11 to provide overall ratios of 110, 111, 112, ... The 5 volt level output goes to a cascade of three decade counters. These counters are preset to a number given by the frequency control and count down to zero. The '12014 detects an all zero state, presets the counters and drives the '4044 phase comparison input.

The narrow pulse indicating completion of a count sequence is input to a 4044 phase detector. The pulse sets a flip-flop which turns on a positive charge pump. The flip-flop is reset by the 100 kHz reference which turns on a negative charge pump. The charge pump outputs are amplified and low pass filtered twice. One low pass is in the '4044, the other is an external operational amplifier circuit. This charge pump signal is then applied to the astable oscillator control pin to close the phase lock control loop.

The circuit gain is high enough that a one degree of phase shift will cover the entire tuning range. In actual operation the timing of logic switching will cause larger phase shifts which can vary with the frequency set point. The loop settling time is about 10 millisec and the second filter produces a non-dominant pole which reduces phase jitter at the astable oscillator. Loop instability has been seen at a few frequency setpoints, particularly subharmonics of 50 MHz, and filter parameters were adjusted to eliminate the problem. Instability manifested itself as a noisy readout which varied over a 10 digit range.

FIGURE 13



PHASE LOCK LOOP

The frequency control inputs of 001 to 298 are converted to divider chain control numbers by addition circuits. The first digit has five added, and the middle and last digits are unchanged for the RF frequency control. The last digit has one added for the local oscillator control. Addition uses logic gates and holds the '4' digit high to convert 0, 1, 2 to 5, 6, 7.

The 50 MHz PLL has a fixed divider chain at 500 whose first stage is a '12013 counter set for division by 10. This is followed by two '90 counters with divisions of 10 and 5. The phase detector is built from gates and the charge pump is two FETs. The 50 MHz ECL level signal is split by a resistor network and boosted to +7 dBm by two GPD amplifiers before being input to the mixer's LO input ports.

The mixer section generates 0.1 MHz to 29.8 MHz outputs from the 50 MHz signal and 50.1 MHz through 79.8 MHz voltage controlled oscillator inputs. See figure 4 for a schematic diagram. The mixer outputs are low pass filtered at 40 MHz to eliminate sum products and then buffered by GPD amplifiers. Output levels are about +5 dBm. One signal goes to the local oscillator fiber optic link. The other signal goes to the transmitter coil driver via a 50 ohm cable.

The transmitter coil is similar to the receiver coil. It is excited by a single D44 transistor with a 50 ma current. The transistor is driven at its emitter (common base connection) by a high power GPD amplifier. See figure 8 for a schematic diagram. Emitter drive boosts the frequency response to the 250 MHz transistor limit but the circuit has no current gain. Phase shift is dominated by the 2-pole resonance of the transistor output capacitance of 80 pf with the coil inductance of 1.2 microhenry. This results in 90^{o} of phase delay at 16 MHz.

Computer Interface

Hand recording of data and subsequent transfer to the branch computer is error prone and labor intensive. After some experience with the sounder we added a data acquisition system (DAS) which could generate machine readable data records. It comprises an analog to digital convertor, latch circuits and a UART at the receiver and a fiber optic link to a computer. The fiber optic link removes computer noise from the vicinity of the sounder. The communication uses a general purpose RS-232 serial link. We have operated the system with Hewlett Packard HP85 and HP110, Toshiba T1000 computers.

The data set was upgraded by using more frequencies and measuring the coplanar and perpendicular response at every frequency. With four measurements (in-phase and quadrature amplitudes for two antenna orientations) we can compute the tilt angle and ellipticity at each frequency. These ratio parameters provide information about surface properties equivalent to the magnitude and phase measurements. The ratios are much less affected by instrumentation artifacts because the only change is antenna orientation; the same electronics are used for both coplanar and perpendicular response measurements.

DAS operation uses the computer to select a frequency and an orientation and to transmit appropriate RS-323 control words to the receiver A/D. The sounder performs the measurement and the A/D converts the results to serial

data words which are returned to the computer. The process is repeated at various frequencies to generate the sounding curve. The computer writes the data to a storage disc or tape for later analysis. We measure in-phase and quadrature amplitudes, temperature, battery voltage, gain control voltage, the X1-X10 attenuator switch position, a zero level and a reference voltage. Normally only the in-phase and quadrature amplitudes are stored. The computer adds a preamble to the data record describing the equipment setup and surface conditions.

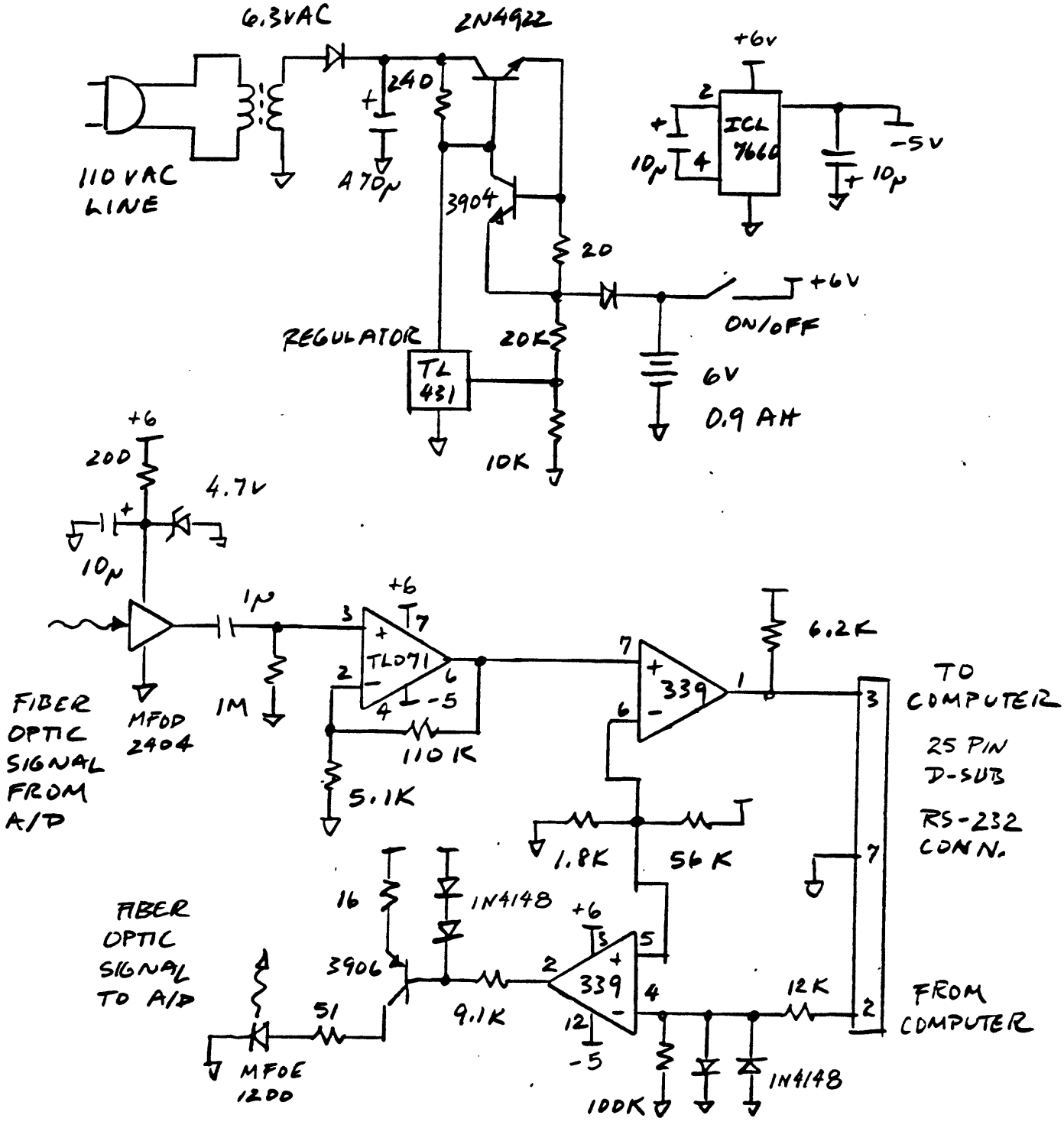
The link begins at the computer serial port with the RS-232 to fiber optic interface diagrammed in figure 14. The unit can be line powered or battery operated. It contains amplifiers and drivers for the fiber optic signals and a battery charger. We don't use all of the RS-232 lines. Communication is at 1200 baud with 8 data bits and odd parity.

The A/D converter at the receiver has the following functions: a. convert serial computer signals to frequency control bits and convert digital numbers to serial data. The serial to parallel conversion uses a UART. b. display frequency data for system test and checkout. c. Accept 8 analog voltages and convert them to 12 bit digital values. The computer serial output is 5 words long. Each word is presented in parallel form at the UART output and latched by '4042s (see fig. 11). The first word is the orientation, coded by a 2 (perpendicular) or an 8 (coplanar) in the lower four bits. The next three words are the three frequency digits, most significant digit first. These first 4 words must have zeros in the upper four bits. The last word must be the ASCII symbol for a carriage return: 0d in base 16. The clocking logic is reset by the carriage return (CR) symbol. The UART 'data ready' line is ANDed with a counter output to successively latch each digit.

The frequency control digits go to '4543 seven segment decoders for the frequency display. They also go to '157 data selectors in the receiver box. The second input to the data selectors is the frequency control thumbwheel switch. A 'local/remote' switch on the receiver panel selects the computer or thumbwheel frequency. Refer to figure 11 for the details of the selection switch operation.

The analog to digital conversion and data transmission to the computer uses the UART to send 16 serial words. Each word pair has 8 low order bits in the first word and 4 high order bits in the second. Conversion begins 0.5 seconds after 'CR' is received to allow the receiver lock-in amplifier to settle. A DG508 multiplexer selects one voltage to input to the MAX162 conversion chip. Reading and conversion is done at 17 Hz rate. When 8 voltages have been read a flip-flop is reset and the circuit waits for the next 'CR'. See figure 15 and 16 for the schematic diagrams.

FIGURE 14



RS-232 TO FIBER OPTIC INTERFACE

FIGURE 15

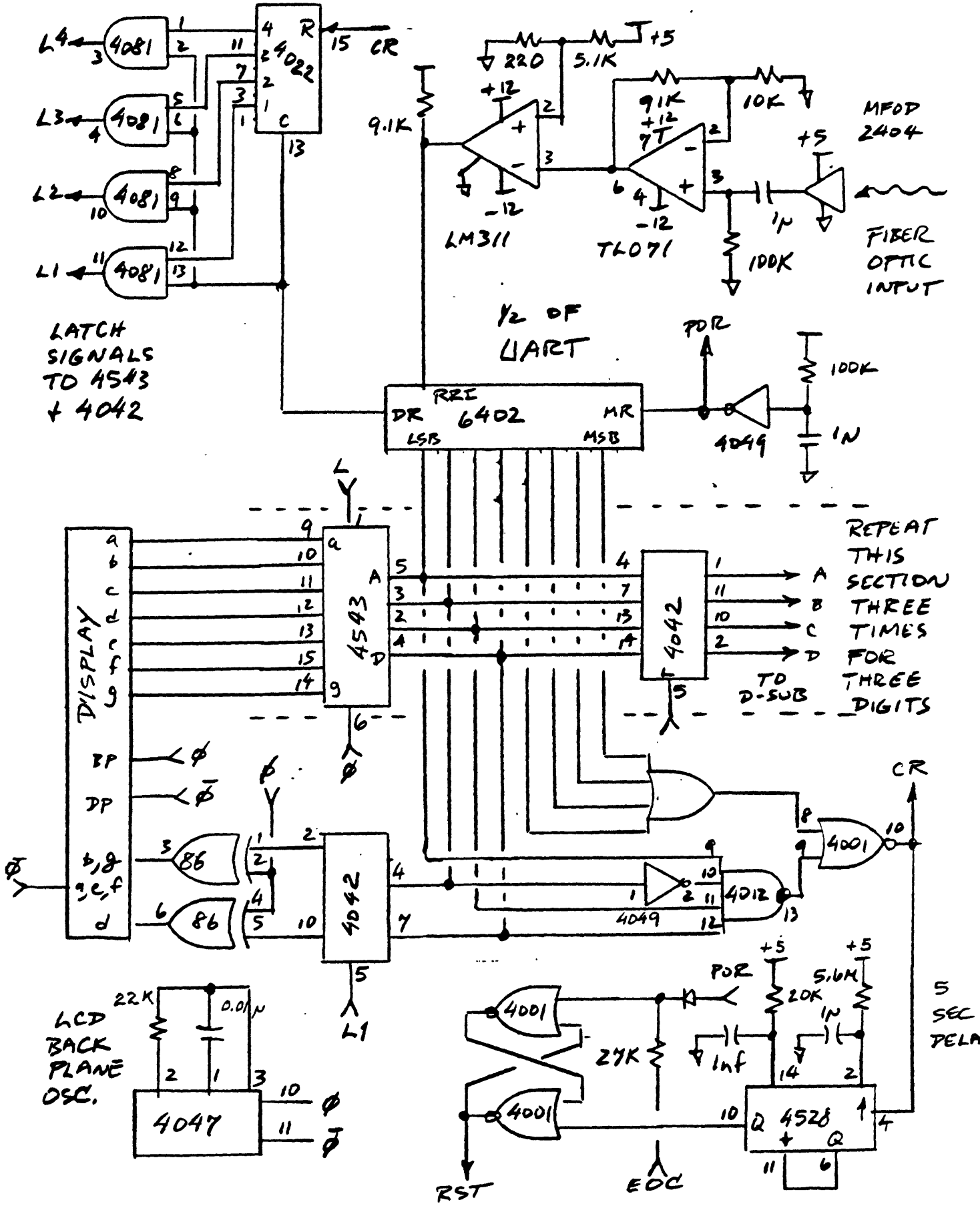
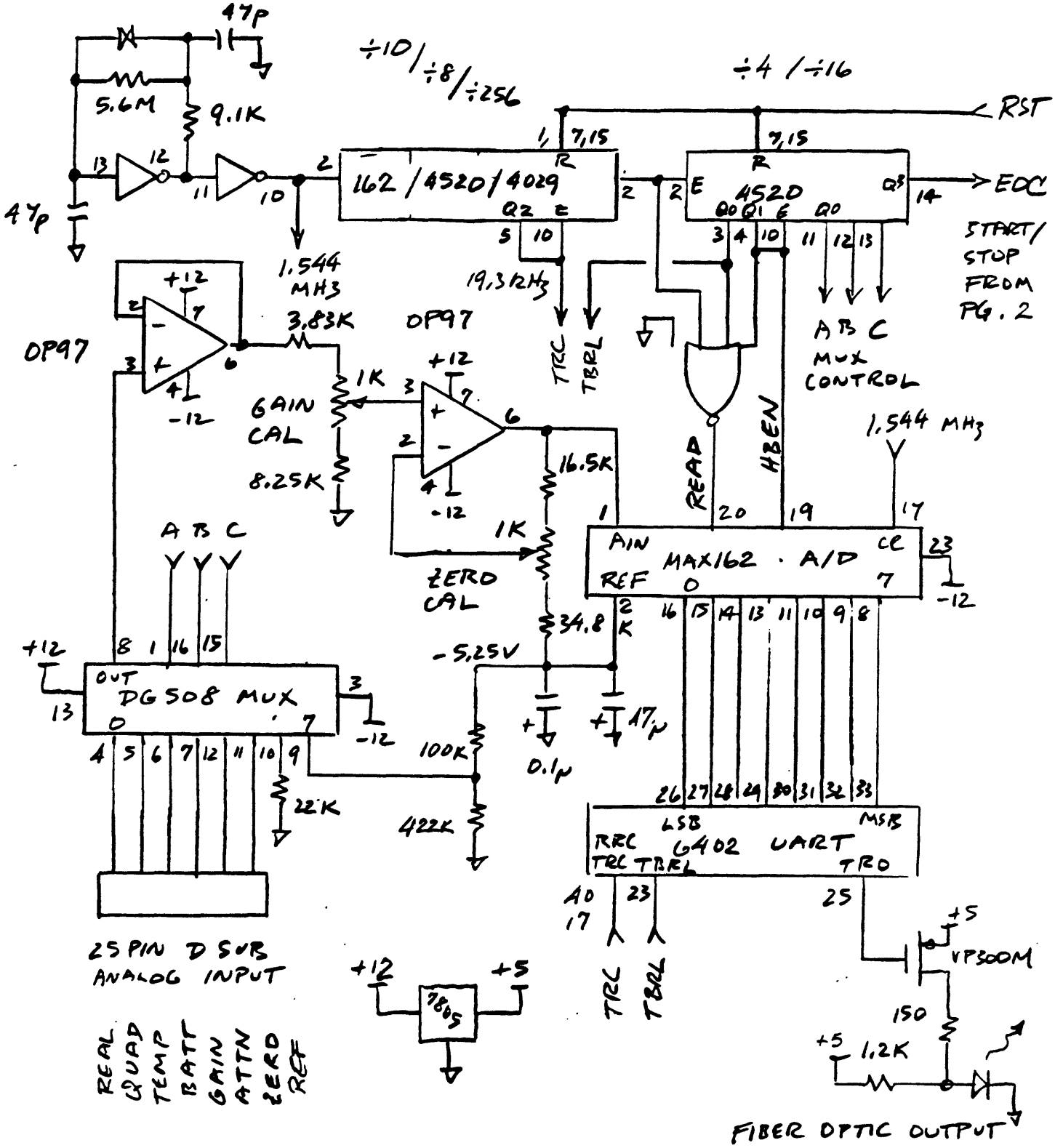

L4
L3
L2
L1
4081
4022
R
CR
LATCH SIGNALS TO 4543 + 4042
220
5.1K
+5
9.1K
+12
-12
LM311
91K
10K
TL071
MFOD 2404
1μ
100K
FIBER OPTIC INPUT
½ OF UART
RRI
6402
DR
MR
LSB
MSB
POR
4049
1N
REPEAT THIS SECTION THREE TIMES FOR THREE DIGITS
TO D-SUB
DISPLAY
4543
4042
BP
DP
86
4001
4012
LCD BACK PLANE OSC.
22K
0.01μ
4047
27K
1nf
5.6M
20K
4528
RST
EOC
5 SEC DELA
A/D CONVERTER PAGE 1 OF 2

FIGURE 16



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